Evaluating the ADRF5515A Dual-Channel, 3.3 GHz to 4.0 GHz, 20 W Receiver Front End

FEATURES

- Full featured evaluation board for the ADRF5515A
- Easy connection to test equipment
- Thru line for calibration

EQUIPMENT NEEDED

- DC power supplies
- Network analyzer

GENERAL DESCRIPTION

The ADRF5515A is an integrated, dual-channel, 3.3 GHz to 4.0 GHz, 20 W receiver front end ideally suited for time division duplexing (TDD) wireless infrastructure applications. The ADRF5515A consists of a high power switch and a two-stage low noise amplifier (LNA) on each channel.

This user guide describes the ADRF5515A-EVALZ, designed to easily evaluate the features and performance of the ADRF5515A. A photograph of the ADRF5515A-EVALZ is shown in Figure 1.

The ADRF5515A data sheet provides full specifications for the ADRF5515A. Consult the ADRF5515A data sheet in conjunction with this user guide when using the ADRF5515A-EVALZ.

ADRF5515A-EVALZ PHOTOGRAPH

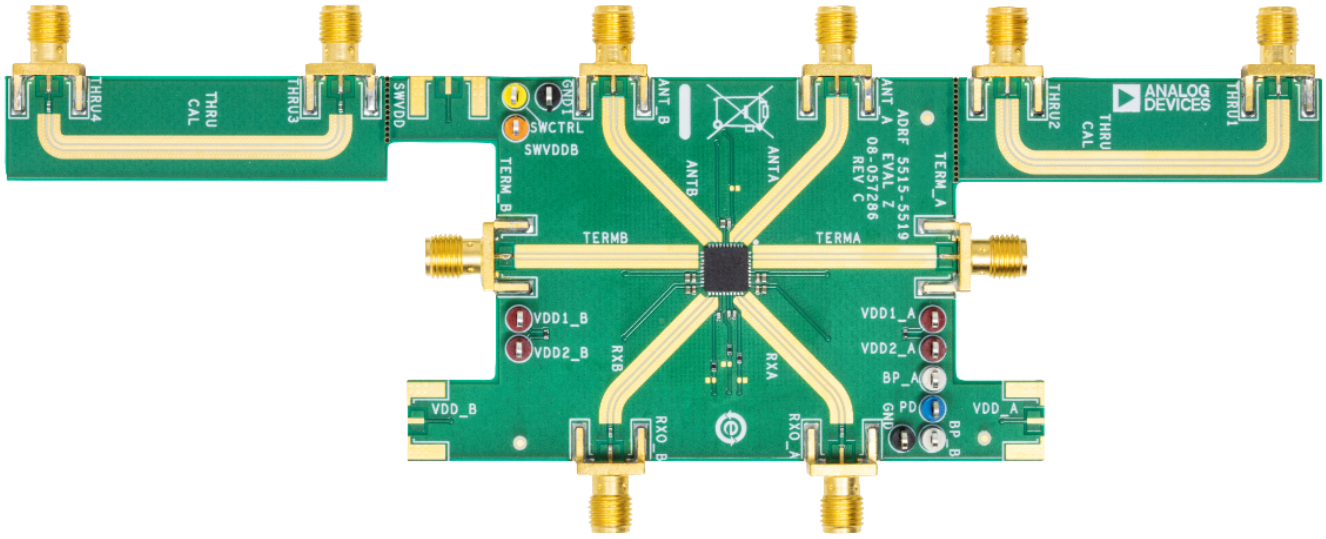

Figure 1.

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REVISION HISTORY

6/2021—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OVERVIEW

The ADRF5515A-EVALZ is preinstalled with connectors (end launch SMA) and assembled with the ADRF5515A and its application circuitry. All components are placed on the primary side of the ADRF5515A-EVALZ. An assembly drawing for the ADRF5515A-EVALZ is shown in Figure 8. An ADRF5515A-EVALZ schematic is provided in Figure 9.

ADRF5515A-EVALZ LAYOUT

The ADRF5515A-EVALZ is designed using RF circuit design techniques on an 8-layer printed circuit board (PCB). The PCB stack-up is shown in Figure 2.

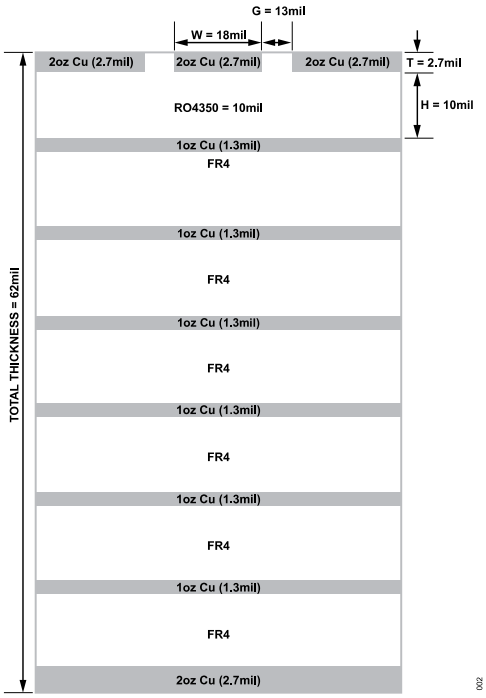

Figure 2. Evaluation Board Stack-Up

The outer copper layers are 2 oz (2.7 mil) thick and the inner layers are 1 oz (1.3 mil) thick. The top dielectric material is 10 mil Rogers 4350B, which provides 50 Ω controlled impedance and optimizes high frequency performance. The remaining six dielectric layers are FR4 based filler layers that improve the mechanical strength of the ADRF5515A-EVALZ and meet the overall board thickness of 62 mil.

All RF traces are routed on the top layer, and the remaining seven layers are ground planes that provide a solid ground for RF transmission lines and help to manage thermal rise on the ADRF5515A-EVALZ during high power operations.

The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 18 mil and ground spacing of 13 mil to have a characteristic impedance of 50 Ω. Ground via fences are arranged on both sides of a CPWG to improve isolation between nearby RF lines and other signal lines.

The exposed ground pad of the ADRF5515A, which is soldered on the PCB ground pad, is the main thermal conduit for heat dissipation. The PCB ground pad is densely populated with filled through vias to provide the lowest possible thermal resistance path temperature from the top to the bottom of the PCB. The connections from the package ground leads to ground are kept as short as possible.

POWER SUPPLY INPUTS

The ADRF5515A-EVALZ has five power supply inputs and two grounds, as shown in Table 1. The dc test points are populated only on the SWVDDB, VDD1_A, and VDD1_B test points, whereas the VDD2_A and VDD2_B points are shorted to VDD1_A and VDD1_B, respectively, via 0 Ω resistors. A single 5 V supply is connected to the dc test points on the SWVDDB, VDD1_A, and VDD1_B test points. Ground reference can be connected to the GND or GND1 test point. The typical total current consumption for the ADRF5515A is 190 mA in receive operation, high gain mode.

Each supply pin for the LNAs of the ADRF5515A-EVALZ is decoupled with 1 nF and 10 µF capacitors. A 10 µF capacitor is used on the supply line for the switches of the ADRF5515A-EVALZ.

Table 1. Test Points for Power Supply Inputs

Test Points	Description
VDD1_A	Supply LNA Stage 1 on Channel A
VDD2_A	Supply LNA Stage 2 on Channel A, do not insert (DNI)
VDD1_B	Supply LNA Stage 1 on Channel B
VDD2_B	Supply LNA Stage 2 on Channel B, DNI
SWVDDB	Supply switches on Channel A and Channel B
GND	Ground
GND1	Ground

The ADRF5515A-EVALZ also has edge mounted Subminiature Version A (SMA) connectors for power supply inputs, as shown in Table 2. These SMA connectors are not populated by default and can be connected by the user.

Table 2. SMA Connectors for Power Supply Inputs

SMA Connectors	Description
VDD_A	Supply LNA on Channel A
VDD_B	Supply LNA on Channel B
SWVDDB	Supply switches on Channel A and Channel B

EVALUATION BOARD HARDWARE

CONTROL INPUTS

The ADRF5515A-EVALZ has four control inputs, as described in Table 3. Each control input is decoupled with a 100 pF capacitor. When no connection is made to the control inputs, both channels are in termination mode with LNAs operating in high gain mode. Populating the 1 kΩ pull down resistors on the SWCTRL, BP_A, BP_B, and PD test points result in the ADRF5515A turning on in receive high gain mode.

Table 3. Control Inputs

Test Points	Description
BP_A	Bypass LNA Stage 2 on Channel A
BP_B	Bypass LNA Stage 2 on Channel B
PD	Power down all LNA stages on Channel A and Channel B
SWCTRL	Control switches on Channel A and Channel B

RF INPUTS AND OUTPUTS

The ADRF5515A-EVALZ has ten edge mounted SMA connectors for the RF inputs and outputs, as shown in Table 4. ANT_A and ANT_B, and TERM_A and TERM_B, are dc-coupled, whereas the RXO_x is ac-coupled using a series capacitor of 10 pF close to the SMA connector.

The SMA connectors and series components on the thru lines are not populated by default and can be connected by the user to measure and calibrate out the evaluation board loss effects. To measure and calibrate out the evaluation board loss effects, the user must connect these connectors and components. Use the thru line on THRU1 and THRU2 to calibrate out the ANT_A or ANT_B to TERM_A or TERM_B evaluation board loss. Use the thru line on THRU3 and THRU4, which have 10 pF capacitors, to calibrate out the RXO_A or RXO_B evaluation board loss.

Table 4. RF Inputs and Outputs

SMA Connectors	Description
ANT_A	Antenna input to Channel A
ANT_B	Antenna input to Channel B
TERM_A	Termination output from Channel A
TERM_B	Termination output from Channel B
RXO_A	Receiver output from Channel A
RXO_B	Receiver output from Channel B
THRU1	Thru line input or output, DNI
THRU2	Thru line input or output, DNI
THRU3	Thru line input or output, DNI
THRU4	Thru line input or output, DNI

TEST PROCEDURE

BIASING SEQUENCE

To bias up the ADRF5515A-EVALZ, perform the following steps:

1. Ground the GND or GND1 test point.
2. Bias up VDD1_A, VDD2_A, and SWVDDB test points.
3. Bias up the SWCTRL test point.
4. Bias up the PD test point.
5. Bias up the BP_A and BP_B test points.
6. Apply an RF input signal.

The ADRF5515A-EVALZ is shipped fully assembled and tested. Figure 3 provides a basic test setup diagram to evaluate the s-parameters (receive gain, transmit insertion loss and isolation, RF input and output return losses) using a network analyzer. Perform the following steps to complete the test setup and verify the operation of the ADRF5515A-EVALZ:

1. Connect the GND or GND1 test point to the ground terminal of the power supply.
2. Connect the VDD1_A, VDD2_A, and SWVDDB test points to the voltage output terminal of the 5 V supply that sources a current of approximately 190 mA in receive operation for high gain mode or 26 mA for power-down mode.
3. Connect the BP_A, BP_B, PD, and SWCTRL test points to the ground terminal of the power supply for high gain receive operation. The ADRF5515A-EVALZ can be configured in different modes by connecting the control test points to 5 V or ground, as shown in Table 5 and Table 6.
4. Connect a calibrated network analyzer to the ANT_A, TERM_A, and RXO_A SMA connectors. Sweep frequency from 1 GHz to 6 GHz and set power to −25 dBm.
5. Connect 50 Ω loads to the ANT_B, TERM_B, and RXO_B SMA connectors.
6. The ADRF5515A-EVALZ is expected to have a high and low receive gain of 36 dB and 17 dB, respectively, at 3.6 GHz. See the expected results in Figure 4 to Figure 7.

Table 5. Truth Table Switch Control

SWCTRL	Signal Path
Low	Receive operation
High	Transmit operation

Table 6. Truth Table Receive Operation

PD	BP_A, BP_B	Receive Operation
Low	Low	High gain mode
Low	High	Low gain mode
High	Low	Power-down, high isolation mode
High	High	Power-down, low isolation mode

Additional test equipment is needed to fully evaluate the device functions and performance.

For noise figure evaluation, use either a noise figure analyzer or a spectrum analyzer with noise option. The use of a low excess noise ratio (ENR) noise source is recommended.

For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is recommended.

For power compression and power handling evaluations, use a two-channel power meter and a signal generator. A power amplifier with great enough power is recommended at the input. Test accessories such as couplers and attenuators must have enough power handling.

The ADRF5515A-EVALZ comes with a support plate attached to the bottom side. To ensure maximum heat dissipation and to reduce thermal rise on the ADRF5515A-EVALZ during high power evaluations, this support plate must be attached to a heat sink using thermal grease.

Note that the measurements performed at the SMA connectors of the ADRF5515A-EVALZ include the losses of the SMA connectors and the PCB. The thru line must be measured to calibrate out the ADRF5515A-EVALZ effects. The thru line is the summation of an RF input line and an RF output line that are connected to the device and equal in length.

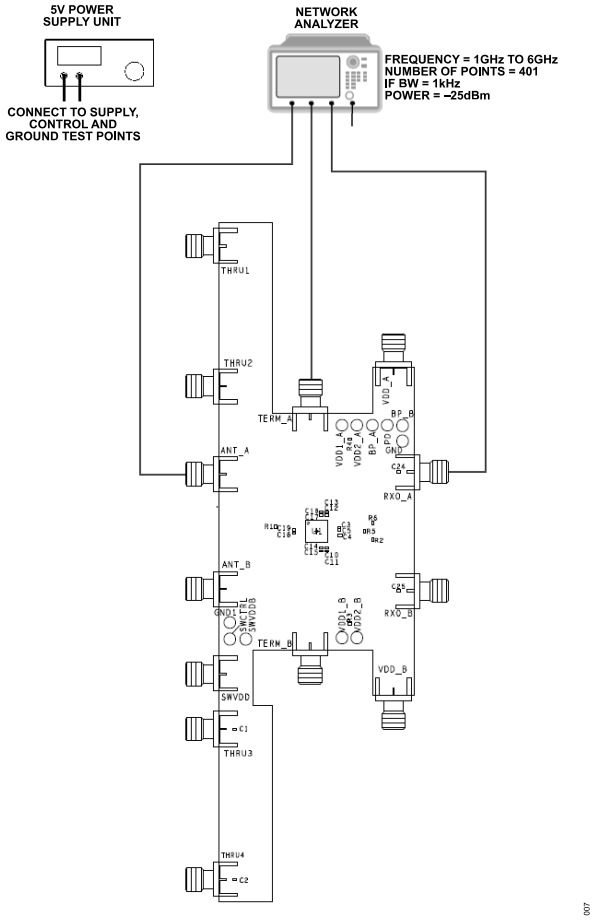

Figure 3. Test Setup Diagram

TEST PROCEDURE

EXPECTED RESULTS

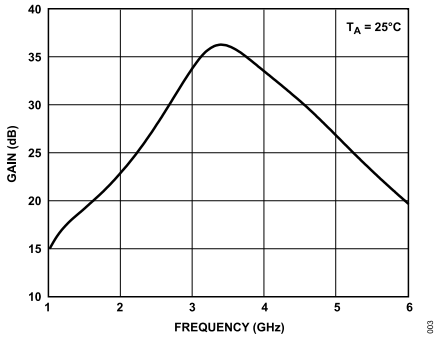

Figure 4. Receive Operation, High Gain

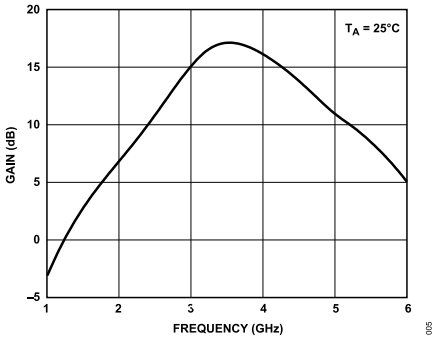

Figure 6. Receive Operation, Low Gain

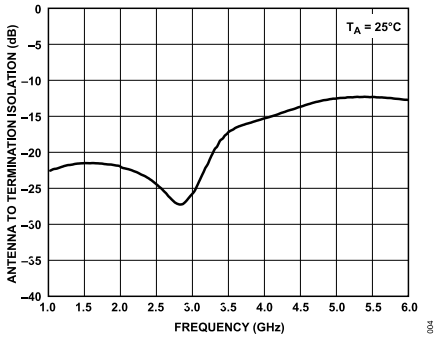

Figure 5. Receive Operation, Antenna to Termination Isolation

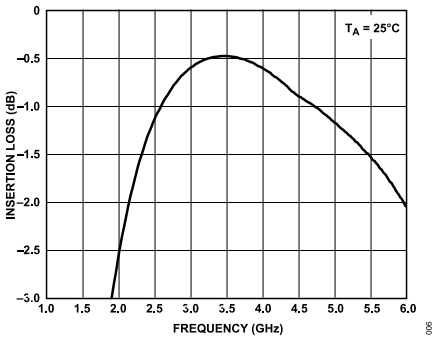

Figure 7. Transmit Operation, Antenna to Termination Insertion Loss

EVALUATION BOARD ARTWORK AND SCHEMATIC

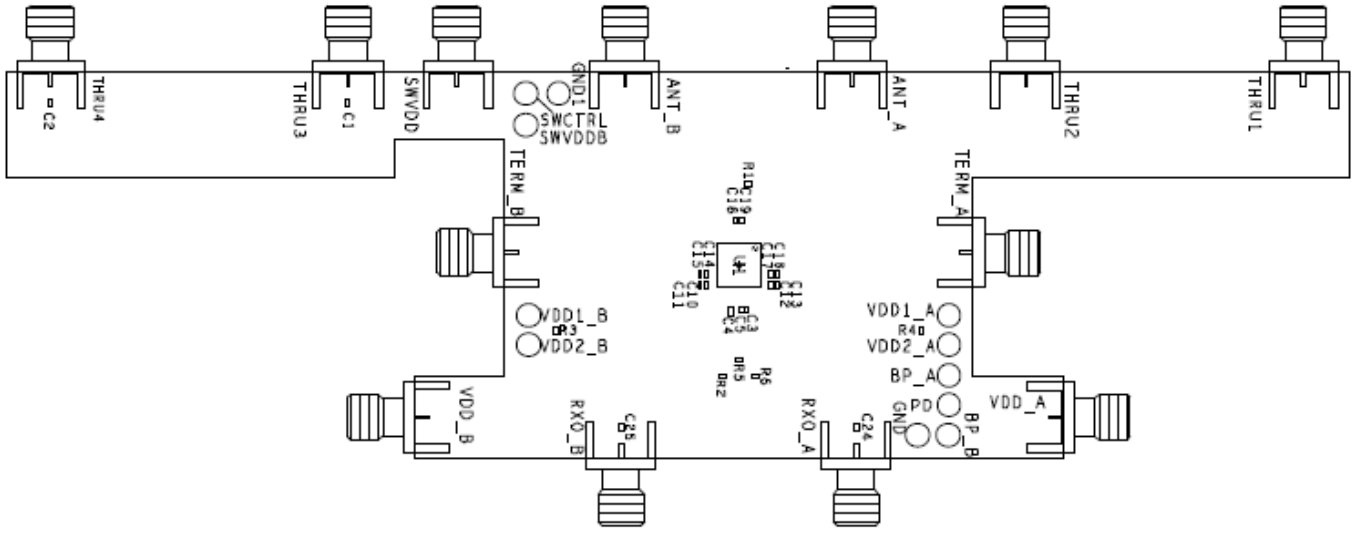

Figure 8. ADRF5515A-EVALZ Assembly Diagram

EVALUATION BOARD ARTWORK AND SCHEMATIC

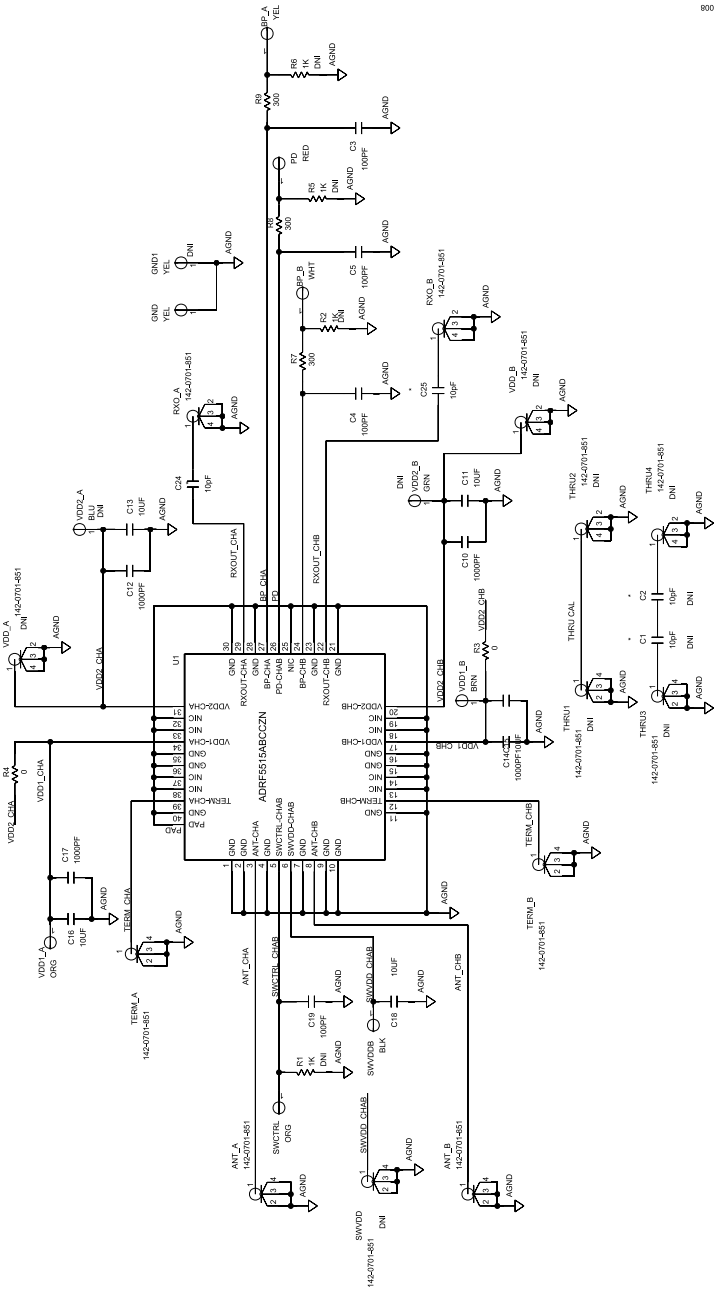

Figure 9. ADRF5515A-EVALZ Schematic

ORDERING INFORMATION

BILL OF MATERIALS

Table 7. Bill of Materials for the ADRF5515A-EVALZ

Reference Designator	Description	Manufacturer	Part Number
ANT_A, ANT_B, RXO_A, RXO_B, TERM_A, TERM_B	PCB mount SMA connectors	Johnson/Cinch Connectivity Solutions	142-0701-851
C3, C4, C5	100 pF capacitors, 50 V, 0402 package	Murata Electronics	GCM1555C1H101JA16D
C19	100 pF capacitors, 200 V, 0402 package	KEMET	C0402C101J2GACTU
C24, C25	10pF capacitor, 200V, 0402 package	American Technical Ceramics	ATC600L100JT200T
C10, C12, C14, C17	1000 pF capacitors, 25 V, 0402 package	TDK	CGJ2B2X7R1E102K050BA
C11, C13, C15, C16, C18	10 µF capacitors, 10 V, 0402 package	Samsung Electro-Mechanics	CL05A106MP5NUNC
R3, R4	0 Ω resistors, 0402 package	Panasonic Electronic Components	ERJ-2GE0R00X
R7, R8, R9	300 Ω resistors, 0402 package	Panasonic Electronic Components	ERJ-2GEJ301X
U1	Integrated dual-channel, 3.3 GHz to 4.0 GHz, 20 W receiver front end	Analog Devices, Inc.	ADRF5515A
PCB	Printed circuit board	Analog Devices	08-057286C

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.