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Devices Connected/Referenced	
AD9142A	Dual 16-bit, 1.6 GSPS TxDAC+® Digital-to-Analog Converter
ADRF6720	Wideband Quadrature Modulator with Integrated Fractional-N PLL and VCOs
ADL5320	400 MHz to 2700 MHz, ¼ Watt, RF Driver Amplifier

Broadband Low Distortion Transmitter for 3G, 4G, and LTE Communication System

EVALUATION AND DESIGN SUPPORT

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a broadband low distortion RF transmitter with a dual high speed TxDAC+ digital-to-analog converter (DAC), a wideband I/Q modulator, and an output driver amplifier.

The devices are well matched, and the direct interface between the DAC and the modulator, and between the modulator and the driver amplifier, offers a compact solution for many RF communications applications including 3G, 4G, and LTE.

CIRCUIT DESCRIPTION

The RF transmitter shown in Figure 1 and Figure 2 utilizes the AD9142A TxDAC, the ADRF6720 phase locked loop (PLL)/voltage controlled oscillator (VCO) integrated wideband I/Q modulator, and the ADL5320 ¼ W driver amplifier.

Signal biasing and scaling in the DAC-to-modulator interface circuit is controlled by the four ground referenced resistors (R_{BI+}, R_{BI-}, R_{BQ+}, and R_{BQ-}) and the two shunt resistors (R_{LI} and R_{LQ}), respectively. The input and output matching on the ADL5320 driver amplifier is implemented using shunt capacitors at the input and the output. The required matching components and placement are shown in the ADL5320 data sheet.

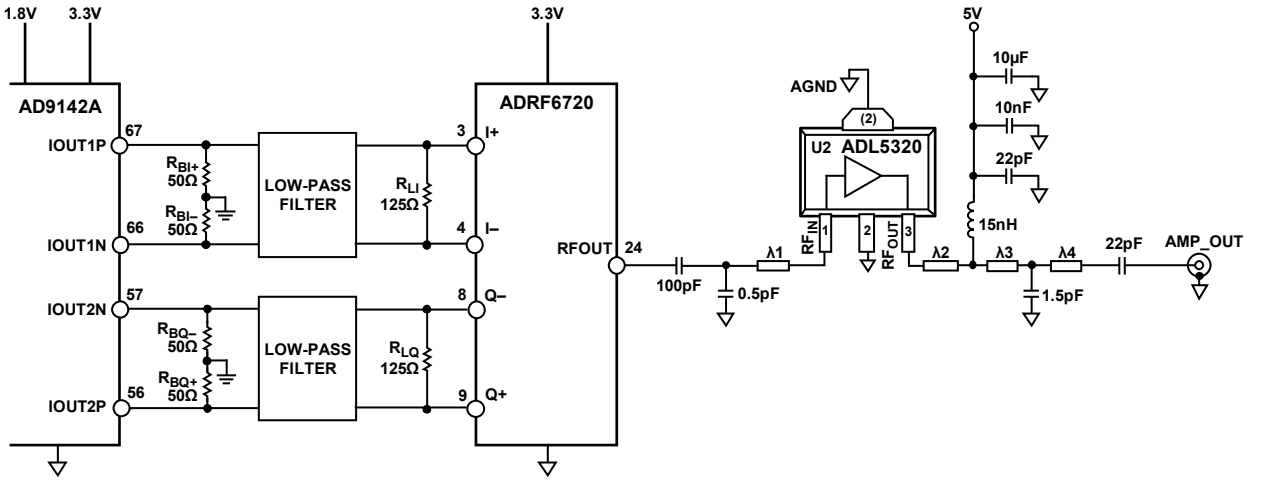

Figure 1. Simplified Circuit Schematic for I/Q Modulator with DAC and Driver Amplifier (All Connections and Decoupling Not Shown)

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

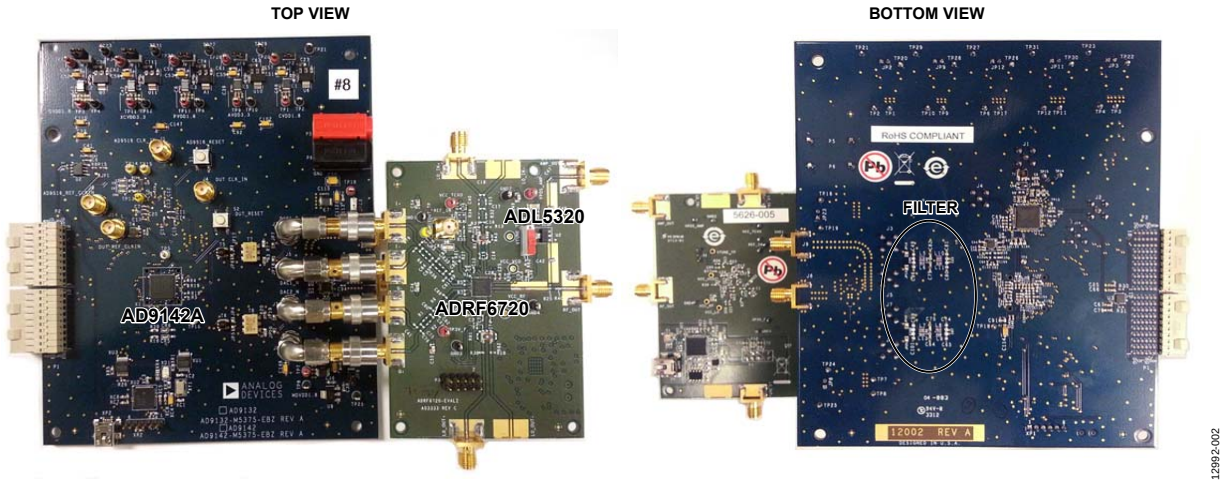

Figure 2. Modified AD9142A Evaluation Board and ADRF6720 Evaluation Board for Circuit Implementation

The nominal and default value of the AD9142A full-scale output current is 20 mA. This current generates the 500 mV dc bias level and a full-scale output voltage swing of 2 V p-p differential on each DAC output pair with the four ground referenced 50 Ω resistors ($R_{BI+} = R_{BI-} = R_{BQ+} = R_{BQ-}$). The 2 V p-p voltage swing can be adjusted by the R_L shunt resistors ($R_L = R_{LI} = R_{LQ}$), which are in parallel with the 500 Ω I/Q input impedance of the ADRF6720 modulator. The 500 mV dc bias level is not affected by this adjustment. For example, with a 100 Ω effective differential load, each single-ended output swings between 250 mV and 750 mV but still maintains an average value of 500 mV.

Figure 3 shows the resulting peak-to-peak differential swing as a function of the R_L swing limiting resistor and the 500 Ω parallel differential input impedance.

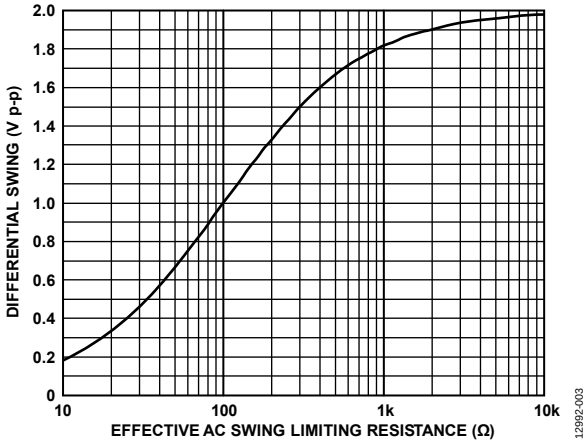

Figure 3. Relationship Between the Effective AC Swing Limiting Resistance and the Peak-to-Peak Voltage Swing with 50 Ω Bias Setting Resistors

I/Q Filtering

An antialiasing filter between the DAC and the modulator is necessary to filter out Nyquist images, common-mode noise, and broadband DAC noise. The filter is placed between the dc bias setting resistors and the ac swing-limiting resistor.

The dc bias-setting resistors set the filter source impedance, and the ac swing limiting resistor in parallel with the ADRF6720 500 Ω input impedance sets the filter load impedance.

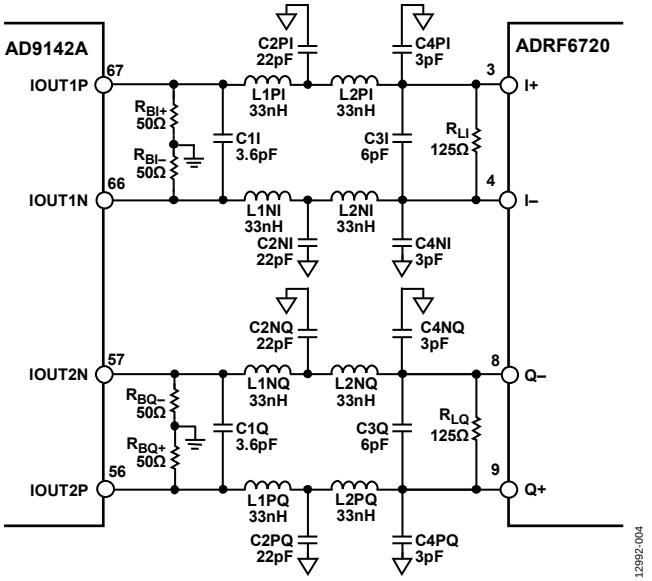

Figure 4. Recommended DAC Modulator Interface Topology with f_C = 300 MHz, Fifth-Order, Butterworth Filter

System Level Simulation

Figure 5 shows the simulated cascaded performance of the DAC, the I/Q modulator and the driver amplifier at 2140 MHz. The AD9142A, ADRF6720, and ADL5320 are well matched in terms of dynamic range and gain. Figure 5 shows 39.4 dBm for composite output third-order intercept (OIP3) and approximately −76 dBc adjacent channel leakage ratio (ACLR) performance. The simulation was done using the ADIsimRF Design Tool.

The linearity of the ADRF6720 can be optimized through the MOD_RSEL (Register 0x31, Bits[12:6]) and MOD_CSEL (Register 0x31, Bits[5:0]) settings. These settings control the amount of antiphase distortion to the baseband input stages to correct for distortion.

Figure 6 through Figure 11 show the measured plots of the output second-order intercept (OIP2) and OIP3 optimization at zero IF, 100 MHz, and 200 MHz complex IF by varying the settings of the MOD_RSEL register and the MOD_CSEL register in the ADRF6720.

Figure 6, Figure 7, and Figure 8 show optimized OIP3 performance every 32 steps on the MOD_RSEL axis; OIP3 performance does not vary significantly as a function of MOD_CSEL at zero IF. However, there is more sensitivity to MOD_CSEL at the higher IF frequencies.

Through MOD_RSEL and MOD_CSEL optimization, OIP3 is approximately 42 dBm at zero IF, 45 dBm at 100 MHz IF, and 48 dBm at 200 MHz IF.

The RSEL and CSEL adjustment do not impact OIP2 performance significantly; however, there is some degradation at high IF frequencies.

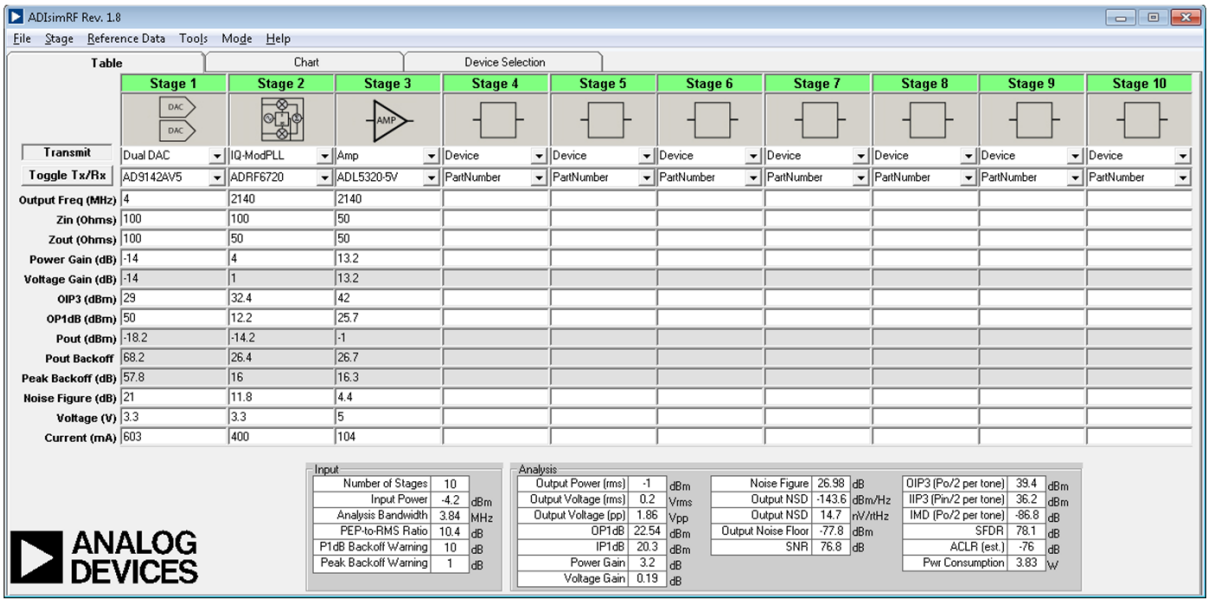

Figure 5. ADIsimRF Design Tool Screenshot Showing Cascaded Performance of the AD9142A, ADRF6720, and ADL5320

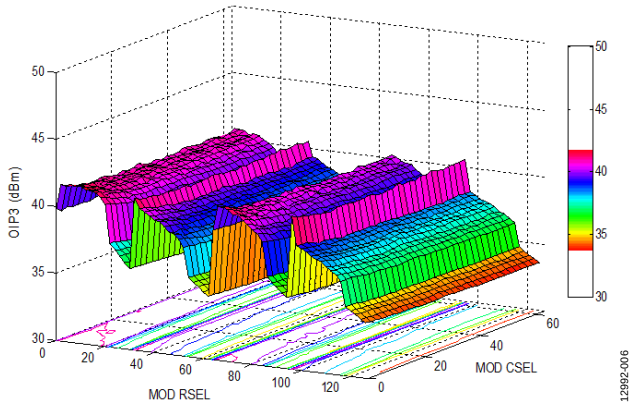

Figure 6. OIP3 vs. MOD_CSEL and MOD_RSEL at f_{RF} = 2140 MHz, Zero IF, Output Power of ADL5320 = 11 dBm

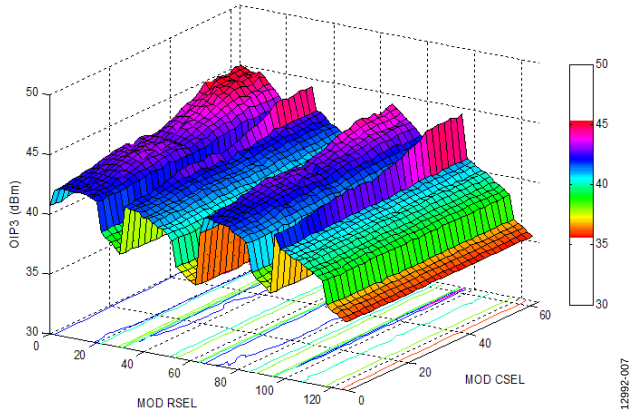

Figure 7. OIP3 vs. MOD_CSEL and MOD_RSEL at f_{RF} = 2140 MHz, 100 MHz IF, 2340 MHz LO, Output Power of ADL5320 = 11 dBm

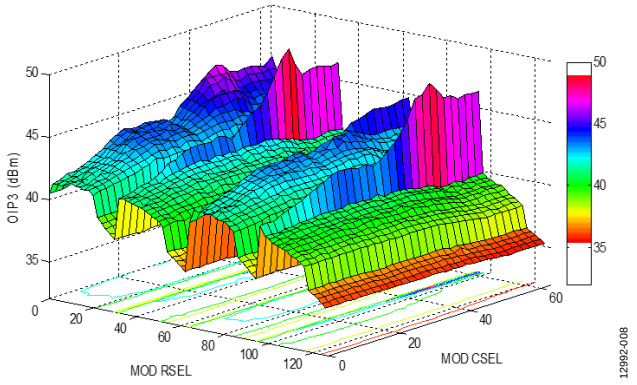

Figure 8. OIP3 vs. MOD_CSEL and MOD_RSEL at f_{RF} = 2140 MHz, 200 MHz IF, 2340 MHz LO, Output Power of ADL5320 = 11 dBm

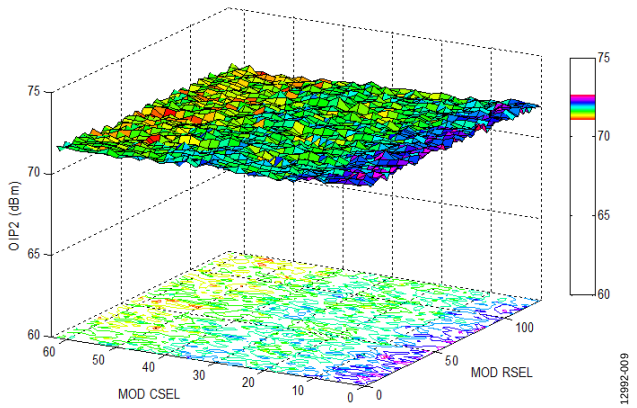

Figure 9. OIP2 vs. MOD_CSEL and MOD_RSEL at f_{RF} = 2140 MHz, Zero IF, Output Power of ADL5320 = 11 dBm

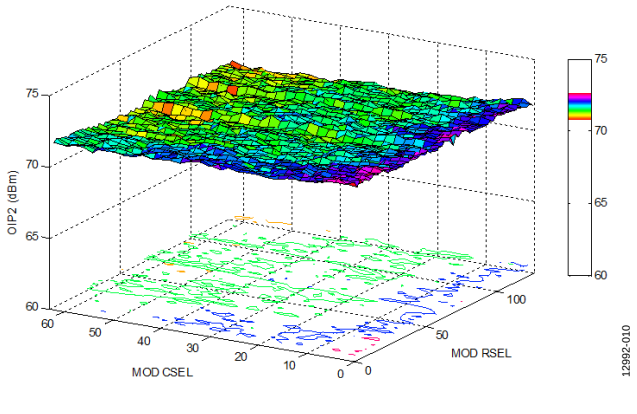

Figure 10. OIP2 vs. MOD_CSEL and MOD_RSEL at f_{RF} = 2140 MHz, 100 MHz IF, 2340 MHz LO, Output Power of ADL5320 = 11 dBm

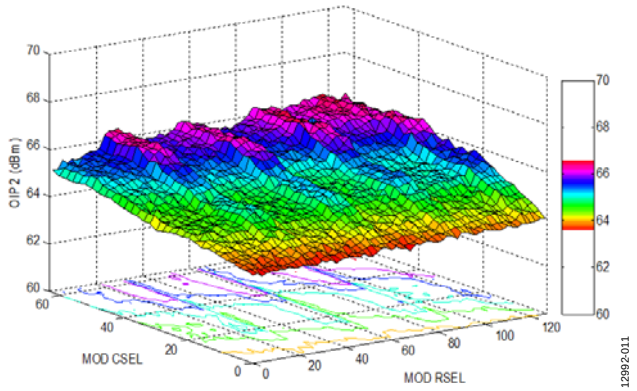

Figure 11. OIP2 vs. MOD_CSEL and MOD_RSEL at f_{RF} = 2140 MHz, 200 MHz IF, 2340 MHz LO, Output Power of ADL5320 = 11 dBm

Choosing an Output Power Level

While the circuit can achieve output power levels up to 12 dBm, operation at that level is not practical, especially with modulated carriers with high peak-to-average ratios. To achieve an acceptable level of distortion, significant backoff is required. Adjacent channel power ratio (ACPR) has become a popular metric for assessing the system level distortion.

Figure 12 and Figure 13 show the measured ACPR vs. output power at the ADL5320 output for three IF cases in single carrier WCDMA (Test Model 1-64) and LTE (Test Model 1_1 64QAM) cases, respectively. The system achieves an ACPR of approximately −75 dB to −80 dB at the −2 dBm to +6 dBm output power range. In the case of an LTE signal, ACPR is defined as the ratio of the power in the carrier (in a bandwidth of 4.515 MHz) to the power in an adjacent channel (channel spacing = 5 MHz), also measured in a 4.515 MHz bandwidth.

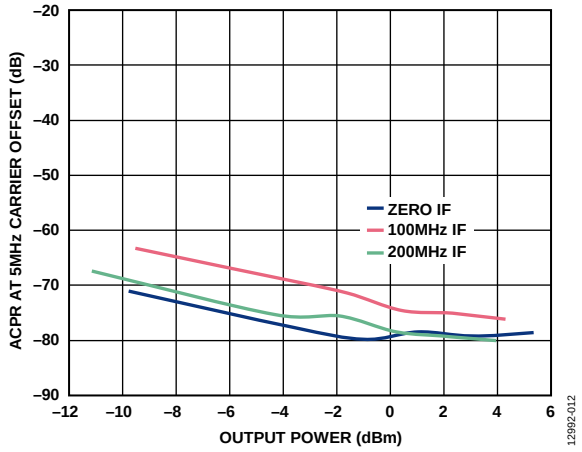

Figure 12. ACLR vs. Output Power at ADL5320 Amplifier Output, Zero IF, Optimized RSEL and CSEL on ADRF6720 at 2140 MHz, 1C WCDMA TM1-64

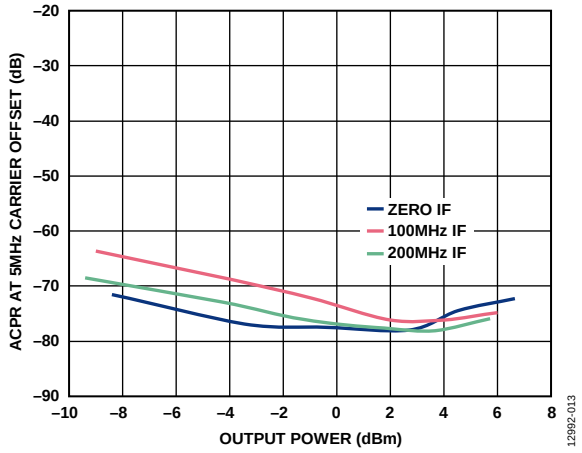

Figure 13. ACLR vs. Output Power at ADL5320 Amplifier Output, OIP3 Optimized RSEL and CSEL on ADRF6720, 1C LTE TM1_1 64QAM

OIP2 and OIP3 can be improved by the MOD_RSEL and MOD_CSEL adjustment shown in the previous section, and accordingly, the ACPR improvement is shown in Figure 13 and Figure 14. The improvement is more noticeable at high output power levels.

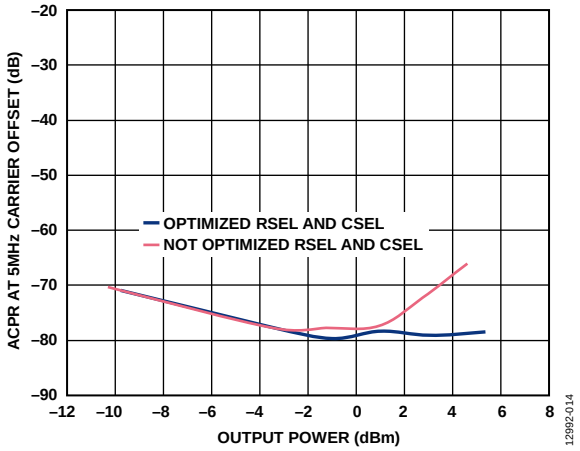

Figure 14. ACLR vs. Output Power at ADL5320 Amplifier Output, Zero IF, Optimized and Not Optimized RSEL and CSEL on ADRF6720 at 2140 MHz, 1C WCDMA TM1-64

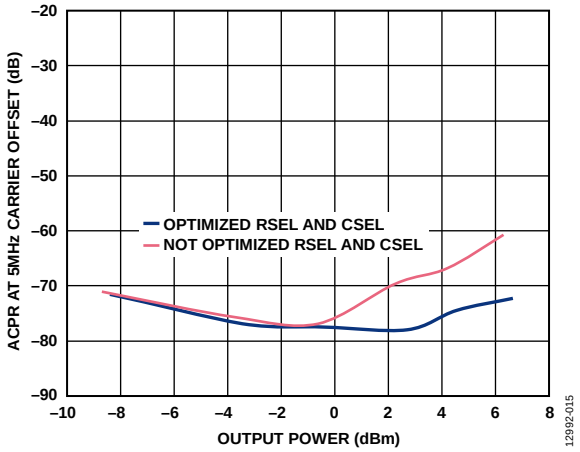

Figure 15. ACLR vs. Output Power at ADL5320 Amplifier Output, Zero IF, Optimized and Not Optimized RSEL and CSEL on ADRF6720 at 2140 MHz, 1C LTE TM1_1 64QAM

The spectrum plots of the single WCDMA and LTE at 2140 MHz are shown in Figure 16 and Figure 17, respectively.

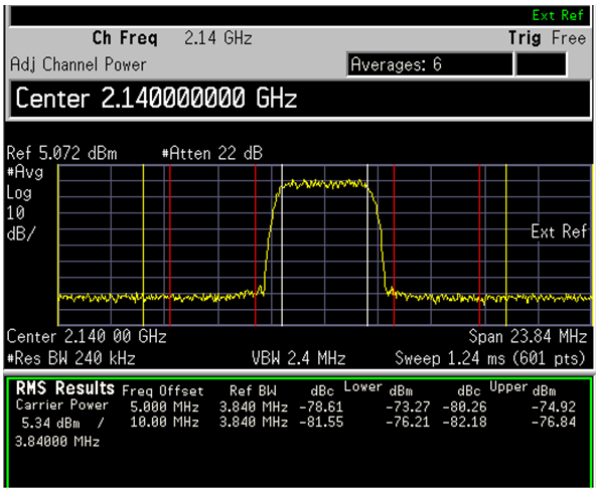

Figure 16. Adjacent Channel Power Performance at ADL5320 Amplifier Output, Zero IF, Optimized RSEL and CSEL on ADRF6720 at 2140 MHz, 1C WCDMA TM1-64

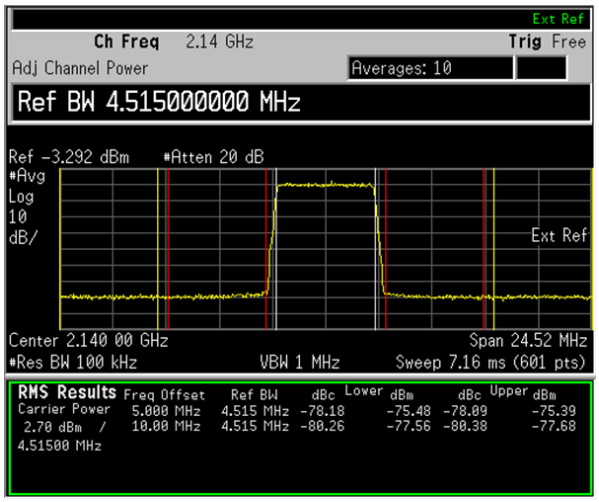

Figure 17. Adjacent Channel Power Performance at ADL5320 Amplifier Output, Zero IF, Optimized RSEL and CSEL on ADRF6720 at 2140 MHz, 1C LTE TM1_1 64QAM

PCB Layout Recommendations

Take special care in the layout of the DAC/modulator/amplifier interface. The following are recommendations for PCB layout:

- Keep all I/Q differential trace lengths well matched.
- Place the filter termination resistors as close as possible to the modulator input.
- Place the DAC output 50 Ω resistors as close as possible to the DAC.
- Use thick trace widths through the filter network to reduce signal loss.
- Place vias around all DAC output traces, filter networks, modulator output traces, LO input traces, amplifier input traces, and amplifier output traces.
- Route LO and modulator outputs on different layers or at 90° angles to each other to prevent coupling.

COMMON VARIATIONS

The DAC and modulator interface described in this circuit note can be used between any TxDAC digital-to-analog converter that is set for 20 mA full-scale current and the I/Q modulators that require 0.5 V baseband dc bias levels. Examples of TxDACs include the AD9779A, AD9788, AD9125, AD9144, and AD9148. I/Q modulators include the ADL5370/ADL5371/ADL5372/ADL5373/ADL5374/ADL5385/ADL5386, and the ADRF6701/ADRF6702/ADRF6703/ADRF6704 PLL/VCO integrated families.

For operation at higher power, the ADL5324 ½ W driver amplifier is recommended. The ADL5320 and ADL5324 must be tuned to the frequency at which they will be operating. The data sheets of both devices contain tables that provide recommended values for tuning components at popular operating frequencies.

CIRCUIT EVALUATION AND TEST

Equipment Needed

The following equipment is needed. Equivalents can be substituted.

- AD9142A evaluation board (AD9142-M5375-EBZ) modified with SMA connectors added to allow direct connection to TxDAC current outputs.
- ADRF6720 evaluation board (ADRF6720-EVALZ)
- Analog Devices, Inc., Digital Pattern Generator (DPG)
- Signal generator for clock (R&S SMIQ 03B)
- Signal generator for reference input of ADRF6720 (R&S SMIQ 03B)
- Spectrum analyzer (Agilent E4440A)
- Power supply (Agilent E3631A, two needed)

Setup and Test

1. Connect the set up and measurement system as shown in Figure 18.
2. Set the power supply to 5 V for the AD9142A evaluation board.
3. Set the power supply to 3.3 V for the ADRF6720.evaluation board.
4. Set the power supply to 5 V for the ADL5320 on the ADRF6720 evaluation board.
5. Set the signal generator for the clock to 1.5 GHz at 5 dBm, and set the signal generator for the ADRF6720 reference input to 153.6 MHz at 4 dBm.
6. Turn on the power supply and the signal generators. Set the spectrum analyzer at 2140 MHz.
7. Set up the AD9142A through the USB using the AD9142A SPI control software, as shown in Figure 19, and run. See the AD9142A Evaluation Board Quick Start Guide.
8. Set up the DPG, as shown in Figure 20, and run. See the AD9142A Evaluation Board Quick Start Guide.
9. Set up the ADRF6720, as shown in Figure 21, and run. See the ADRF6720-EVALZ User Guide (UG-689).

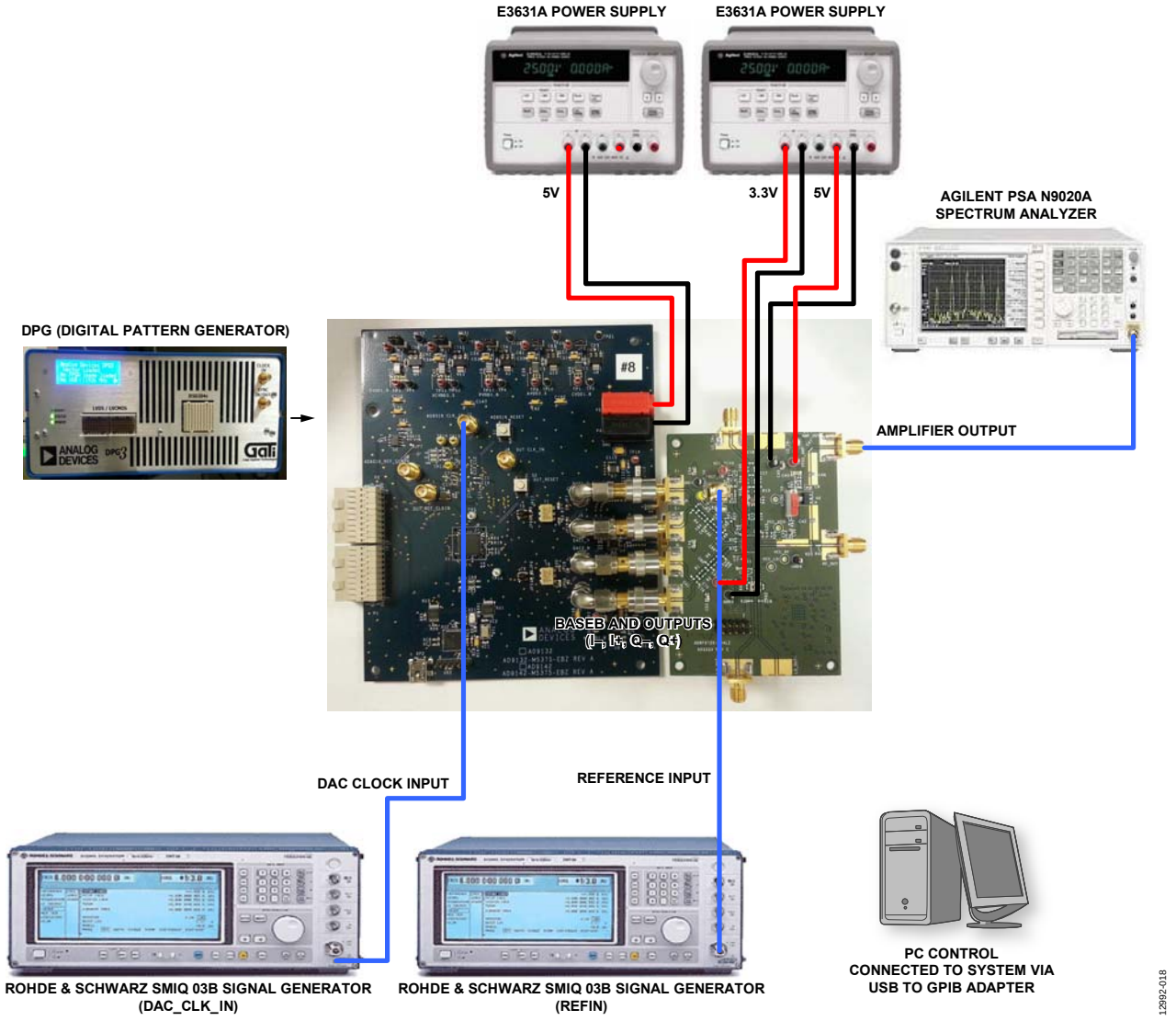

Figure 18. Test Setup

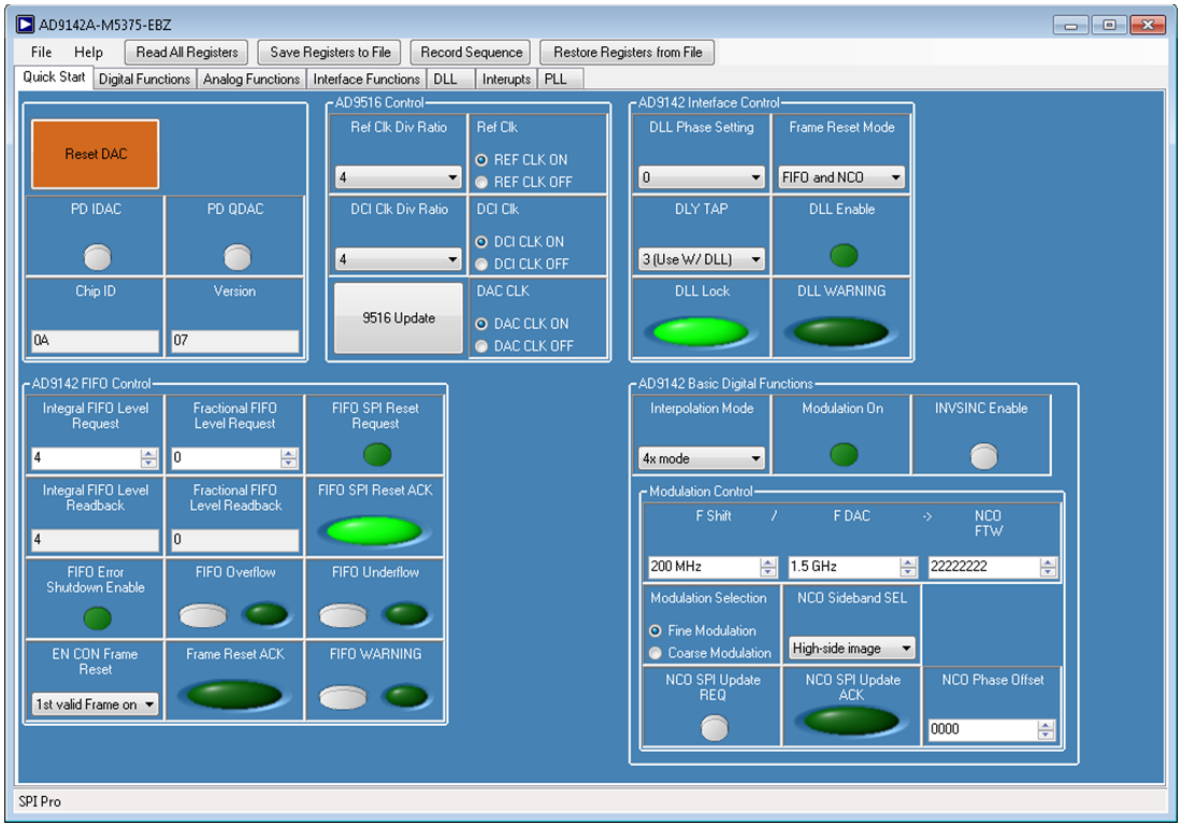

Figure 19. SPI Control User Interface Setup for AD9142A

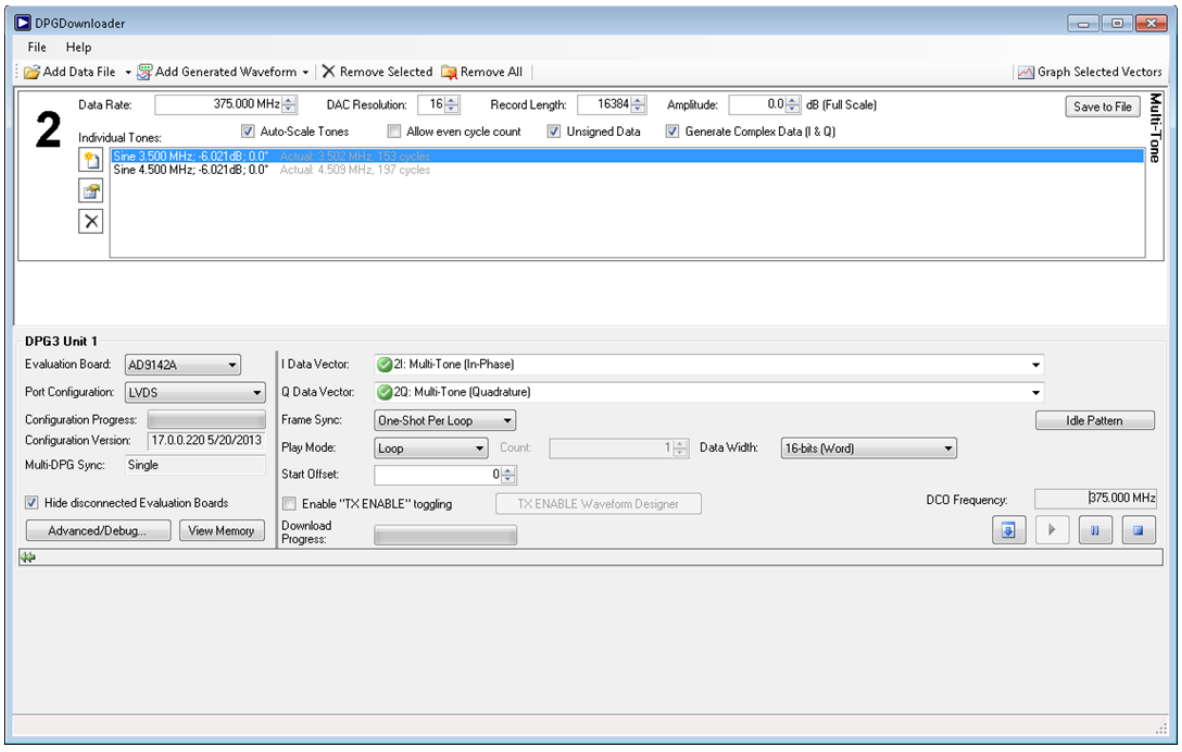

Figure 20. Setting Up the DPG Using the DPG Downloader Software

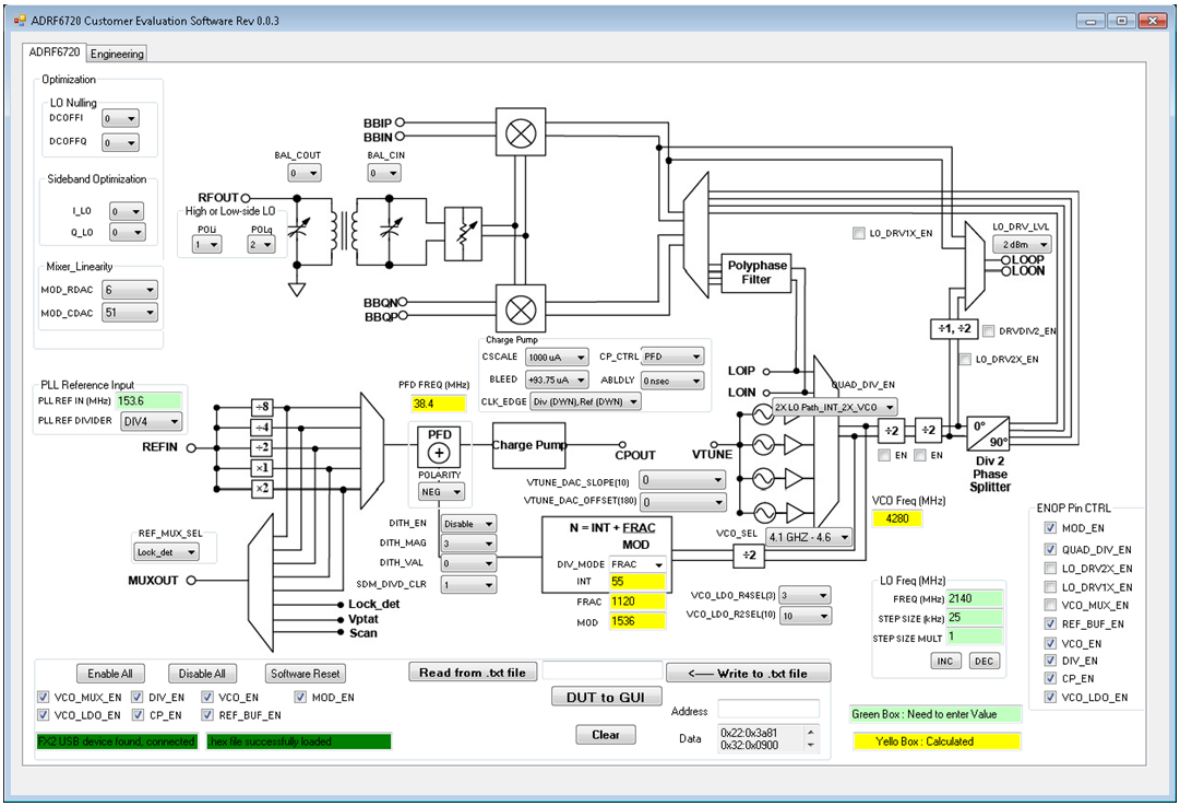

Figure 21. Setting Up the ADRF6720 Using the ADRF6720 Control Software

LEARN MORE

CN-0375 Design Support Package:
www.analog.com/CN0375-DesignSupport

Circuit Note CN-0016. *Interfacing the ADL5370 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC.* Analog Devices.

Circuit Note CN-0017. *Interfacing the ADL5371 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC.* Analog Devices.

Circuit Note CN-0018. *Interfacing the ADL5372 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC.* Analog Devices.

Circuit Note CN-0019. *Interfacing the ADL5373 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC.* Analog Devices.

Circuit Note CN-0020. *Interfacing the ADL5374 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC.* Analog Devices.

Circuit Note CN-0021. *Interfacing the ADL5375 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC.* Analog Devices.

Circuit Note CN-0134. *Broadband Low Error Vector Magnitude (EVM) Direct Conversion Transmitter.* Analog Devices.

Circuit Note CN-0144. *Broadband Low Error Vector Magnitude (EVM) Direct Conversion Transmitter Using LO Divide-by-2 Modulator*. Analog Devices.

Circuit Note CN-0205. *Interfacing the ADL5375 I/Q Modulator to the AD9122 Dual Channel, 1.2 GSPS High Speed DAC.* Analog Devices.

Circuit Note CN-0243. *High Dynamic Range RF Transmitter Signal Chain using Single External Frequency Reference for DAC Sample Clock and IQ Modulator LO Generation.* Analog Devices.

Nash, Eamon. AN-1039 Application Note. *Correcting Imperfections in IQ Modulators to Improve RF Signal Fidelity.* Analog Devices.

Zhang, Yi. AN-1100 Application Note. *Wireless Transmitter I/Q Balance and Sideband Suppression.* Analog Devices.

AN-1237 Application Note. *Precise Control of I/Q Modulator Output Power Using the ADL5386 Quadrature Modulator and the AD5621 12-Bit DAC.* Analog Devices.

ADIsimPLL Design Tool

ADIsimRF Design Tool

UG-689, ADRF6720-EVALZ User Guide

AD9142A Evaluation Board Quick Start User Guide

Analog Devices Data Pattern Generator (DPG)

Data Sheets and Evaluation Boards

AD9142A Data Sheet

ADRF6720 Data Sheet

AD9142-M-5375-EBZ Evaluation Board

ADRF6720-EVALZ Evaluation Board

REVISION HISTORY

1/15—Revision 0: Initial Version