Technical Notes on using Analog Devices' DSP components and development tools
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Recommended Handling of Unused SHARC Pins

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SHARC Bits

Introduction

The ADSP-2106x (SHARC) processors contain 240 pins. Several of these pins are only necessary for specific functions, such as the Serial Port Signals. If an application does not make use of a function the associated signals (pins) may still require a connection rather than be left floating (unconnected). The following application note suggests recommended methods of handling the pins associated with unused functions.

The application note is broken down into sections based on the SHARCs functions. Within each section will be a list of each pin associated with the particular section, and the recommended handling of the unused pin.

Link Ports

$LxDAT_{3-0}$, LxCLK, LxACK: The link port data, clock and acknowledge lines all contain internal pull-up resistors, therefore they can be left floating if unused.

Serial Ports

DTx_{3-0}, DRx, TCLKx, RCLKx: The serial port transmit receive data, transmit clock and receive clock lines all contain internal pull-up resistors, therefore they can be left floating if unused.

TFSx, RFSx: The transmit frame sync and receive frame sync lines should be pulled or tied high if unused. Pulling or tying frame sync signals high will prevent unwanted power consumption if the serial ports are inadvertently enabled.

External Interface

$ADDR_{31-0}$, $DATA_{47-0}$: The address and data and select lines can be left floating if unused.

MS_{3-0} , PAGE, ADRCLK, REDY: The memory select, page, address clock and redy lines can be left floating because they are outputs.

RD, WR, SW: In the unusual case no host is driving read or write and the SHARC is not bus master the read and write lines should be pulled high. If the SHARC is the bus master the read and write lines can be left floating. (The master drives the read and write lines.) (SW adheres to the same rules as RD and WR).

ACK: If the acknowledge signal will not be used, leave ACK floating.

HBR, CS: If there is no host processor, host bus request and chip select should be pulled or tied high.

HBG: In the unusual case the SHARC has an id greater than 1 and there is no bus master, the host bus grant line should be pulled high. If id is 1 or less and there will be no arbitration for he bus, host bus grant can be left floating.

BR_{6-1}: In a multiprocessor system pull the unused Bus Request pins high (the processor drives its own BRx line). If id=000 leave bus request pins floating.

DMA Requests

DMAR1, DMAR2: If DMA request 1 and DMA request 2 will not be used pull the pins high. Pulling them high will prevent them from floating to a low logic level and interfering with DMA channels 7 and 8.

DMAG1, DMAG2: DMAG1 and DMAG2 are outputs and can be left floating if unused.

Interrupt Requests, Flags and Timer Expired

$FLAG_{3-0}$: The flag pins can be left floating if unused.

IRQ_{2-0}: If the interrupt request lines are unused they should be pulled or tied high.

TIMEXP: Timer expired is an output and can be left floating if unused.

JTAG

TRST: The test reset pin must be asserted (pulsed) low after power up. If the JTAG emulator will not be used, the test reset pin must be tied low.

TCK: The test clock should be pulled or tied either high or low if the JTAG emulator will not be used.

TMS, TDI: The test mode select and test data input pins can be left floating if the JTAG emulation is not used. These pins have internal pull-up resistors.

TDO, EMU: The test data output and emulation status pins can be left floating if JTAG emulation is unused. These signals are output only.

Miscellaneous

SBTS: The suspend bus three state should be tied high if no other device will be connected and the pin is not used.

CPA: The core priority access pin can be left floating if unused. The CPA is pulled high with an internal pull-up resistor.

BMS: If EPROM boot select (EBOOT) is deserted, i.e. EPROM boot is not selected, boot memory select must be tied low of high. If EPROM is asserted BMS is an output.

ICSA, NC: These pins are reserved and should always be left unconnected.

The remaining pins, which will be listed for completeness, are associated with functionality that *must* be used. The pins either configure a mode, supply vdd or gnd, clock or reset. Please refer to the ADSP-2106x SHARC User's Manual or the ADSP-2106x Data Sheet for the proper connection of the following pins: **ID_{2-0}, RPBA, EBOOT, LBOOT, CLKIN, RESET, VDD** and **GND**.