

# ADSP-21065L SHARC DSP

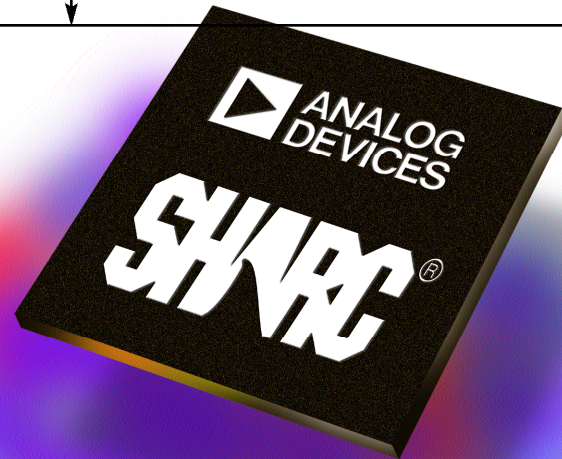
## 32-Bit Floating-Point Performance

### Key Features

- Up to 198 MFLOPS (32-bit floating-point)
- Up to 198 MOPS (32-bit fixed-point)
- 16K x 32-bit dual-ported on-chip memory (544 Kbits configurable)
- 64M x 32-bit word external address space
- Glueless SDRAM interface
- 2 serial transmit/receive ports support 32-channel TDM
- I<sup>2</sup>S mode supports up to 8 channels
- Two timers with event capture and PWM options
- 12 programmable I/O pins
- 10 DMA channels
- Glueless multiprocessing with two ADSP-21065L SHARC DSPs
- SHARC DSP family binary code compatible
- 3.3 Volt, 208-pin PQFP, 196 ball mBGA
- QFP and BGA packages available

### Target Markets

- Digital Audio
  - Digital Amplifiers, Keyboards, Digital Speakers, Synthesizers, Professional Audio Mixing Consoles, Digital Equalization and Effects Processing
- Automotive
  - Digital Surround Audio, Cruise Control, Collision Avoidance, and In-cabin Multi-Function Platforms
- Communications
  - Computer Telephony, Multifunction Desk-phones, GPS (Global Positioning Satellite), Speech Recognition, Video Phones, Voice and Data Infrastructure Equipment
- Industrial and Medical
  - Bar-Code Scanners, Factory Automation Systems, Electronic Metering, Imaging, ECG, and Ultrasound Equipment
- Instrumentation
  - Digital Oscilloscopes, Spectrum Analyzers, Network Analyzers and Test Equipment
- Biometrics
  - Fingerprint Recognition and Speaker Identification



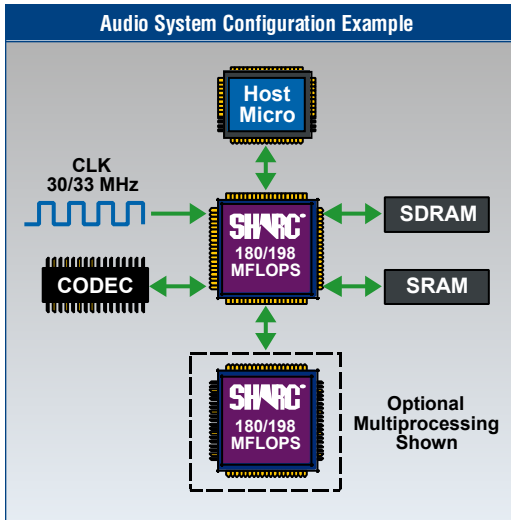
**Communications • Digital Audio • Automotive  
Industrial and Medical • Instrumentation • Biometrics**

*The SHARC DSP Family Consists of 32-bit Floating-point Processors, Which are Easily Programmable to Suit Many Price Sensitive, High Precision Applications.*

### Overview

The ADSP-21065L SHARC<sup>®</sup> DSP is a general-purpose, programmable 32-bit DSP that allows users to program with equal efficiency in both fixed- or floating-point arithmetic. The primary feature of this SHARC DSP is its leading floating-point DSP core with a rich and powerful instruction set. The two processing elements in the core allow for parallel computes, loads and stores maximizing data throughput. The ADSP-21065L has a dual-ported memory architecture which enables simultaneous access of two operands and I/O processing. The two on-chip buses allow two data operands to be fetched from memory, while an instruction cache provides instructions when needed for an overall three bus performance. In addition, the zero-overhead DMA allows the core to access internal memory in parallel with IOP accesses preventing core stalls. For additional performance, the ADSP-21065L has on-chip bus arbitration for glueless multiprocessing. The multiprocessor address space allows the processors to share DSP resources.

This 32-bit floating-point DSP is an excellent choice for audio applications allowing for easy integration with ADI's high performance converters and additional bits for extra precision. The ADSP-21065L is code compatible with the SHARC DSP family making it easier for customers to have immediate access to software and hardware development tools from ADI and SHARC DSP third-party developers.



SHARC DSPs Provide Superior System Performance to a Wide Range of Real-time, Embedded Applications. The ADSP-21065L Uses Multiple Buses to Create High-speed Thoroughfares Between the Core, I/O Peripherals, Internal Dual-ported Memory and External Synchronous DRAM.

### Development Tools

SHARC DSPs are supported by ADI's CROSSCORE™ brand of industry leading development tools. The CROSSCORE components include the VisualDSP++™ software development environment, EZ-KIT Lite™ evaluation systems, and emulators. VisualDSP++ is an integrated software development environment, allowing for fast and easy development, debug, and deployment. The EZ-KIT Lite evaluation system provides an easy way to investigate the power of the Analog Devices family of processors and begin to develop applications. Emulators are available for PCI and USB host platforms for rapid on-chip debugging. Additional development tools and algorithms are available from an extensive third-party development community.

### CROSSCORE Tools Support

Tel: 1-800-ANALOGD  
 Email: [dsptools@analog.com](mailto:dsptools@analog.com)  
 Web: [www.analog.com/dsp/tools](http://www.analog.com/dsp/tools)

### Ordering Information

Please call Analog Devices CROSSCORE Tools at 603/883-2430 or your local ADI sales representative or distributor for pricing and ordering information for part number: **ADDS-21065L-EZLITE**.

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ADSP-21065L SHARC DSP Benefits	
Features	Benefits
<b>32-bit Processing</b>	<ul style="list-style-type: none"> <li>• 32-bit words essential for processing 20 and 24-bit input signals</li> <li>• Improved signal-to-noise ratio at low levels</li> <li>• Wide dynamic range</li> </ul>
<b>Fixed- and floating-point</b>	<ul style="list-style-type: none"> <li>• Greater flexibility</li> <li>• Reduced development time</li> </ul>
<b>Up to 66 MIPS, 198 MFLOPS</b>	<ul style="list-style-type: none"> <li>• Eliminates bus bottlenecks</li> </ul>
<b>16K x 32bit (544 Kbits) of user-configurable on-chip memory</b>	<ul style="list-style-type: none"> <li>• Reduces overall system cost, size and power consumption</li> <li>• Allows freedom in allocating data and program memory</li> </ul>
<b>Feature-rich I/O:</b> <ul style="list-style-type: none"> <li>- 2 serial Tx +2 serial and Rx ports</li> <li>- I<sup>2</sup>S Interface</li> <li>- TDM Interface</li> <li>- 10 DMA Channels</li> </ul>	<ul style="list-style-type: none"> <li>• Process more audio channels using just one DSP</li> <li>• Multiple channels supported in communication systems</li> <li>• Direct interface to T1/E1 lines</li> </ul>
<b>Glueless 32-bit SDRAM Interface</b>	<ul style="list-style-type: none"> <li>• Maximize synchronous data transfer rate</li> <li>• Reduce overall system cost</li> </ul>
<b>Up to 264 Mbytes/sec external port</b>	<ul style="list-style-type: none"> <li>• Maximum data throughput</li> </ul>
<b>Non-intrusive DMA</b>	<ul style="list-style-type: none"> <li>• Utilize full capabilities of core processor</li> </ul>