Technical Notes on using Analog Devices' DSP components and development tools
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ADSP-2106x SPORT DTx Pins: Is There Potential MCM Data Contention Between Different SHARCs on Adjacent TDM Timeslots?

Last Modified: 9/2/98
By: JT

Question:

Dear ADI SHARC Apps Engineer,

I plan to use multiple SHARCs (ADSP-21060s) in my design, sending data to each other via the SPORTs in multichannel mode. I think it's safe to say they will all be within 25C of each other.

A question came up when I was reviewing the SPORT timings in the data sheet. I am very concerned about a possible contention on the DTx pin of the SPORTs for multiple DSPs transmitting in adjacent channels.

Looking on page 36 in the 21060 Data Sheet in (Figure 22), there are 2 timing parameters:

T_{DDTEN} - Data Enable from External SCLK - 3.5 nanoseconds minimum

T_{DDTTE} - Data Disable from External SCLK - 10.5 nanoseconds maximum

It appears that there can be a potential 7 ns of overlap in transmitting for the last bit of one SHARC's channel to the first bit in the next channel by another SHARC.

I am trying to get an understanding of how much contention there really is. Is there really 7ns of contention possible? If this potential for overlap exists, will it be small enough where contention will be negligible? Also, Is there any characterization data for a maximum overlap specification?

Are there things we can control, perhaps in software and how the port is used, that can minimize the contention? Still, it seems that limiting the environmental variables will lessen, but not eliminate, the contention problem. Is this correct? Our concern is that we are using our design to test flight boards and that bus contention will shorten the life of the devices contending.

Answer:

The apparent serial port contention issue is an artifact of specifications that are meant to cover all possible situations and are not intended to be added or subtracted. i.e.:

- one specification comes from "Fast process"/ -40C /"High VDD"
- and one comes from "Slow process"/ 85C / "Low VDD"

This sets up an extreme worst case scenario. We are already aware that this is a timing discrepancy in the data sheet specification.

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In reality this contention is unlikely to occur since the parametric operating point of all devices (voltage, temperature and process) are likely to be similar and significantly more closely matched that the intentionally skewed material that we used for characterization.

With regards to the driver vulnerability to driven conflict - assuming that there is a driven conflict at each channel switch point, the SHARC drivers in particular were designed to be more robust than they need to be. You can easily show this by intentionally overdriving an output pin to either power rail continuously without damaging the driver. If you did this to all driver pins on the part simultaneously you may damage the part, but a periodic driven conflict on a single pin for a 7ns duration is very unlikely to damage the driver.

The risk of long term damage due to the conflict is significantly less than the standard risk of ESD damage to the pin involved in normal handling.

Analog Devices Test Results

Information was gathered in response to your question regarding an apparent overlap between serial port data transmissions. The results are shown in TABLE 1. The datasheet shows, for externally clocked serial ports, an apparent overlap of 7ns between devices enabling and disabling SPORT data transmissions. Actual data however, from production devices **Device "A"** (enabling data transmission device) and **Device "B"** (disabling data transmission), is shown in TABLE1 in nanoseconds.

SPORT data transmission overlap was only evidenced in one of the above test cases ie: Both parts at max temperature (85C) and opposite voltage extremes. The overlap was 0.20nS. This is not considered significant and is unlikely to result in any adverse conditions. Given that the measurement techniques on the automated tester are conservative in their determination of release to tri-state, this is likely not to exist.

TABLE1. SPORT MCM Mode Overlap Test

Temperature		A=4.7V	B=5.3V		
DevA	DevB	DevA	DevB	(B - A)	ns
85C	85C	6.89	6.25	-0.64	
85C	25C	6.89	5.26	-1.63	
85C	-40C	6.89	4.63	-2.26	
25C	-40C	6.02	4.63	-1.39	
-40C	-40C	5.23	4.63	-0.60	
Temperature		**A=5.3V**	**B=4.7V**		
DevA	**DevB**	**DevA**	**DevB**	**(B - A)**	**ns**
85C	85C	6.41	6.61	+0.20	
85C	25C	6.41	5.71	-0.70	
85C	-40C	6.41	4.81	-1.60	
25C	-40C	5.53	4.81	-0.72	
-40C	-40C	4.94	4.81	-0.13	
Temperature		**A=5.3V**	**B=5.3V**		
DevA	**DevB**	**DevA**	**DevB**	**(B - A)**	**ns**
85C	85C	6.41	6.25	-0.16	
85C	25C	6.41	5.26	-1.15	
85C	-40C	6.41	4.63	-1.78	
25C	-40C	5.53	4.63	-0.90	
-40C	-40C	4.94	4.63	-0.31	

NOTE:
PartA always the device enabling a data transmission
PartB always the device disabling a data transmission

A "-" in the "B-A" category indicates no overlap
A "+" in the "B-A" category indicates overlap

Additional Information:

1) Chapter 10: Serial Ports, *ADSP-2106x SHARC User's Manual,* Second Edition, Analog Devices Inc, Norwood, MA, (1996)

2) *ADSP-21062/ADSP-21062L Data Sheet*, ,Rev A, Analog Devices Inc, Norwood, MA (1998)