



Moving from the ADSP-21160M SHARC® DSP to the ADSP-21160N SHARC DSP

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Introduction

While functionally the ADSP-21160M SHARC® DSP and ADSP-21160N SHARC DSP are essentially the same, there are some issues that need to be addressed when moving from ADSP-21160M to the ADSP-21160N in your design. It is important to look at the datasheet for the ADSP-21160N when migrating your design to the ADSP-21160N. Below is a list of items to keep in mind:

Considerations

1. The nominal core voltage requirement on the ADSP-21160N is 1.9V vs. the 2.5V required on the ADSP-21160M.
2. On the ADSP-21160N, an external pull-up resistor should be placed on /HBG as some aspects of the host bus signaling were changed in the silicon for the ADSP-21160N. We recommend a resistor value in the 20-50K ohm range be placed on /HBG.
3. The new startup specification will apply to ADSP-21160N due to the PLL re-design. This information is documented in the ADSP-21160N datasheet.
4. All anomalies on the ADSP-21160M have been resolved in the ADSP-21160N except for anomalies numbers 44-56 and anomaly number 14. Both the ADSP-21160N anomaly list and the ADSP-21160M anomaly

list are available on the web at www.analog.com

5. Since the ADSP-21160N does not have many of the anomalies that are present on the ADSP-21160M silicon, those M specific workarounds should not be implemented in the N design. We recommend that any workarounds implemented be reviewed for compatibility to N silicon. Below are some notes on anomaly workarounds that should be reversed when moving to N silicon:
 - a. Anomaly #13 IMASKP register not updated correctly - If the workaround is left unchanged in design when moving to N silicon the workaround will result in incorrect interpretation of IMASKP settings. Backing out workaround can be done via the use of conditional code based upon silicon ID information in MODE2_SHDW register and thus accommodate all revisions of ADSP-21160M and ADSP-21160N.
 - b. Anomaly #44 IMASKP bits are left shifted by 1 bit for writes to bits 14-31. If the workaround is left in place it will result in incorrect settings of IMASKP register by user code. Backing out workaround can be done via the use of conditional code based upon silicon ID information in MODE2_SHDW register and thus accommodate all revisions of ADSP-21160M and ADSP-21160N.

- c. Anomalies #22 and #23 deal with the PLL and power sequencing. Do not implement the workaround in the ADSP-21160M anomaly list. Instead be sure to follow the power up sequence documented in the ADSP-21160N datasheet.

Check the ADSP-21160N anomaly list for anomalies that would be present on the ADSP-21160N and not on the ADSP-21160M. There are anomaly workarounds that do not need to be reversed, but can be reversed to simplify your system or increase available bandwidth.

- 6. A number of pins on the ADSP-21160N ball out are different than the ones on the ADSP-21160M ball out. To be exact, A14, B13, C12 are connected to VDD and M4 is connected to GND on the ADSP-21160M silicon, but are NC on the ADSP-21160N silicon. Those pins are not connected internally. While you can just as well leave them floating, connecting them to GND or Voltage won't do any harm. You will not need to implement layout changes due to the fact that this pins are indicated as NC in the datasheet.

References

- [1] ADSP-21160M SHARC DSP Datasheet. Rev. 0, Analog Devices, Inc.
- [2] ADSP-21160N SHARC DSP Datasheet. Rev PrB, Analog Devices, Inc.
- [3] ADSP-21160M anomaly list. April 2003, Analog Devices, Inc.
- [4] ADSP-21160N anomaly list. April 2003, Analog Devices, Inc.
- [5] ADSP-21160 Hardware Reference. Second Edition, March 2002. Analog Devices, Inc.

All references are available on the Analog Devices website at www.analog.com

Document History

Version	Description
September 02, 2003 by G.Linden	Added consideration 6 regarding NC pins on the 21160N
May 21, 2003 by G.Linden	Updated item 4 to reflect new anomalies found on the 21160.
June 26, 2002 by G.Linden.	Initial Release