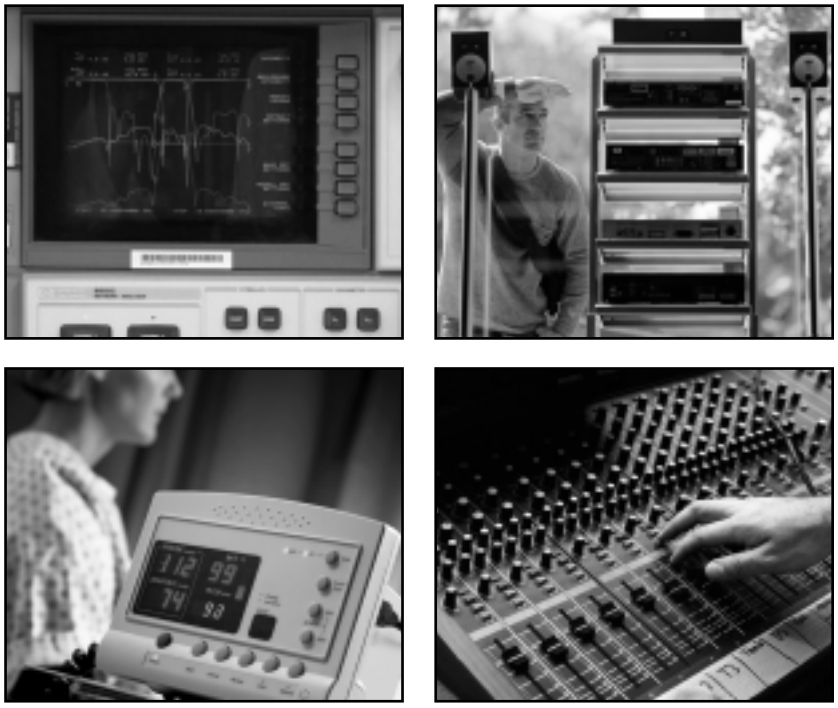
ADSP-21262 High Performance Third Generation SHARC DSP

ADSP-21262 DSP Key Features

- 200 MHz (5 ns) SIMD SHARC core capable of 1200 MFLOPS
- Code compatible with all SHARC DSPs
- IEEE compatible 32-/40-bit floating-point and 32-bit fixed-point data types
- 2 Mbits on-chip dual-ported SRAM
  - 2.4 Gbyte/s on-chip bandwidth
- 4 Mbits mask-programmable ROM
- 22 zero-overhead DMA channels
- Six independent serial ports providing up to 24 serial data channels
  - Standard DSP serial, I^2S, left justified sample-pair and TDM modes
  - Up to 12 TDM streams of 128 channels per frame with support for H.100 and H.110 telephony interfaces and selection of companding on a channel basis
- SPI® compatible interface
- 16-bit parallel port
- Digital Applications Interface providing:
  - 12 precision clock generators
  - Input data port, which includes the parallel data acquisition port (PDAP)
  - Signal routing unit, enabling software control of all the DAI components
- PLL, providing many software and hardware multiplier/divider ratios
- Four timers: one core and three timers supporting PWM generation, capture/ pulse width measurement and external watchdog modes
- 136-ball BGA (12 mm × 12 mm) and 144-lead LQFP (20 mm × 20 mm) packages
- Commercial and industrial temperature ranges



ADSP-21262 SHARC DSP enables the lowest system cost through high system integration; it is optimized for a wide range of general-purpose applications.

Low Cost 32-Bit Floating-Point SHARC Optimized for High Precision Signal Processing

The ADSP-21262 is the first member of the third generation of SHARC® programmable DSPs. The ADSP-21262 delivers high performance floating-point processing at the lowest system cost. Optimized for applications requiring high precision signal processing, such as consumer and professional audio, automotive entertainment systems, voice recognition, medical appliances and measurement devices, the ADSP-21262 leverages the integration of large on-chip memory with a wide variety of peripheral support that allows designers to speed time to market and reduce development and system costs.

The ADSP-21262 is based on the SHARC single-instruction, multiple-data (SIMD) core, which supports execution of 32-bit fixed-point and 32-/40-bit floating-point arithmetic formats. With its core running at 200 MHz, the ADSP-21262 executes 1024-point complex Fast Fourier Transform (FFT) operations in 46 µs. The SIMD mode effectively doubles the DSP performance for audio applications.

Memory and Peripheral Integration Enables High Performance, Low Cost Systems

The ADSP-21262 includes 2 Mbits of on-chip, dual-ported SRAM and 4 Mbits of mask-programmable ROM. This high level of on-chip memory integration enables sustained DSP and I/O performance, without the need for external memory. System I/O is comprised of six full-duplex serial ports, four timers, a 16-bit parallel port, a serial peripheral interface (SPI), 22 zero-overhead Direct Memory Access (DMA) channels delivering fast data transfers without DSP intervention and an innovative Digital Applications Interface (DAI) offering complete software control through its Signal Routing Unit (SRU).

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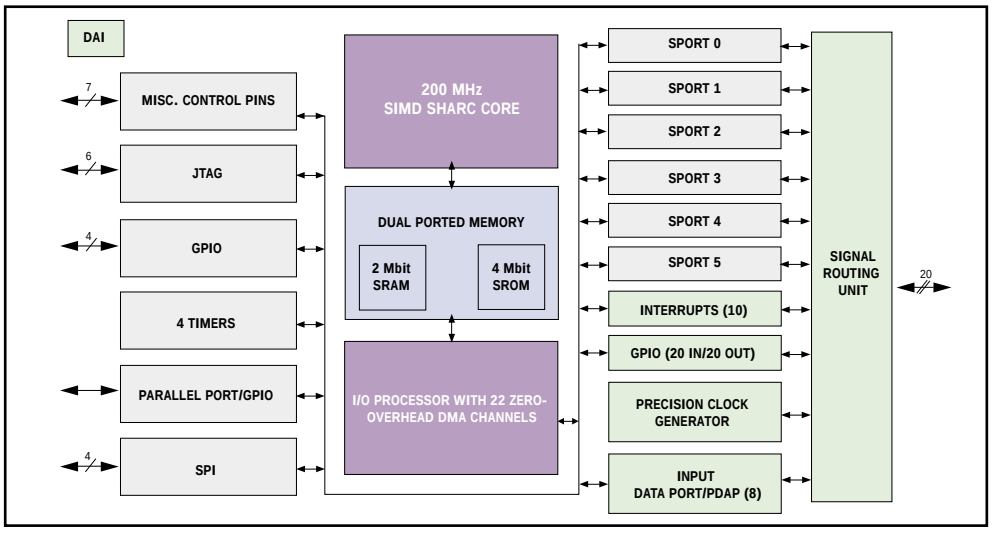


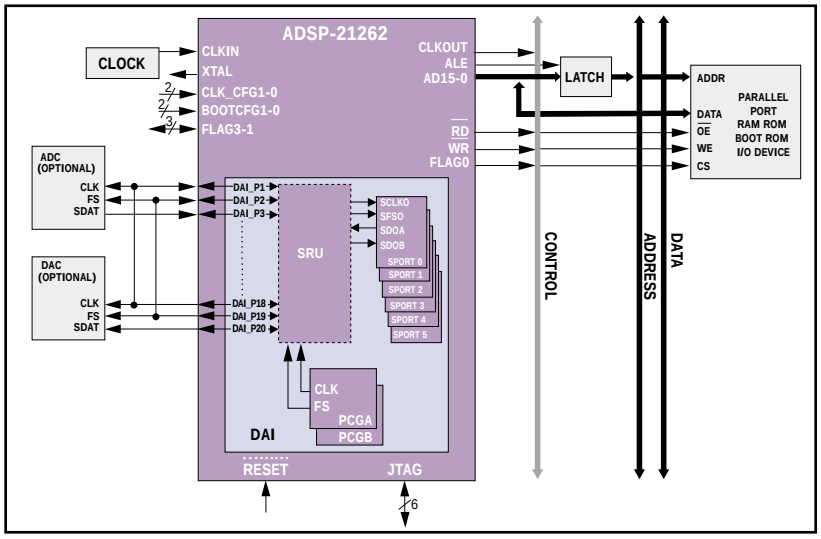
ADSP-21262 Functional Block Diagram.

Digital Applications Interface for Simplified I/O System Development

The ADSP-21262 introduces the DAI, an innovative architecture that enables complete software programmability of various peripherals. The flexibility and ease of use of the SHARC programming model, combined with the DAI, allow manufacturers to deploy one hardware configuration for multiple product offerings with different I/O requirements.

Connections are made using the flexible SRU, a matrix routing group of pins that provides configurable and flexible connectivity between all DAI components and the SRU. Peripherals connected through the DAI are 12 precision clock generators (PCGs), an input data port (IDP), six SPORTS (serial ports), six flag inputs, six flag outputs, three timers, and the SRU. The IDP provides an additional input path to the DSP core, configurable as eight channels of receive serial data or as seven channels of receive serial data and a single channel of up to 20-bit wide parallel data.

An ADSP-21262 sample configuration taking advantage of one of the many possible DAI connections.



CROSSCORE™ Development Tools

Development Tools and Third-Party Developers

The SHARC DSP family is supported by CROSSCORE, Analog Devices' product line of DSP software and hardware development tools. The CROSSCORE components include the VisualDSP++™ software development and debugging environment, EZ-KIT Lite™ evaluation kits, and emulators for rapid on-chip debugging.

The SHARC DSP architecture is supported by the DSP Collaborative™, Analog Devices' third-party network. DSP Collaborative developers help decrease customer time to market by providing products and services, such as completely populated SHARC DSP design hardware, algorithms/source code, reference designs, and consultant services.

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