ADSP-21262 EZ-KIT Lite®
Evaluation System Manual

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ANALOG DEVICES

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Regulatory Compliance

The ADSP-21262 EZ-KIT Lite evaluation system is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The ADSP-21262 EZ-KIT Lite evaluation system has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC amended by 93/68/EEC and, therefore, carries the "**CE**" mark.

The ADSP-21262 EZ-KIT Lite evaluation system has been appended to Analog Devices, Inc. EMC Technical File (EMC TF) referenced "**DSPTOOLS1**" dated December 21, 1997 and was declared CE compliant by an appointed Notified Body (No.0673) as listed below.

Notified Body Statement of Compliance: Z600ANA1.013

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The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

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PREFACE

USING THE ADSP-21262 EZ-KIT LITE

ADSP-21262 EZ-KIT LITE HARDWARE REFERENCE

PREFACE

Thank you for purchasing the ADSP-21262 EZ-KIT Lite®, Analog Devices, Inc. evaluation system for SHARC® processors (DSPs).

The SHARC processors are based on a 32-bit super Harvard architecture that includes a unique memory architecture comprised of two large on-chip, dual-ported SRAM blocks coupled with a sophisticated IO processor, which gives a SHARC processor the bandwidth for sustained high-speed computations. SHARC processors represent today's de facto standard for floating-point processor targeted for premium audio applications.

The evaluation system is designed to be used in conjunction with the CrossCore® Embedded Studio (CCES) and VisualDSP++® development environments to demonstrate capabilities of the ADSP-21262 SHARC processors. The development environment aids advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and ADSP-21262 assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-21262 processor from a personal computer (PC) is achieved through a USB port or an optional JTAG emulator. The USB

interface gives unrestricted access to the ADSP-21262 processor and the evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and processor development tools, go to http://www.analog.com/dsp/tools.

The ADSP-21262 EZ-KIT Lite provides example programs to demonstrate the capabilities of the evaluation board.

Product Overview

The board features:

- Analog Devices ADSP-21262 SHARC processor
  - 136-pin BGA package
  - 300 MHz core clock speed
- Synchronous random access memory (SRAM)
  - 512K bit x 8-bit
- Flash memory
  - 1M x 8-bit
- Serial peripheral interconnect (SPI) flash memory
  - 2M bit

- Analog audio interface
    - AD1835A codec
    - 4x2 RCA phono jack for 4 channels of stereo output
    - 2x1 RCA phono jack for 1 channel of stereo input
    - Headphone jack for 1 channel stereo output
- Digital audio interface (DAI)
    - CS8416 Sony/Philips Digital Interface (S/PDIF) receiver
    - RCA phono jack input
- LEDs
    - Twelve LEDs: one power (green), one board reset (red), S/PDIF (amber), one USB monitor (amber), and eight general-purpose (amber)
- Push buttons
    - five push buttons: one reset, two connected to DAI, two connected to processor FLAG pins
- Expansion interface (type A)
    - Parallel port, FLAGs, DAI, SPI
- Other features
    - JTAG ICE 14-pin header
    - 0-ohm resistors for processor current measurement
    - SPI header
    - DAI header

The EZ-KIT Lite board has a total of 1 MB of parallel flash memory and 2M bit of SPI flash memory. Flash memories can store user-specific boot code, allowing the board to run as a stand-alone unit. For more information, see "External Memory" on page 1-12 and "Boot Mode and Clock Ratio Select Switch (SW10)" on page 2-11. The board also has 512 KB of SRAM, which can be used at runtime.

The DAI of the processor connects to the AD1835A audio codec and the CS8416 S/PDIF receiver. These devices facilitate creation of digital and analog audio signal processing applications. See "Analog Audio Interface" on page 1-13 and "Digital Audio Interface" on page 1-14 for more information.

Additionally, the EZ-KIT Lite board provides access to all of the processor's peripheral ports. Access is provided in the form of a three-connector expansion interface. See "Expansion Interface" on page 2-7 for details.

Purpose of This Manual

The *ADSP-21262 EZ-KIT Lite Evaluation System Manual* provides instructions for installing the product hardware (board). The text describes operation and configuration of the board components and provides guidelines for running your own code on the ADSP-21262 EZ-KIT Lite. Finally, a schematic and a bill of materials are provided as a reference for future designs.

Intended Audience

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set.

Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts that describe your target architecture. For the locations of these documents, see "Related Documents".

Programmers who are unfamiliar with CCES or VisualDSP++ should refer to the online help and the user's manuals.

Manual Contents

The manual consists of:

- Chapter 1, "Using the ADSP-21262 EZ-KIT Lite" on page 1-1
  Provides information on the EZ-KIT Lite from a programmer's perspective and provides an easy-to-access memory map.
- Chapter 2, "ADSP-21262 EZ-KIT Lite Hardware Reference" on page 2-1
  Provides information on the EZ-KIT Lite hardware components.
- Appendix A, "ADSP-21262 EZ-KIT Lite Bill Of Materials" on page A-1
  Provides a list of components used to manufacture the EZ-KIT Lite board.
- Appendix B, "ADSP-21262 EZ-KIT Lite Schematic" on page B-1
  Provides the resources to allow board-level debugging or to use as a reference guide. Appendix B is part of the online help.

What's New in This Manual

This is revision 3.2 of the *ADSP-21262 EZ-KIT Lite Evaluation System Manual*. The manual has been updated to include CCES information. In addition, modifications and corrections based on errata reports against the previous manual revision have been made.

For the latest version of this manual, please refer to the Analog Devices Web site.

Technical Support

You can reach Analog Devices processors and DSP technical support in the following ways:

- Post your questions in the processors and DSP support community at EngineerZone®:
  `http://ez.analog.com/community/dsp`
- Submit your questions to technical support directly at:
  `http://www.analog.com/support`
- E-mail your questions about processors, DSPs, and tools development software from **CrossCore Embedded Studio** or **VisualDSP++**:

  Choose **Help > Email Support**. This creates an e-mail to `processor.tools.support@analog.com` and automatically attaches your **CrossCore Embedded Studio** or **VisualDSP++** version information and `license.dat` file.
- E-mail your questions about processors and processor applications to:
  `processor.support@analog.com` or
  `processor.china@analog.com` (Greater China support)

- In the **USA only**, call **1-800-ANALOGD** (1-800-262-5643)
- Contact your Analog Devices sales office or authorized distributor. Locate one at:
  www.analog.com/adi-sales
- Send questions by mail to:
  Processors and DSP Technical Support
  Analog Devices, Inc.
  Three Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

Supported Processors

The ADSP-21262 EZ-KIT Lite evaluation system supports the Analog Devices ADSP-21262 SHARC processors.

Product Information

Product information can be obtained from the Analog Devices Web site and the online help system.

Analog Devices Web Site

The Analog Devices Web site, www.analog.com, provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a

link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, myAnalog is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests, including documentation errata against all manuals. myAnalog provides access to books, application notes, data sheets, code examples, and more.

Visit myAnalog (found on the Analog Devices home page) to sign up. If you are a registered user, just log on. Your user name is your e-mail address.

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EngineerZone is a technical support forum from Analog Devices. It allows you direct access to ADI technical support engineers. You can search FAQs and technical information to get quick answers to your embedded processing and DSP design questions.

Use EngineerZone to connect with other DSP developers who face similar design challenges. You can also use this open forum to share knowledge and collaborate with the ADI support team and your peers. Visit http://ez.analog.com to sign up.

Related Documents

For additional information about the product, refer to the following publications.

Table 1. Related Processor Publications

Title	Description
ADSP-21261/ADSP-21262/ADSP-21266 SHARC Processor Data Sheet	General functional description, pinout, and timing of the processor
ADSP-2126x SHARC Processor Hardware Reference	Description of the internal processor architecture, registers, all peripheral functions, and all allowed processor assembly instructions

If you plan to use the EZ-KIT Lite board in conjunction with a JTAG emulator, also refer to the documentation that accompanies the emulator.

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
Close command (**File** menu)	Titles in reference sections indicate the location of an item within the development environment's menu system (for example, the **Close** command appears on the **File** menu).
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as `this` or `that`. One or the other is required.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.

Example	Description
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of `this`.
`.SECTION`	Commands, directives, keywords, and feature names are in text with `letter gothic` font.
`filename`	Non-keyword placeholders appear in text with italic style format.
	**Note:** For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	**Caution:** Incorrect device operation may result if ... **Caution:** Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol.
	**Warning:** Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol.

1 USING THE ADSP-21262 EZ-KIT LITE

This chapter provides specific information to assist you with development of programs for the ADSP-21262 EZ-KIT Lite evaluation system.

The information appears in the following sections.

- "Package Contents" on page 1-3
  Lists the items contained in your EZ-KIT Lite package.
- "Default Configuration" on page 1-3
  Shows the default configuration of the EZ-KIT Lite board.
- "CCES Install and Session Startup" on page 1-4
  Instructs how to start a new or open an existing EZ-KIT Lite session using CCES.
- "VisualDSP++ Install and Session Startup" on page 1-8
  Instructs how to start a new or open an existing EZ-KIT Lite session using VisualDSP++.
- "CCES Evaluation License" on page 1-10
  Describes the CCES demo license shipped with the EZ-KIT Lite.
- "VisualDSP++ Evaluation License" on page 1-11
  Describes the VisualDSP++ demo license shipped with the EZ-KIT Lite.
- "External Memory" on page 1-12
  Describes how to access external memory and defines the memory map of the EZ-KIT Lite.

- "Analog Audio Interface" on page 1-13
  Describes how to set up and communicate with the on-board audio codec.
- "Digital Audio Interface" on page 1-14
  Describes how to use the on-board Sony/Philips Digital Interface (S/PDIF) receiver.
- "LEDs and Push Buttons" on page 1-15
  Describes how to configure use the on-board LEDs and bush buttons.
- "Example Programs" on page 1-17
  Provides information about example programs included in the evaluation system.
- "Board Design Database" on page 1-17
  Highlights the available technical resources for the design, layout, fabrication, and assembly of the EZ-KIT Lite.

For information on the graphical user interface, including the boot loading, target options, and other facilities of the EZ-KIT Lite system, refer to the online help.

For detailed information on how to program the ADSP-21262 SHARC processor, refer to the documents referenced in "Related Documents".

Package Contents

Your ADSP-21262 EZ-KIT Lite evaluation system package contains the following items.

- ADSP-21262 EZ-KIT Lite board
- Universal 7V DC power supply
- USB 2.0 cable

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

Default Configuration

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

The ADSP-21262 EZ-KIT Lite board is designed to run outside your personal computer as a standalone unit. You do not have to open your computer case.

When removing the EZ-KIT Lite board from the package, handle the board carefully to avoid the discharge of static electricity, which may damage some components. Figure 1-1 shows the default connector locations and LEDs used in installation. Confirm that your board is set up in the default configuration before using the board.

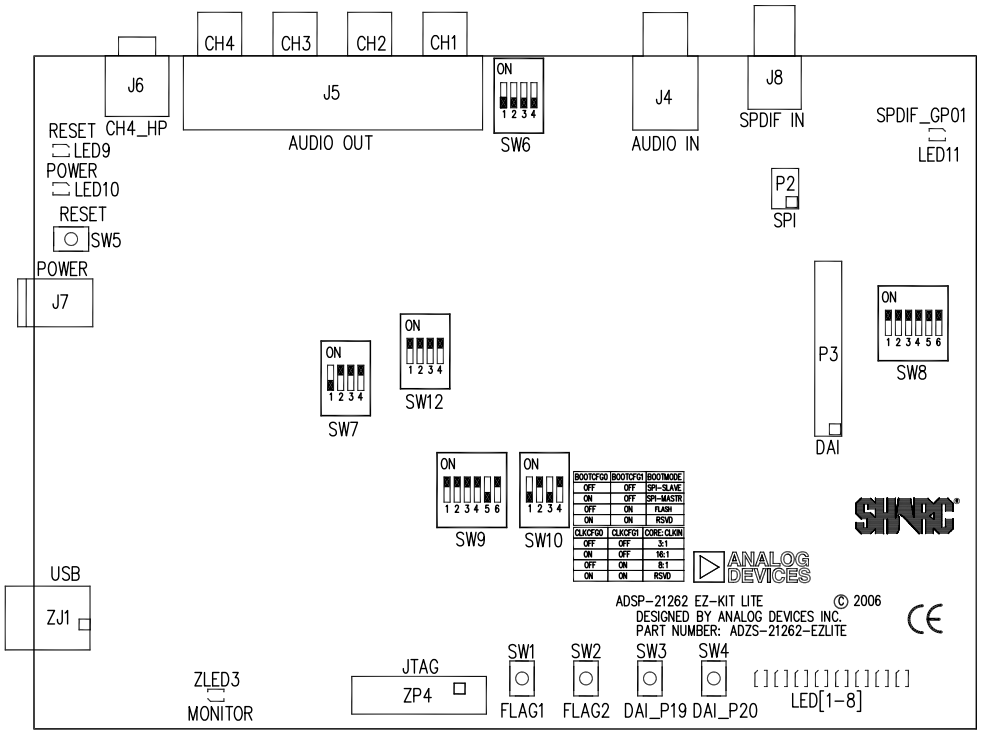


Figure 1-1. EZ-KIT Lite Hardware Setup

CCES Install and Session Startup

For information about CCES and to download the software, go to www.analog.com/CCES. A link for the ADSP-21262 EZ-KIT Lite Board Support Package (BSP) for CCES can be found at http://www.analog.com/SHARC/EZKits.

Follow these instructions to ensure correct operation of the product software and hardware.

Step 1: Connect the EZ-KIT Lite board to a personal computer (PC) running CCES using one of two options: an Analog Devices emulator or via the debug agent.

Using an Emulator:

1. Plug one side of the USB cable into the USB connector of the emulator. Plug the other side into a USB port of the PC running CCES.
2. Attach the emulator to the header connector ZP4 (labeled JTAG) on the EZ-KIT Lite board.

Using the on-board Debug Agent:

1. Plug one side of the USB cable into the USB connector of the debug agent ZJ1 (labeled USB).
2. Plug the other side of the cable into a USB port of the PC running CCES.

Step 2: Attach the provided cord and appropriate plug to the 7V power adaptor.

1. Plug the jack-end of the power adaptor into the power connector J7 on the EZ-KIT Lite board.
2. Plug the other side of the power adaptor into a power outlet. The power LED (labeled LED10) is lit green when power is applied to the board.
3. Power the emulator (if used). Plug the jack-end of the assembled power adaptor into the emulator and plug the other side of the power adaptor into a power outlet. The enable/power indicator is lit green when power is applied.

Step 3 (if connected through the debug agent): Verify that the yellow USB monitor LED (labeled ZLED3)and the green power LED (labeled ZLED4) on the debug agent are both on. This signifies that the board is communicating properly with the host PC and ready to run CCES.

Session Startup

It is assumed that the CrossCore Embedded Studio software is installed and running on your PC.

Note: If you connect the board or emulator first (before installing CCES) to the PC, the Windows driver wizard may not find the board drivers.

1. Navigate to the CCES environment via the **Start** menu.

   Note that CCES is not connected to the target board.

2. Use the system configuration utility to connect to the EZ-KIT Lite board.

   If a debug configuration exists already, select the appropriate configuration and click **Apply and Debug** or **Debug**. Go to step 8.

   To create a debug configuration, do one of the following:

   - Click the down arrow next to the little bug icon, select **Debug Configurations**
   - Choose **Run > Debug Configurations**.

   The **Debug Configuration** dialog box appears.

3. Select **CrossCore Embedded Studio Application** and click  (**New launch configuration**).

   The **Select Processor** page of the **Session Wizard** appears.

4. Ensure **Blackfin** is selected in **Processor family**. In **Processor type**, select **ADSP-21262**. Click **Next**.

   The **Select Connection Type** page of the **Session Wizard** appears.

5. Select one of the following:

   - For standalone debug agent connections, **EZ-KIT Lite** and click **Next**.
   - For emulator connections, **Emulator** and click **Next**.

   The **Select Platform** page of the **Session Wizard** appears.

6. Do one of the following:

   - For standalone debug agent connections, ensure that the selected platform is **ADSP-21262 EZ-KIT** Lite via Debug Agent.
   - For emulator connections, choose the type of emulator that is connected to the board.

7. Click **Finish** to close the wizard.

   The new debug configuration is created and added to the program(s) to load list.

8. In the **Program(s) to load** section, choose the program to load when connecting to the board. If not loading any program upon connection to the target, do not make any changes.

   Note that while connected to the target, there is no way to choose a program to download. To load a program once connected, terminate the session.

To delete a configuration, go to the **Debug Configurations** dialog box and select the configuration to delete. Click and choose **Yes** when asked if you wish to delete the selected launch configuration. Then **Close** the dialog box.

To disconnect from the target board, click the terminate button (red box) or choose **Run > Terminate**.

To delete a session, choose **Target > Session > Session List**. Select the session name from the list and click **Delete**. Click **OK**.

VisualDSP++ Install and Session Startup

For information about VisualDSP++ and to download the software, go to www.analog.com/VisualDSP.

1. Plug the provided power supply into J7 on the EZ-KIT Lite board. Visually verify that the green power LED (LED10) is on.
2. Verify that the red reset LED (LED9) goes on for a moment and then goes off, and, finally, LED1 through LED8 are blinking sequentially.
3. Connect one end of the USB cable to an available full speed USB port on your PC and the other end to ZJ1 on the ADSP-21262 EZ-KIT Lite board.
4. Verify that the yellow USB monitor LED (ZLED3, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.

Session Startup

1. If you are running VisualDSP++ for the first time, navigate to the VisualDSP++ environment via the **Start** > **Programs** menu. The main window appears. Note that VisualDSP++ does not connect to any session. Skip the rest of this step to step 2.

   If you have run VisualDSP++ previously, the last opened session appears on the screen. You can override the default behavior and force VisualDSP++ to start a new session by pressing and holding down the **Ctrl** key while starting VisualDSP++. Do not release the **Ctrl** key until the **Session Wizard** appears on the screen. Go to step 3.

2. To connect to a new EZ-KIT Lite session, start **Session Wizard** by selecting one of the following.

   - From the **Session** menu, **New Session**.
   - From the **Session** menu, **Session List**. Then click **New Session** from the **Session List** dialog box.
   - From the **Session** menu, **Connect to Target**.

3. The **Select Processor** page of the wizard appears on the screen. Ensure **SHARC** is selected in **Processor family**. In **Choose a target processor**, select **ADSP-21262**. Click **Next**.

4. The **Select Connection Type** page of the wizard appears on the screen. Select **EZ-KIT Lite** and click **Next**.

5. The **Select Platform** page of the wizard appears on the screen. In the **Select your platform** list, select **ADSP-21262 EZ-KIT Lite via Debug Agent**. In **Session name**, highlight or specify the session name.

   The session name can be a string of any length; although, the box displays approximately 32 characters. The session name can include space characters. If you do not specify a session name, VisualDSP++ creates a session name by combining the name of the selected platform with the selected processor. The only way to change a session name later is to delete the session and open a new session.

   Click **Next**.

6. The **Finish** page of the wizard appears on the screen. The page displays your selections. Check the selections. If you are not satisfied, click **Back** to make changes; otherwise, click **Finish**. VisualDSP++ creates the new session and connects to the EZ-KIT Lite. Once connected, the main window's title is changed to include the session name set in step 5.

To disconnect from a session, click the disconnect button  or select **Session** > **Disconnect from Target**.

To delete a session, select **Session** > **Session List**. Select the session name from the list and click **Delete**. Click **OK**.

CCES Evaluation License

The ADSP-21262 EZ-KIT Lite software is part of the Board Support Package (BSP) for the SHARC ADSP-2126x family. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for 90 days after activation. Once the evaluation period ends, the evaluation license

becomes permanently disabled. If the evaluation license is installed but not activated, it allows 10 days of unrestricted use and then becomes disabled. The license can be re-enabled by activation.

An evaluation license can be upgraded to a full license. Licenses can be purchased from:

- Analog Devices directly. Call (800) 262-5645 or 781-937-2384 or go to: http://www.analog.com/buyonline.
- Analog Devices, Inc. local sales office or authorized distributor. To locate one, go to: http://www.analog.com/salesdir/continent.asp.

The EZ-KIT Lite hardware must be connected and powered up to use CCES with a valid evaluation or full license.

VisualDSP++ Evaluation License

The ADSP-21262 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ allows a connection to the ADSP-21262 EZ-KIT Lite via the USB Debug Agent interface only. Connections to simulators and emulation products are no longer allowed.
- The linker restricts a users program to 10922 words of memory for code space with no restrictions for data space.

To avoid errors when opening VisualDSP++, the EZ-KIT Lite hardware must be connected and powered up. This is true for using VisualDSP++ with a valid evaluation or full license.

External Memory

The EZ-KIT Lite contains three types of memory: parallel flash (1 MB), serial peripheral interconnect (SPI) flash (2M bit), and synchronous random access memory (SRAM) (512K bit). Flash memories can store user-specific boot code, allowing the board to run as a standalone unit. For more information about setting the boot device for the processor, see "Boot Mode and Clock Ratio Select Switch (SW10)" on page 2-11.

Table 1-1 provides a map of the board's external memory.

Table 1-1. EZ-KIT Lite Evaluation Board External Memory

Start Address	End Address	Content
0x0100 0000	0x010F FFFF	Flash memory
0x0120 0000	0x012F FFFF	SRAM memory
0x0140 0000	0x0140 FFFF	LEDs; see "LEDs and Push Buttons" on page 1-15.
0x0160 0000	0x017F FFFF	Unused chip select 1
0x0180 0000	0x019F FFFF	Unused chip select 2

The parallel flash memory and the SRAM connect to the parallel port of the processor. The parallel port is a multiplexed address and data port. The port can connect to 8-bit and 16-bit memory devices. When configuring the parallel port, keep in mind that the memory devices on the board are 8 bits wide.

To access the SRAM and flash memories, set up a parallel port DMA. For more information on how to connect the SRAM and flash memories, see "Parallel Port" on page 2-3.

The SPI flash memory connects to the processor's SPI port and uses FLAG0 as a chip select. In order for FLAG0 to behave as a chip select, clear the PPFLG bit in the SYSCTL register.

An example program is included in the EZ-KIT Lite installation directory to demonstrate how the parallel port and SPI port can be configured to access the memories.

Analog Audio Interface

The AD1835A is a high-performance, single-chip codec featuring four stereo digital-to-analog converters (DAC) for audio output and one stereo analog-to-digital converters (ADC) for audio input. The codec can input and output data with a sample rate of up to 96 kHz on all channels. A 192 kHz sample rate can be used with the one of the DAC channels.

The processor is interfaced with the AD1835A via the digital audio interface (DAI) port. The DAI interface pins can be configured to transfer serial data from the AD1835A codec in either time-division multiplexed (TDM) or 2-wire interface (TWI) mode. For more information on how the AD1835A connects to the DAI, see "DAI Interface" on page 2-4.

The master input clock (MCLK) for the AD1835A can be generated by the on-board 12.288 MHz oscillator or can be supplied by one of the DAI pins of the processor. Using one if the pins to generate the MCLK, as opposed to the on-board oscillator, allows synchronization of multiple devices in the system. This is done on the EZ-KIT Lite when data is coming from the S/PDIF receiver and being output through the audio codec. The S/PDIF MCLK is routed to the AD1835A MCLK in the processor's signal routing unit (SRU). It is also necessary to disable the on-board audio oscillator from driving the audio codec and the processor's input pin. For instructions on how to configure the clock, refer to "Codec Setup Switch (SW7)" on page 2-8.

The AD1835A codec can be configured as a master or as a slave, depending on the DIP switch settings (SW7). In master mode, the AD1835A drives the serial port clock and frame sync signals to the processor. In slave mode, the processor must generate and drive all of the serial port clock

and frame sync signals. For information on how to set the mode, refer to "Codec Setup Switch (SW7)" on page 2-8.

The AD1835A audio codec's internal configuration registers are configured using the processor's SPI port. The FLAG3 register is used as the select for the device. For information on how to configure the multichannel codec, refer to the product data sheet at AD1835A.

The RCA connector (J4) is used to input analog audio. When using an electret microphone on this connector, configure the SW6 switch according the instructions in "Electret Microphone Select Switch (SW6)" on page 2-8. The four output channels connect to the RCA connector J5. Channel 4 of the codec connects to the headphone jack J6. For more information about the connectors, see "Connectors" on page 2-16.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate how to configure and use the board's analog audio interface.

Digital Audio Interface

The CS8416 is a monolithic complementary metal oxide semiconductor (CMOS) device which receives and decodes one of eight channels of audio data according to IEC60958, S/PDIF, EIAJ CP1201, or AES3 interface standards. The CS8416 receives data from a transmission line, recovers the clock and synchronization signals, and de-multiplexes the audio and digital data.

The CS8416 is attached to the DAI port of the processor. The configuration registers of the S/PDIF receiver are programmed via an SPI, which is connected to the processor's SPI. The S/PDIF receiver is capable of transmitting a variety of data formats, which are set up via the SPI interface. For more information about the CS8416 and DAI connection, see "DAI Interface" on page 2-4.

The S/PDIF input signal is input on J8 via a coax connector.

To output the audio received by the CS8416 via the AD1835A audio codec, the master clock of both chips must be synchronized to prevent the loss of samples. Put the AD1835A in slave mode and disconnect the 12.288 MHz oscillator from the master clock (MCLK) input (see "Codec Setup Switch (SW7)" on page 2-8 for how to).

The CS8416 genera- purpose output 1 (GPO1) is connected to LED11, and can be configured, via the SPI, to indicate a variety of conditions within the S/PDIF receiver.

Shipped with the kit example programs demonstrate how to configure and use the board's digital audio interface.

LEDs and Push Buttons

The EZ-KIT Lite has eight general-purpose user LEDs and four general-purpose push buttons.

Two of the general-purpose push buttons are attached to the processor's FLAG pins, while the other two are attached to the DAI pins. All of the push buttons connect to the processor through a DIP switch. See "Push Button Enable Switch (SW9)" on page 2-11 for instructions on how to disable the push buttons from driving the corresponding processor pins.

The value of the push buttons connected to the FLAG pins can be determined by reading the FLAG register. The push buttons connected to the DAI pins must be configured as interrupts. It is necessary to set up an interrupt routine to determine each pin's state. Table 1-2 shows how each push button connects to the processor. Refer to the related example program shipped with the EZ-KIT Lite for more information.

Table 1-2. Push Button Connections

Push Button Reference Designator	Processor Pin
SW1	FLAG1
SW2	FLAG2
SW3	DAI_P19
SW4	DAI_P20

The LEDs connect to the parallel port pins, AD7-0, via a latch. The parallel port of the processor can be set up as a memory bus or as general-purpose FLAG pins. The latch allows the LEDs to be written to in both cases. Information about setting up the latch can be found in "Push Button Enable Switch (SW9)" on page 2-11.

When the LEDs are accessed as FLAG pins, the latch must be set up to pass through the data on the processor's pins AD7-0. In this mode, it is also necessary to set up the parallel port to be FLAG pins. To set up the parallel port as FLAG pins, set the PPFLG bit in the SYSCTL register. Table 1-3 summarizes the LED and FLAG connections.

Table 1-3. LED Connections

LED Reference Designator	Processor Pin	Mapped as Flag
LED1	AD0	FLAG8
LED2	AD1	FLAG9
LED3	AD2	FLAG10
LED4	AD3	FLAG11
LED5	AD4	FLAG12
LED6	AD5	FLAG13
LED7	AD6	FLAG14
LED8	AD7	FLAG15

An example program is included in the EZ-KIT Lite installation directory to demonstrate functionality of the LEDs and push buttons.

Example Programs

Example programs are provided with the ADSP-21262 EZ-KIT Lite to demonstrate various capabilities of the product. The programs are included in the product installation kit and can be found in the `Examples` folder of the installation. Refer to a readme file provided with each example for more information.

CCES users are encouraged to use the example browser to find examples included with the EZ-KIT Lite Board Support Package.

Board Design Database

A `.zip` file containing all of the electronic information required for the design, layout, fabrication and assembly of the product is available for download from the Analog Devices board design database at: `http://www.analog.com/sharc-board-design-database`.

2 ADSP-21262 EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-21262 EZ-KIT Lite board. The following topics are covered.

- "System Architecture" on page 2-2
  Describes the ADSP-21262 board configuration and explains how the board components interface with the processor.
- "Switch Settings" on page 2-8
  Shows the locations and describes the board switches.
- "LEDs and Push Buttons" on page 2-13
  Shows the locations and describes the LEDs and push buttons.
- "Connectors" on page 2-16
  Shows the locations and provides part numbers for the on-board connectors. In addition, the manufacturer and part number information is provided for the mating parts.

System Architecture

This section describes the processor's configuration on the EZ-KIT Lite board.

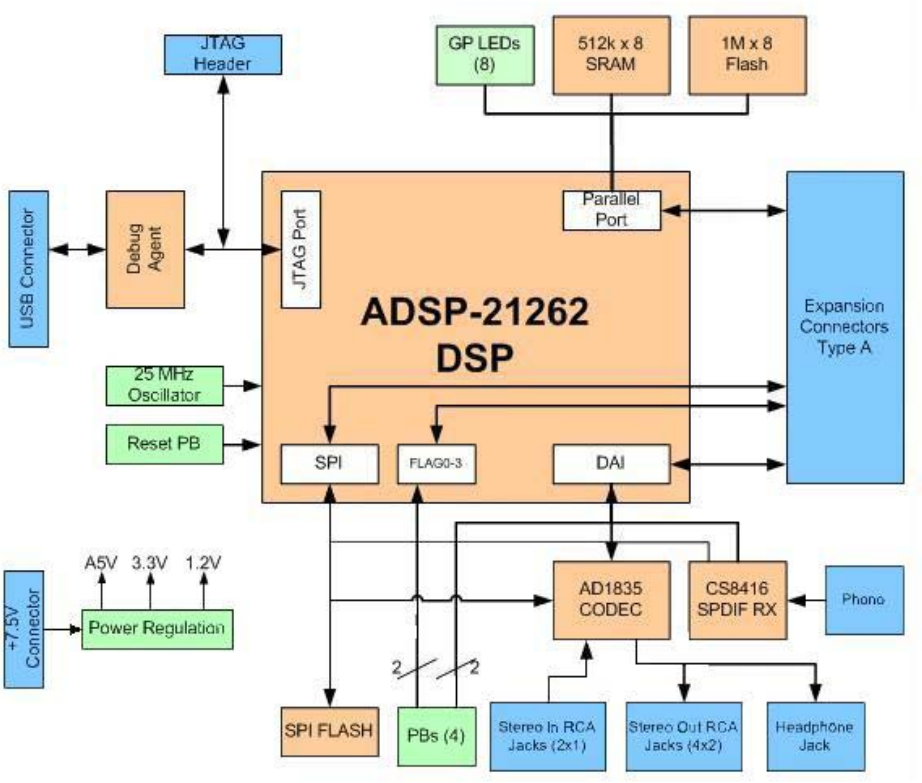


Figure 2-1. System Architecture Block Diagram

This EZ-KIT Lite has been designed to demonstrate the capabilities of the ADSP-21262 processor. The processor core is powered at 1.2V, and the IO is powered at 3.3V. Two 0-ohm resistors give access to the processor's power planes and allow to measure the power consumption of the processor. The R79 resistor provides access to the IO voltage of the processor,

and the R80 resistor provides access to the core voltage plane of the processor.

The CLKIN pin of the processor connects to a 25 MHz oscillator. The core frequency of the processor is derived by multiplying the frequency at the CLKIN pin by a value determined by the state of the processor pins, CLKCFG1 and CLKCFG0. The value at these pins is determined by the state of the SW10 switch (see "Boot Mode and Clock Ratio Select Switch (SW10)" on page 2-11). By default, the EZ-KIT Lite gives a core frequency of 200 MHz.

The SW10 switch also configures the boot mode of the processor. The EZ-KIT Lite is capable of parallel port boot and serial port interconnect (SPI) master boot. By default, the EZ-KIT Lite boots from the parallel port. For information about configuring the boot modes, see "Boot Mode and Clock Ratio Select Switch (SW10)" on page 2-11.

Parallel Port

The parallel port (PP) of the ADSP-21262 processor consists of a 16-bit multiplex address/data memory bus (AD15-0) and an address latch-enable pin (ALE). The interface does not have any memory select pins; these signals must be generated by decoding the address.

The PP connections to the EZ-KIT Lite are shown in Figure 2-2. The PP connects to an 8-bit parallel flash memory, an 8-bit SRAM memory, and eight general-purpose LEDs. The upper three address bits connect to a 3-to-8 decoder, providing eight memory select pins. See "External Memory" on page 1-12 for more information about accessing flash and SDRAM memories.

Because the PP is a multiplexed address/data memory bus, two 8-bit latches are used to latch the upper address bits. Additional latch is used to drive the LEDs. The latter allows the LED values to be written to as if they were at a memory location. For more information about using the LEDs, refer to the "LEDs and Push Buttons" on page 1-15.

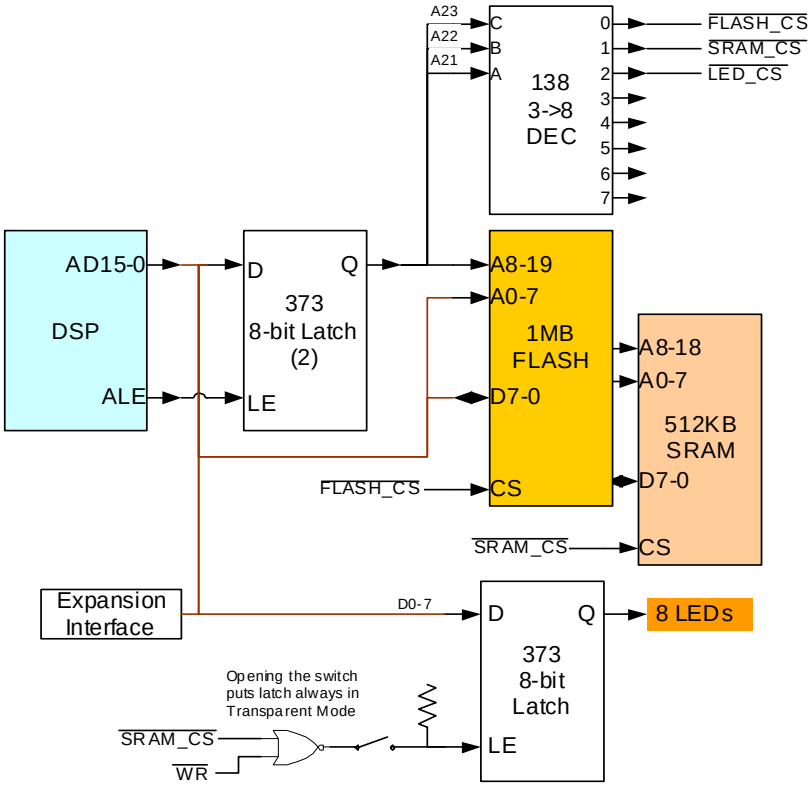


Figure 2-2. Parallel Port Connections Block Diagram

All of the PP signals are available externally via the expansion interface connectors (J1-3). The pinout of the connectors can be found in "ADSP-21262 EZ-KIT Lite Schematic" on page B-1.

DAI Interface

The pins of the digital audio interface (DAI) connect to the signal routing unit (SRU). The SRU is a flexible routing system, providing a large system of signal flows within the processor. In general, the SRU allows to route the DAI pins to different internal peripherals in various combinations.

The DAI pins connect to the AD1835A audio codec, the CS8414 S/PDIF receiver, the audio oscillator output, and two push buttons. Figure 2-3 illustrates the EZ-KIT Lite connections to the DAI.

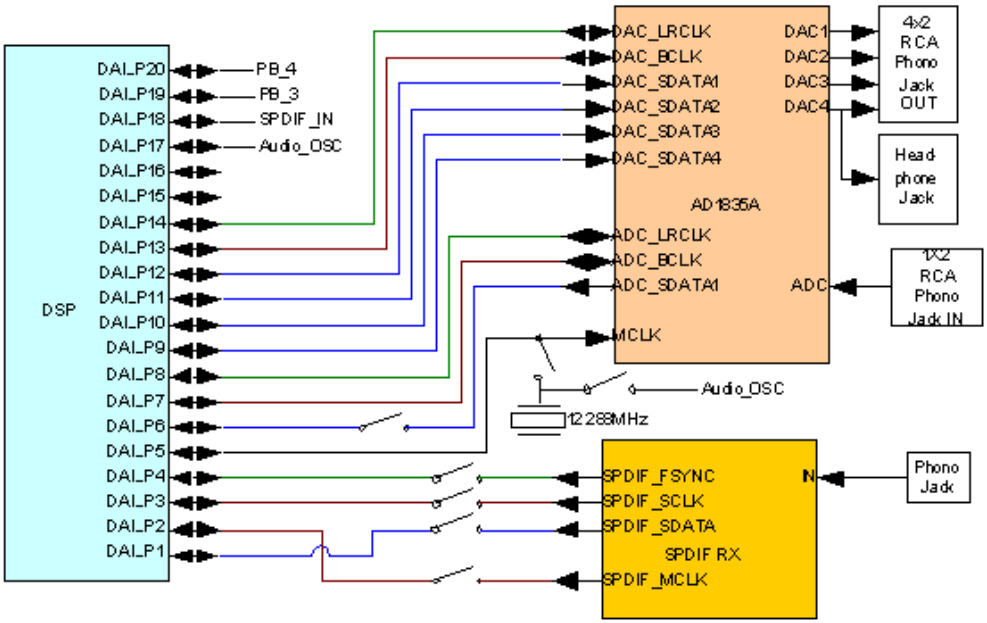


Figure 2-3. DAI Connections Block Diagram

Refer to "Analog Audio Interface" on page 1-13 and "Digital Audio Interface" on page 1-14 for more information about setting the processor to communicate with these devices.

To use the DAI for a different purpose, disable any signal, which is driving the DAI pins, with a switch. See "Codec Setup Switch (SW7)" on page 2-8 and "S/PDIF Signal Enable Switch (SW8)" on page 2-10 for how to information. In addition, the codec setup switch allows flexible routing of the 12.288 MHz audio oscillator's output signal. By default, this signal is used as the master clock (MCLK) for the AD1835A codec.

SPI Interface

The processor's serial peripheral interconnect (SPI) interface connects to an SPI flash memory, the CS8416 S/PDIF receiver, and the AD1835A audio codec. The FLAG0 pin is used as a memory select for accessing the SPI flash memory, and the FLAG3 pin is used for accessing the AD1835A's configuration registers.

The SPI chip select lines for the SPI flash memory and the AD1835A audio codec connect to the processor via switch SW12 pins 1 and 3. The default for SW12 is all positions ON. The switch disables the SPI devices on the EZ-KIT Lite, allowing the same flag pins to be driven on the expansion interface

All of the SPI signals are available externally via the expansion interface connectors (J1-3), as well as the 0.1' spaced header P2. The pinout of these connectors can be found in "ADSP-21262 EZ-KIT Lite Schematic" on page B-1.

Flag Pins

The processor has four general-purpose IO flag pins. Table 2-1 describes the connection of each flag.

Table 2-1. IO Flag Pins

Flag Pin	EZ-KIT Lite Function
FLAG0	SPI flash chip select
FLAG1	Push button (SW1) input
FLAG2	Push button (SW2) input
FLAG3	AD1835A SPI interface chip select

For information on how to disable the push buttons from driving the corresponding processor flag pin, see section "Push Button Enable Switch (SW9)" on page 2-11.

The flag signals are available externally via the expansion interface connectors (J3-1). The pinout of these connectors can be found in "ADSP-21262 EZ-KIT Lite Schematic" on page B-1.

Expansion Interface

The expansion interface consists of the three 90-pin connectors. Table 2-2 shows the interfaces each connector provides. For the exact pinout of these connectors, refer to "ADSP-21262 EZ-KIT Lite Schematic" on page B-1. The mechanical dimensions of the connectors can be obtained from Technical Support.

Table 2-2. Expansion Interface Connectors

Connector	Interfaces
J1	5V, AD15-0
J2	3.3V, FLAG3-0, DAI_P20-1, SPI
J3	5V, 3.3V, RESET, parallel port control signals

Limits to the current and to the interface speed must be taken into consideration when using the expansion interface. The maximum current limit is dependent on the capabilities of the used regulator. Additional circuitry can also add extra loading to signals, decreasing their maximum effective speed.

Analog Devices does not support and is not responsible for the effects of additional circuitry.

JTAG Emulation Port

The JTAG emulation port allows an emulator to access the processor's internal and external memory through a 6-pin interface. The JTAG emulation port of the processor is also connected to the USB debugging interface. When an emulator connects to the board at ZP4, the USB debugging interface is disabled. This is not the standard connection of the JTAG interface.

For information about the standard connection of the interface, see *EE-68* published on the Analog Devices Web site. For more information about the JTAG connector, see "JTAG Header (ZP4)" on page 2-21. To learn more about SHARC processor emulators, go to http://www.analog.com/processors/tools/sharc.

Switch Settings

Figure 2-4 shows the locations and default settings of the EZ-KIT Lite switches.

Electret Microphone Select Switch (SW6)

To connect an electret microphone to the audio input, place all positions of the SW6 switch ON. The default position of this switch is all OFF. When all of the switches are in the ON position, a DC offset of 2.5V is added to the signal, and gain of the input amplifiers is changed from 1x to 10x.

Codec Setup Switch (SW7)

The codec setup switch (SW7) can be used to change the routing of some of the signals going to the AD1835A codec and to setup the communication protocol of the codec.

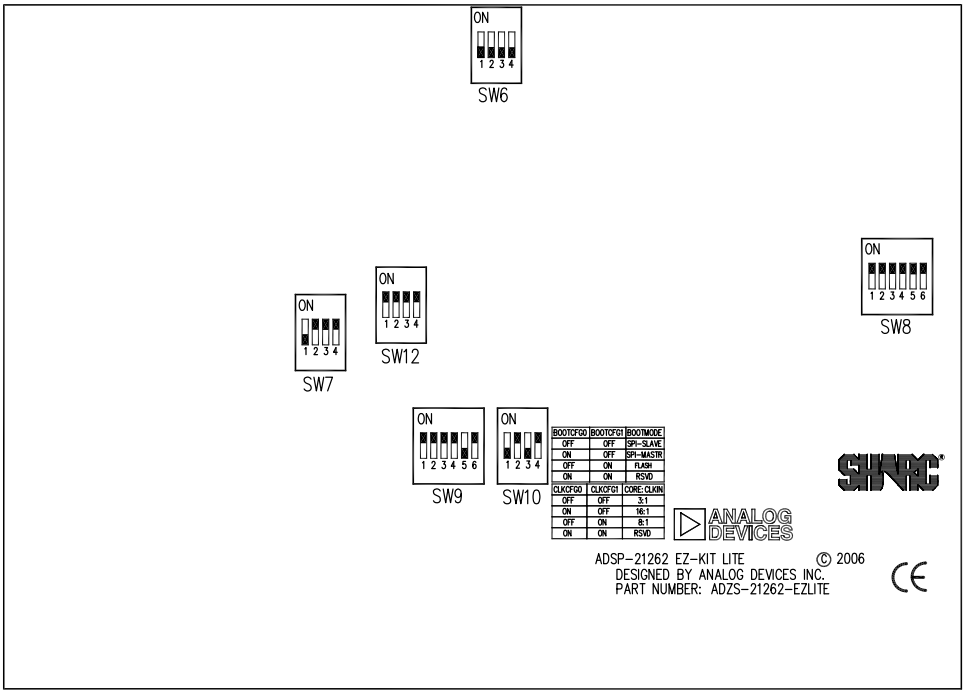


Figure 2-4. Switch Locations and Default Settings

Positions 1 and 2 determine the clock routing for the audio oscillator to the codec and to the processor. Figure 2-5 illustrates how the switch positions 1 and 2 are connected on the board. In the default position, route the DAI_P17 pin to DAI_P6 (in software) to clock the AD1835A.

Position 3 of the SW7 switch determines if the AD1835A device is a master or is a slave. If the AD1835A is a master, the device's serial interface generates the frame sync and clock signals necessary to transfer data. When the device is a slave, the processor must generate the frame sync and clock signals. By default, position 3 is ON, and the AD1835A generates the control signals.

Position 4 of SW7 disconnects the AD1835A codec's ADC_DATA pin from the DAI interface. This is useful when the DAI interface is to connect to another device.

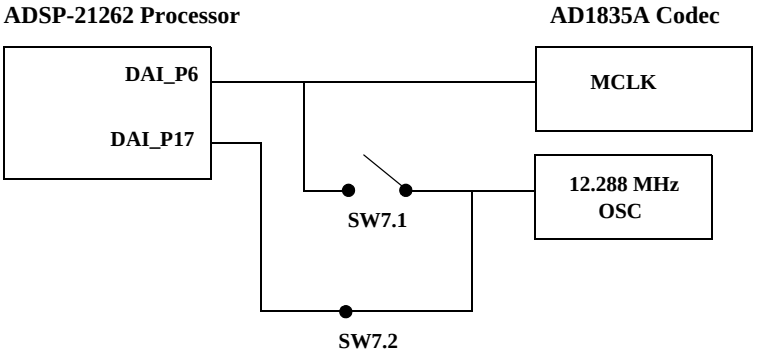


Figure 2-5. Audio Clock Routing

S/PDIF Signal Enable Switch (SW8)

The S/PDIF signal enable switch (SW8) disconnects always driving signal of the CS8416 S/PDIF receiver serial interface.

Table 2-3 shows which processor signal is no longer being driven when the corresponding switch position is OFF.

Table 2-3. SW8 Connections

Switch Position	Processor Pin	S/PDIF RX Pin
1	DAI_P2	MCK
2	DAI_P1	SDATA
3	DAI_P4	FSYNC
4	DAI_P3	SCK
5	DAI_P15	SPI_CS
6	DAI_P16	GPOO

Push Button Enable Switch (SW9)

The push button enable switch (SW9) disconnects the push buttons from the corresponding processor pins. This allows the signals to be used for another purpose. Table 2-4 shows the signal and SW9 connections. By default, all of the position of the SW9 switch are ON, allowing the push buttons to function as designed.

Table 2-4. Push Button Enable Switch (SW9) Connections

Switch Position	Push Button Reference Designator	Processor Pin
1	SW1	FLAG1
2	SW2	FLAG2
3	SW3	DAI_P19
4	SW4	DAI_P20

Position 6 of SW9 connects or disconnects the latch-enable pin of the LED to the logical OR of the $\overline{WE}$ and $\overline{LED\_CS}$ signals. When position is OFF, the latch-enable pin of the LED latch (U24) is always pulled high, making the latch transparent. In this position, the value of the LEDs is directly connected to AD7-0. When position 6 is ON, the values of the LEDs are set by writing to a memory location. The lower 8 bits of the data, written to the address 0x1400 0000, set the values of the LEDs. By default, position 6 is ON, allowing the LEDs to be written by writing to a memory address. For more information refer to "LEDs and Push Buttons" on page 2-13.

Boot Mode and Clock Ratio Select Switch (SW10)

The SW10 switch sets the boot mode and clock multiplier ration. Table 2-5 shows how to set up the boot mode using positions 1 and 2. By default, the EZ-KIT Lite boots in SPI master mode and parallel port mode, and the processor boots from flash memory.

Table 2-5. Boot Mode Configuration

BOOTCFG1 Pin (Position 2)	BOOTCFG0 Pin (Position 1)	Boot Mode
OFF	OFF	SPI slave
OFF	ON	SPI master
ON	**OFF**	**Parallel flash boot (default)**
ON	ON	Internal

Table 2-6 shows how to set up the clock multiply ratio using positions 3 and 4. By default, the processor increases the clock multiply ratio by 8, setting the core clock to 200 MHz.

Table 2-6. Core Clock Rate Configuration

CLKCFG1 (Position 4)	CLKCFG0 (Position 3)	Core to CLKIN Ratio
OFF	OFF	3:1
OFF	ON	16:1
ON	**OFF**	**8:1 (default)**
ON	ON	NA

Loop-Back Test Switch (SW11)

The loop-back test switch (SW11) connects to GPO1 of the CS8416. The GPO1 functionality is programmable via SPI.

SPI Disable Switch (SW12)

The SPI interface switch (SW12) disables the SPI chip select lines connected to the SPI flash memory and the AD1835A audio codec. The switch also disables the ADC_LRCLK and ADC_BCLK signals on the AD1835A device. The switch allows a customer to re-use the same pins on the SPI interface and on the expansion interface. The SW12 default is all positions

ON, unless any of the switch signals or the SPI interface signals are used on the expansion connector or via an EZ-Extender®.

LEDs and Push Buttons

This section describes functionality of the LEDs and push buttons. Figure 2-6 shows the locations of the LEDs and push buttons.

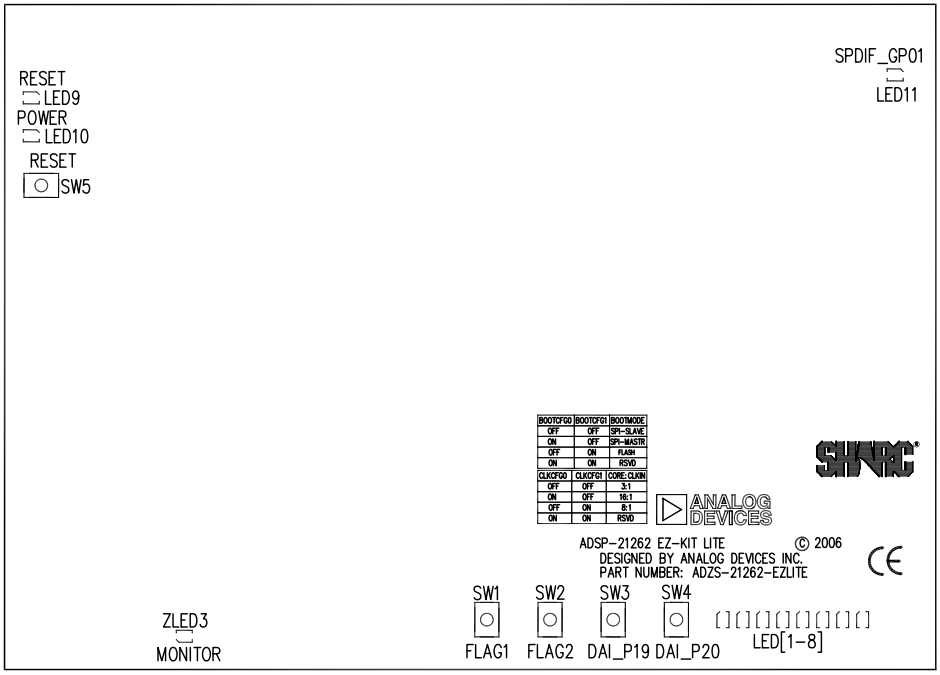


Figure 2-6. LED and Push Button Locations

General Purpose LEDs (LED8–1)

Eight general-purpose LEDs are connected to the processor through a latch on signals AD7-0. These LEDs can be accessed by writing to the FLAG registers or by writing to a memory address. Refer to "LEDs and Push Buttons" on page 1-15 for more information.

Reset LED (LED9)

When LED9 is lit (red), a master reset of all the major ICs is active.

Power LED (LED10)

When LED10 is lit (green), it indicates that power is being properly supplied to the board.

S/PDIF GPO1 LED (LED11)

The S/PDIF GPO1 LED (LED11) connects to the GPO1 signal of the CS8416. The GPO1 functionality is programmable via SPI.

USB Monitor LED (ZLED3)

The USB monitor LED (ZLED3) indicates that USB communication has been initialized successfully and you may connect to the processor using an EZ-KIT Lite session. Once the USB cable is plugged into the board, it takes approximately 15 seconds for the USB monitor LED to light. If the LED does not light, try cycling power on the board and/or reinstalling the USB driver.

When the development software is actively communicating with the EZ-KIT Lite target board, the LED can flicker, indicating communications handshake.

Push Buttons (SW4–1)

Four push buttons (SW4-1) are provided for general-purpose user input. Two of the push buttons connect to the processor's FLAG pins. The other two connect to the processor's DAI. The push buttons are active high and, when pressed, send a high (1) to the processor. Refer to "LEDs and Push Buttons" on page 1-15 for more information. The push button enable switch (SW9) is capable of disconnecting the push buttons from the corresponding processor pin (refer to "Push Button Enable Switch (SW9)" on page 2-11 for more information). The processor signals and corresponding push buttons are summarized in Table 2-7.

Table 2-7. Push Button Connections

Processor Signal	Push Button Reference Designator	Processor Signal	Push Button Reference Designator
FLAG1	SW1	DAI_P19	SW3
FLAG2	SW2	DAIP_20	SW4

Board Reset Push Button (SW5)

The RESET push button (SW5) resets all of the ICs on the board.

Connectors

This section describes the connector functionality and provides information about mating connectors. Figure 2-7 shows the connector locations.

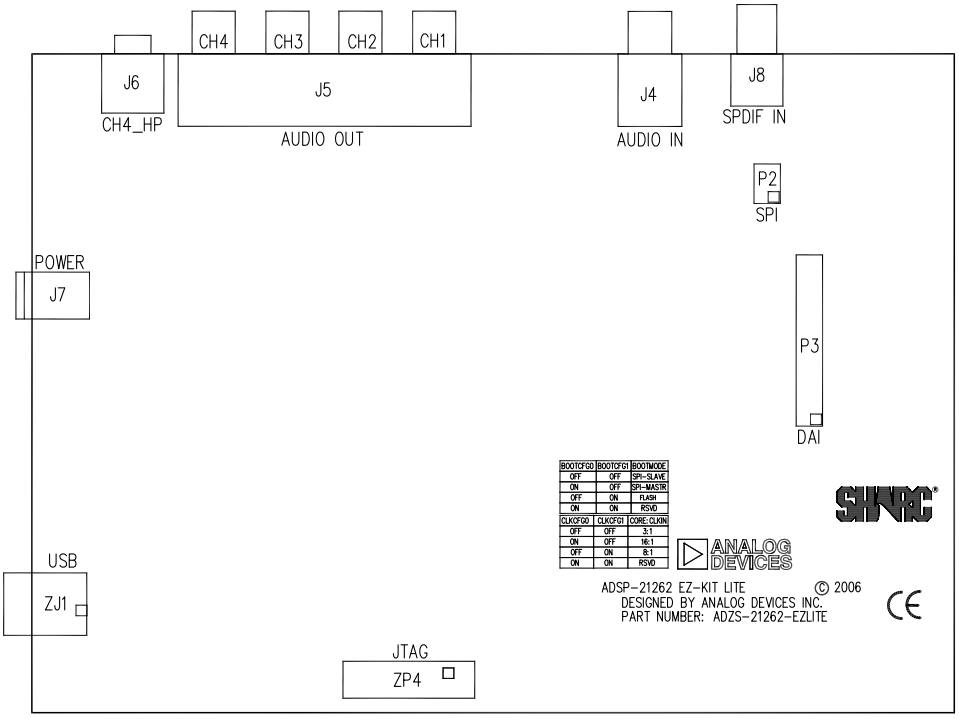


Figure 2-7. Connector Locations

Expansion Interface (J1–3)

Three board-to-board connectors (J1-3) provide signals for most of the processor's peripheral interfaces. The connectors are located at the bottom of the board. For more information about the expansion interface, see "Expansion Interface" on page 2-7. For the connectors availability and pricing, contact Samtec.

Part Description	Manufacturer	Part Number
90-position 0.05" spacing, SMT (J1, J2, J3)	SAMTEC	SFC-145-T2-F-D-A
Mating Connectors		
90-position 0.05" spacing (through hole)	SAMTEC	TFM-145-x1 series
90-position 0.05" spacing (surface mount)	SAMTEC	TFM-145-x2 series
90-position 0.05" spacing (low cost)	SAMTEC	TFC-145 series

Audio In RCA Connector (J4)

Part Description	Manufacturer	Part Number
Two-channel right-angle RCA jack	SWITCHCRAFT	PJRAS1X2S02X
Mating Cable		
Two-channel RCA interconnect cable	MONSTER CABLE	BI100-1M

Audio Out RCA Connector (J5)

Part Description	Manufacturer	Part Number
Six-channel right-angle RCA jack	SWITCHCRAFT	PJRAS4X2U01X
Mating Cable		
Two-channel RCA interconnect cable	MONSTER CABLE	BI100-1M

Headphone Out Jack (J6)

Part Description	Manufacturer	Part Number
3.5 mm stereo jack (J6)	A/D ELECTRONICS	ST-323-5

Power Jack (J7)

The power connector (J7) provides all of the power necessary to operate the EZ-KIT Lite board.

Part Description	Manufacturer	Part Number
2.5 mm power jack (J7)	SWITCHCRAFT DIGI-KEY	RAPC712X RAPC712X-ND
Mating Power Supply (shipped with EZ-KIT Lite)		
7V power supply	CUI STACK	DMS070214-P6P-SZ

The power connector supplies DC power to the EZ-KIT Lite board. Table 2-8 shows the power supply specifications.

Table 2-8. Power Supply Specifications

Terminal	Connection
Center pin	+7 VDC@2.14A
Outer ring	GND

S/PDIF Coax Connector (J8)

Part Description	Manufacturer	Part Number
Coaxial (J8)	SWITCHCRAFT	PJRAN1X1U01X

SPI Header (P2)

The SPI connector (P2) provides access to all of the SPI signals in the from of a .1" spacing header. In addition, the FLAG1 signal can be used as a chip select. If you are using FLAG1 as a chip select, disable the push button associated with the flag. For more information, see "Push Button Enable Switch (SW9)" on page 2-11.

Part Description	Manufacturer	Part Number
6-pin IDC header (P2)	SULLINS	GEC03DAAN

DAI Header (P3)

The DAI connector (P3) provides access to all of the DAI signals in the from of a .1" spacing header. When using the header to access the processor's DAI pins, ensure that signals, which normally drive the processor's DAI pins, are disabled. Refer to "Codec Setup Switch (SW7)" on page 2-8 for more information on how to disable signals already being driven from elsewhere on the EZ-KIT Lite.

Part Description	Manufacturer	Part Number
26-pin IDC header (P3)	BERG	54102-T08-13LF

USB Connector (ZJ1)

The USB connector (ZJ1) allows to configure and program the processor.

Part Description	Manufacturer	Part Number
Type B USB receptacle (ZJ1)	MILL-MAX DIGI-KEY	897-30-004-90-000 ED90064-N

JTAG Header (ZP4)

The JTAG header (ZP4) is the connecting point for a JTAG in-circuit emulator pod. When an emulator is connected to the JTAG header, the USB debug interface is disabled.

Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.

Part Description	Manufacturer	Part Number
14-pin IDC header (ZP4)	FCI	68737-414HLF

A ADSP-21262 EZ-KIT LITE BILL OF MATERIALS

The bill of materials corresponds to "ADSP-21262 EZ-KIT Lite Schematic" on page B-1.

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
1	1	74LVC14A SOIC14	U33	TI	74LVC14AD
2	1	SN74AHC1G02 SOT23-5	U26	TI	SN74AHC1G02DBVRE4
3	1	25MHZ OSC001	U16DIGI-KEY	DIGI-KEY	SGR-8002DC-PCC-ND
4	1	12.288MHZ OSC003	U17	DIGI-KEY	SG-8002CA-PCC-ND(12.288M)
5	1	74LVC138AD SOIC16	U25	TI	SN74LVC138AD
6	3	74LVC373APW TSSOP20	U18,U21,U24	TI	SN74LVC373APWRE4
7	1	IS61LV5128AL TSOP44	U15	ISSI	IS61LV5128AL-10TLI
8	1	LTC1877 MSOP8	VR5	LINEAR TECH	LTC1877EMS8#PBF
9	1	CS8416-CS SOIC28	U3	CIRRUS LOGIC	CS8416-CSZ
10	1	FDC658P SOT23-6	U13	FAIRCHILD	FDC658P

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
11	1	21262 M25P20 "U12"	U12	ST MICRO	M25P20-VMN6TP
12	1	21262 AM29LV081B "U19"	U19	AMD	AM29LV081-120ED
13	1	ADM708SARZ SOIC8	U22	ANALOG DEVICES	ADM708SARZ
14	1	AD8532ARZ SOIC8	U10	ANALOG DEVICES	AD8532ARZ
15	2	ADP3336ARMZ MSOP8	VR1,VR4	ANALOG DEVICES	ADP3336ARMZ-REEL
16	8	AD8606ARZ SOIC8	U2,U4-9,U11	ANALOG DEVICES	AD8606ARZ
17	1	ADSP-21262SKBC-200 BGA136	U1	ANALOG DEVICES	ADSP-21262SKBCZ200
18	1	AD1835AASZ MQFP52	U14	ANALOG DEVICES	AD1835AASZ
19	1	ADP1864 SOT23-6	VR2	ANALOG DEVICES	ADP1864AUJZ-R7
20	5	RUBBER FOOT	M1-5	MOUSER	517-SJ-5018BK
21	1	PWR 2.5MM_JACK CON005	J7	SWITCHCRAFT	RAPC712X
22	1	RCA 4X2 CON011	J5	SWITCHCRAFT	PJRAS4X2U01X
23	1	RCA 1X1 CON012	J8	SWITCHCRAFT	PJRAN1X1U01X
24	5	MOMEN-TARYSWT013	SW1-5	PANASONIC	EVQ-PAD04M

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
25	3	.05 45X2 CON019	J1-3	SAMTEC	SFC-145-T2-F-D-A
26	1	DIP8SWT016	SW11	C&K	TDA08H0SB1
27	2	DIP6SWT017	SW8-9	CTS	218-6LPST
28	4	DIP4SWT018	SW6-7,SW10, SW12	ITT	TDA04HOSB1
29	1	RCA RCA_1X2 CON031	J4	SWITCHCRAFT	PJRAS1X2S02X
30	1	IDC 7X2 IDC7X2	ZP4	FCI	68737-414HLF
31	1	2.5A RESE-TABLEFUS001	F1	RAYCHEM	SMD250F-2
32	1	3.5MM STEREO_JAC K CON001	J6	A/D ELEC-TRONICS	ST-323-5
33	1	IDC 13x2 IDC13x2	P3	BERG	54102-T08-13LF
34	1	IDC 3X2 IDC3X2	P2	SULLINS	GEC03DAAN
35	1	0 1/4W 5% 1206	R82	KOA	0.0ECTRk7372BTTED
36	9	YELLOW LED001	LED1-8,LED11	PANASONIC	LN1461C
37	8	330PF 50V 5% 0805	C104,C106, C108,C110, C112,C114, C116,C118	AVX	08055A331JAT
38	13	0.01UF 100V 10% 0805	C66,C127,C153, C155,C157-158, C160-164,C182, C188	AVX	08051C103KAT2A

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
39	8	0.22UF 25V 10% 0805	C77,C87, C99-102,C111, C131	AVX	08053C224FAT
40	14	0.1UF 50V 10% 0805	C1,C47, C120-121, C132-133,C141, C148,C152, C156,C186-187	AVX	08055C104KAT
41	6	1000PF 50V 5% 0805	C79,C82-83,C85, C88,C98	AVX	08055A102JAT2A
42	21	10K 1/10W 5% 0805	R63-64,R66,R70, R74,R76,R78, R92,R96,R98, R152,R159-164, R171-174	VISHAY	CRCW080510K0JNEA
43	3	33 1/10W 5% 0805	R68,R81,R135	VISHAY	CRCW080533R0JNEA
44	2	4.7K 1/10W 5% 0805	R72,R176	VISHAY	CRCW08054K70JNEA
45	2	2.0K 1/8W 1% 1206	R3,R5	VISHAY	CRCW12062K00FKEA
46	10	49.9K 1/8W 1% 1206	R114-115, R117-124	VISHAY	CRCW120649K9FKEA
47	12	100PF 100V 5% 1206	C2-12,C64	AVX	12061A101JAT2A
48	1	2.2UF 35V 10% B	CT21	AVX	TAJB225K035R
49	2	10UF 16V 10% B	CT13-14	AVX	TAJB106K016R
50	4	100 1/10W 5% 0805	R185-188	VISHAY	CRCW0805100RJNEA
51	2	301.0 1/4W 1% 1206	R1-2	VISHAY	CRCW1206301RFKEA

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
52	9	220PF 50V 10% 1206	C90-97,C183	AVX	12061A221JAT2A
53	1	2A S2A DO-214AA	D2	MICRO COMM	S2A-TP
54	6	600 100MHZ 500MA 1206	FER1-2,FER5-8	STEWARD	HZ1206B601R-10
55	4	237.0 1/8W 1% 1206	R13-14,R18,R20	VISHAY	CRCW1206237RFKEA
56	2	750.0K 1/8W 1% 1206	R11,R116	VISHAY	CRCW1206750KFKEA
57	4	5.76K 1/8W 1% 1206	R6,R10,R19,R22	VISHAY	CRCW12065K76FKEA
58	1	3.01K 1/8W 1% 1206	R125	KOA	RK73H2BTTD3011F
59	10	11.0K 1/8W 1% 1206	R47,R49-50, R52-53,R55-56, R58,R113,R136	VISHAY	CRCW120611K0FKEA
60	5	1UF 16V 10% 0805	C39,C44,C48, C56,C61	PANASONIC	ECJ2FB1E105K
61	1	75 1/8W 5% 1206	R112	VISHAY	CRCW120675R0JNEA
62	1	30PF 100V 5% 1206	C55	AVX	12061A300JAT2A
63	1	10 1/10W 5% 0805	R150	VISHAY	CRCW080510R0FKEA
64	1	249.0K 1/10W 1% 0805	R86	VISHAY	CRCW0805249KFKEA
65	1	124.0K 1/10W 1% 0805	R83	VISHAY	CRCW0805-124KFKEA
66	1	47.0K 1/10W 1% 0805	R17	VISHAY	CRCW080547K0FKEA

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
67	12	680PF 50V 1% 0805	C76,C80-81,C89, C103,C105, C107,C109, C113,C115, C117,C119	AVX	08055A681FAT2A
68	3	10UF 25V +80-20% 1210	C46,C49,C75	PANASONIC	ECJ4YF1E106Z
69	8	2.74K 1/8W 1% 1206	R140-147	VISHAY	CRCW12062K74FKEA
70	20	5.49K 1/8W 1% 1206	R7,R15-16,R21, R25,R28,R31, R34,R37,R40, R43,R46,R48, R51,R54,R57, R59-62	VISHAY	CRCW12065K49FKEA
71	8	1.65K 1/8W 1% 1206	R23,R26,R29, R32,R35,R38, R41,R44	VISHAY	CRCW12061K65FKEA
72	10	10UF 16V 20% CAP002	CT1-9,CT12	PANASONIC	EEE1CA100SR
73	2	68UF 25V 20% CAP003	CT10-11	PANASONIC	EEE-FC1E680P
74	1	2A SL22 DO-214AA	D1	DIGI-KEY	SL22-E3/1GI-ND
75	1	10UH 20% IND001	L1	TDK	445-2014-1-ND
76	1	270 1/10W 5% 0805	R137	VISHAY	CRCW0805270RJNEA
77	10	0 1/10W 5% 0805	R4,R9,R12,R73, R79-80,R90, R126,R151,R192	VISHAY	CRCW08050000Z0EA
78	1	190 100MHZ 5A FER002	FER3	MURATA	DLW5BSN191SQ2

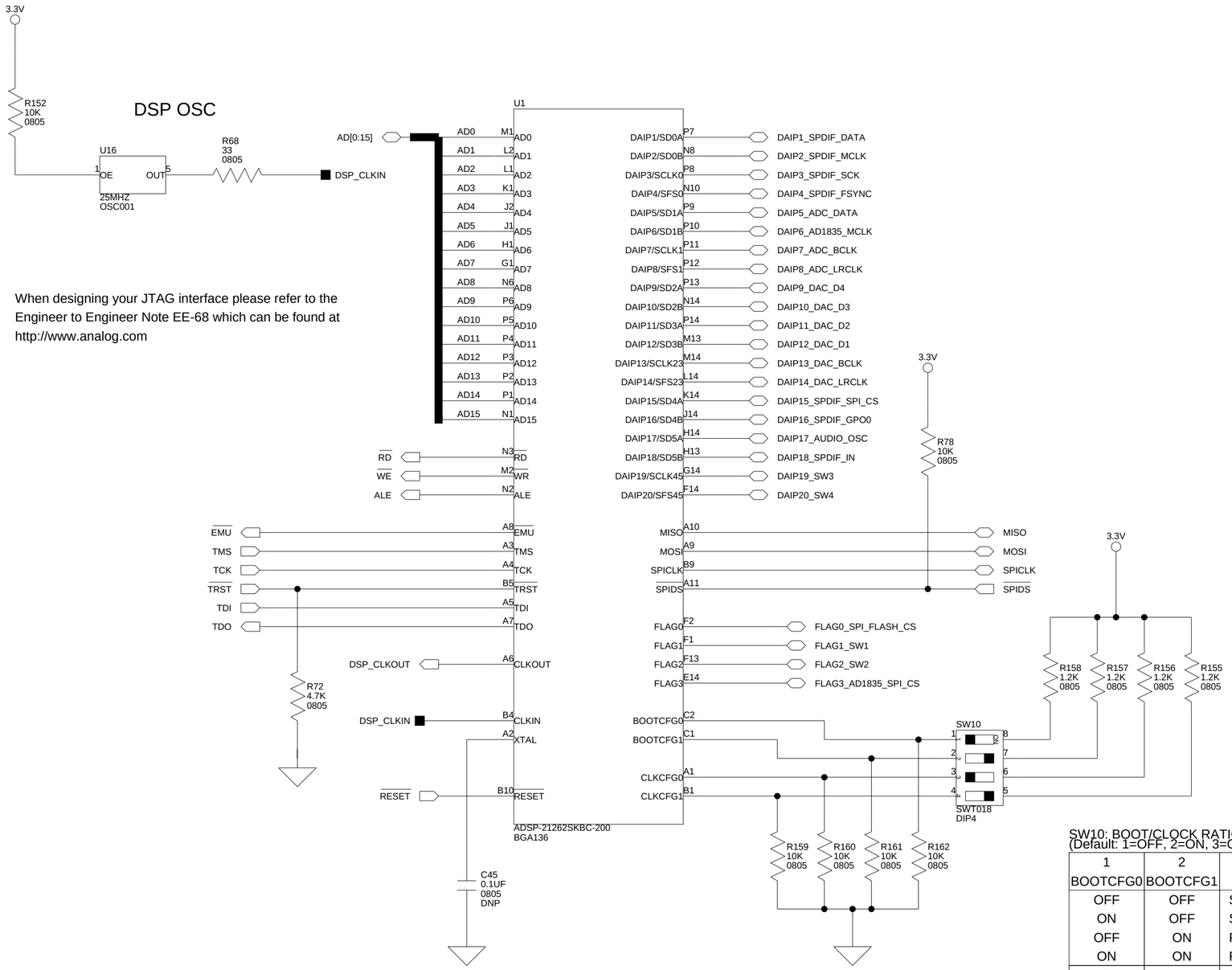
Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
79	8	3.32K 1/10W 1% 0805	R24,R27,R30, R33,R36,R39, R42,R45	PANASONIC	ERJ-6ENF3321V
80	4	1.2K 1/10W 5% 0805	R155-158	VISHAY	CRCW08051K20JNEA
81	6	10UF 6.3V 10% 0805	C26,C40,C50, C52,C84,C145	AVX	080560106KAT2A
82	3	6.04K 1/10W 1% 0805	R65,R148-149	DIGI-KEY	311-6.04KCRCT-ND
83	7	0.1UF 10V 10% 0402	C41,C128-129, C136,C140, C142,C144	AVX	0402ZD104KAT2A
84	5	0.01UF 16V 10% 0402	C134,C138, C147,C149,C151	AVX	0402YC103KAT2A
85	1	47UF 16V 10% D	CT19	DIGI-KEY	478-1788-2-ND
86	8	1000PF 50V 5% 0402	C130,C135, C137,C139, C143,C146, C150,C154	AVX	04025C102JAT2A
87	2	64.9K 1/10W 1% 0805	R67,R87	VISHAY	CRCW080564K9FKEA
88	2	210.0K 1/4W 1% 0805	R69,R88	VISHAY	CRCW0805210KFKEA
89	1	1A SK12 DO-214AA	D3	DIODES INC	B120B-13-F
90	1	0.022UF 50V 5% 0805	C65	AVX	08055C223JAT2A
91	1	68PF 50V 5% 0603	C16	AVX	06035A680JAT2A
92	1	470PF 50V 5% 0603	C15	AVX	06033A471JAT2A

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
93	1	0 1/10W 5% 0603	R85	PHYCOMP	232270296001L
94	1	24.9K 1/10W 1% 0603	R84	DIGI-KEY	311-24.9KHTR-ND
95	1	47UF 6.3V 10% B	CT20	PANASONIC	EEE0JA470WR
96	1	0.05 1/2W 1% 1206	R89	SUSUMA	RL16326-R051-F-N
97	1	10UF 16V 10% 1210	C17	AVX	1210YD106KAT2A
98	1	GREEN LED001	LED10	PANASONIC	LN1361CTR
99	1	REDLED001	LED9	PANASONIC	LN1261CTR
100	2	1000PF 50V 5% 1206	C37-38	AVX	12065A102JAT2A
101	8	2200PF 50V 5% 1206	C67-74	AVX	12065A222JAT050
102	10	270 1/8W 5% 1206	R138-139, R177-184	VISHAY	CRCW1206270RJNEA
103	8	604.0 1/8W 1% 1206	R127-134	PANASONIC	ERJ-8ENF6040V
104	4	1UF 20V 20% A	CT15-18	AVX	TAJA105K020R
105	1	255.0K 1/10W 1% 0603	R93	VISHAY	CRCW06032553FK
106	1	80.6K 1/10W 1% 0603	R91	DIGI-KEY	311-80.6KHRCT-ND
107	1	6.8UH 25% IND009	L2	DIGI-KEY	308-1328-1-ND

ADSP-21262 EZ-KIT Lite Schematic

ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

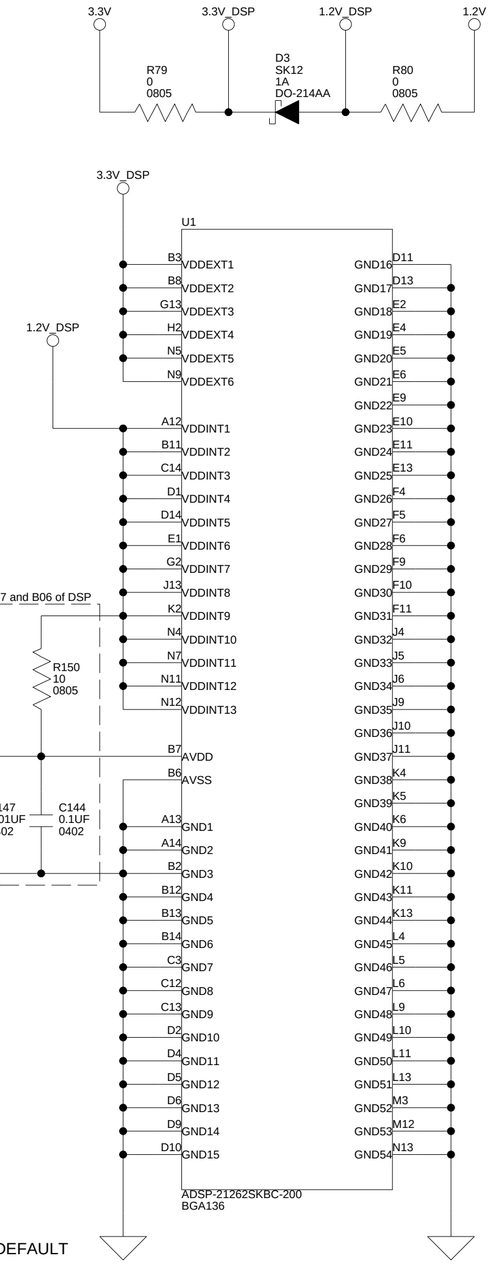
Title	ADSP-21262 EZ-KIT Lite TITLE		
Size C	**Board No.** A0174-2002		**Rev** 2.0C
Date 5-18-2007_14:12		**Sheet** 1 **of** 11	



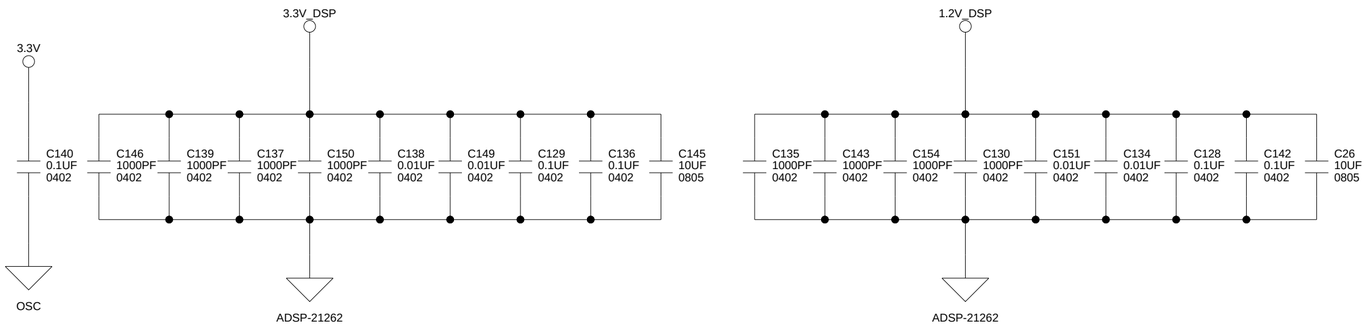
SW10: BOOT/CLOCK RATIO SELECT
(Default: 1=OFF, 2=ON, 3=OFF, 4=ON)

1 BOOTCFG0	2 BOOTCFG1	BOOTMODE
OFF	OFF	SPI SLAVE BOOT
ON	OFF	SPI MASTER BOOT
OFF	ON	PARALLEL PORT BOOT
ON	ON	RESERVED
3 CLKCFG0	**4 CLKCFG1**	**CLOCK RATIO CORE:CLKIN**
OFF	OFF	3:1
ON	OFF	16:1
OFF	ON	8:1
ON	ON	RESERVED

DEFAULT

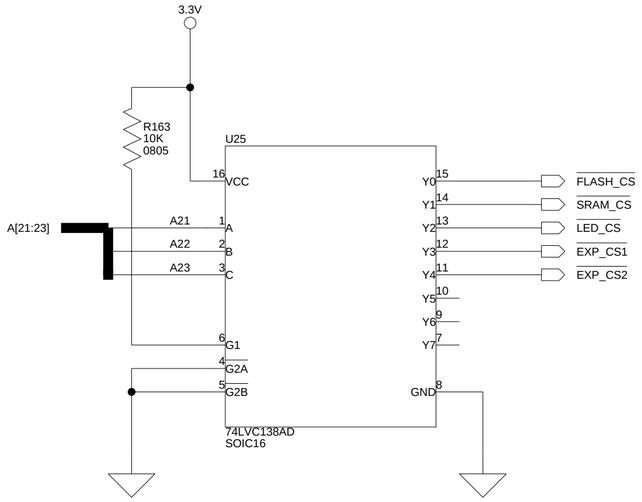


DEFAULT

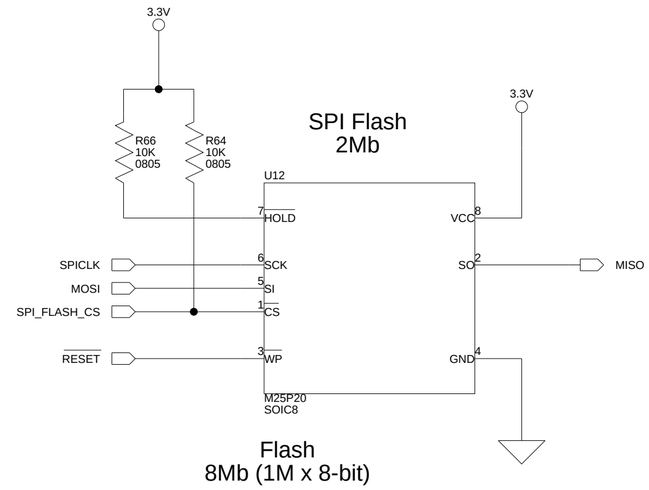


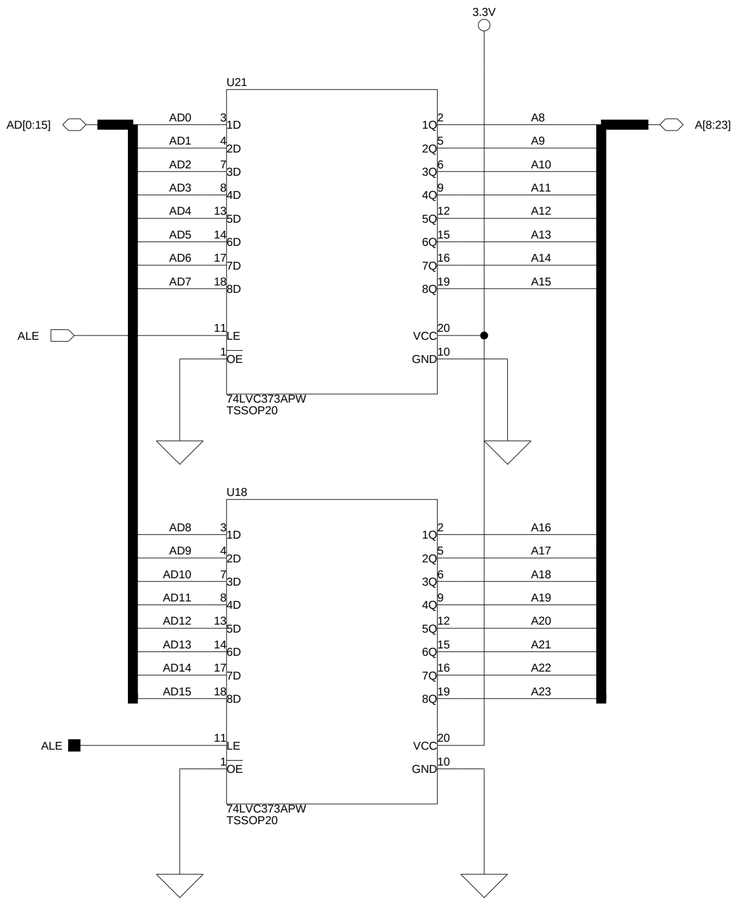
ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

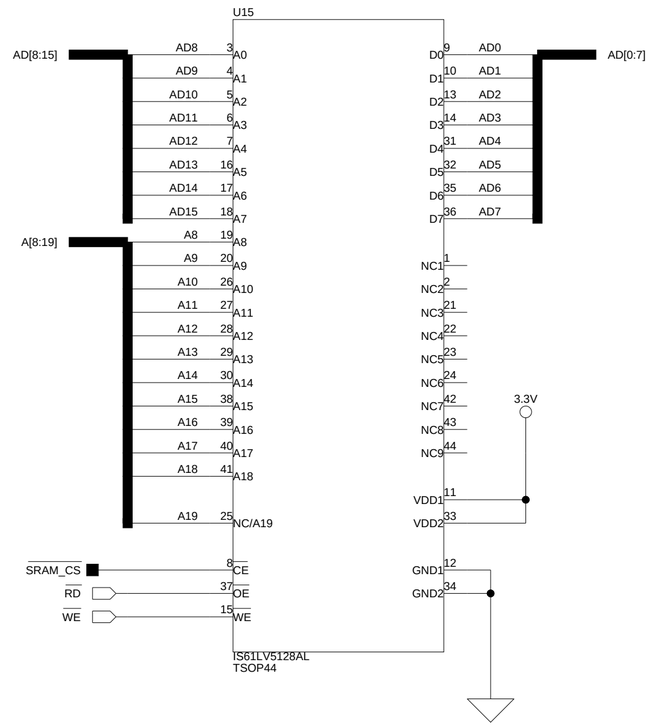
Title	ADSP-21262 EZ-KIT Lite DSP		
Size C	**Board No.** A0174-2002		**Rev** 2.0C
Date 5-18-2007_14:12		**Sheet** 2 **of** 11	

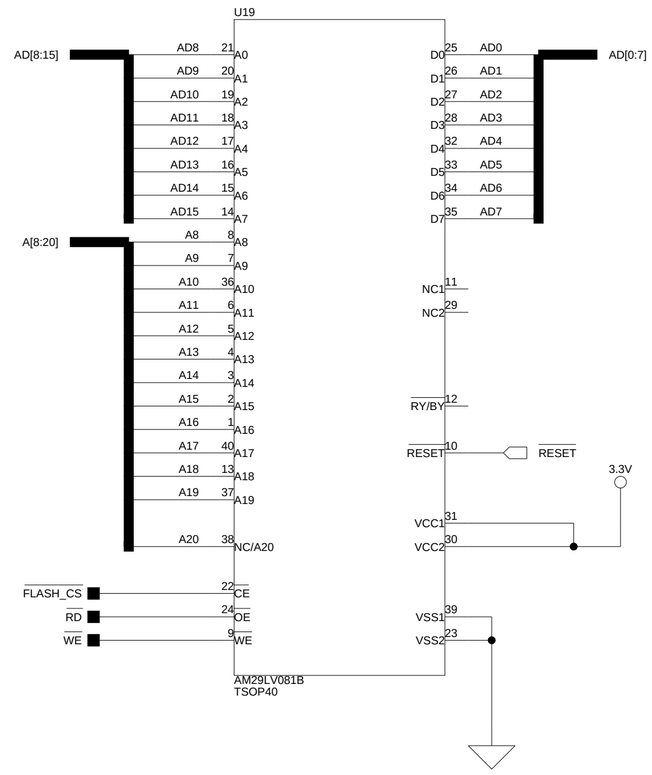


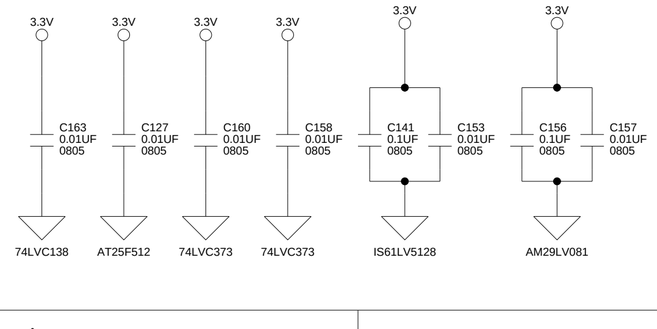
VALID DSP ADDRESS		BANK END	A23	A22	A21	BANK	DEVICE
START	END	ADDRESS					
1A0 0000	X	1FF FFFF	1	-	-	-	NONE
180 0000	X	19F FFFF	1	0	0	Y4	EXPANSION INTERFACE CS 2
160 0000	X	17F FFFF	0	1	1	Y3	EXPANSION INTERFACE CS 1
140 0000	140 0000	15F FFFF	0	1	0	Y2	LEDs
120 0000	127 FFFF	13F FFFF	0	0	1	Y1	SRAM
100 0000	10F FFFF	11F FFFF	0	0	0	Y0	FLASH



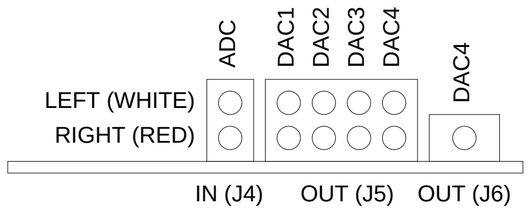




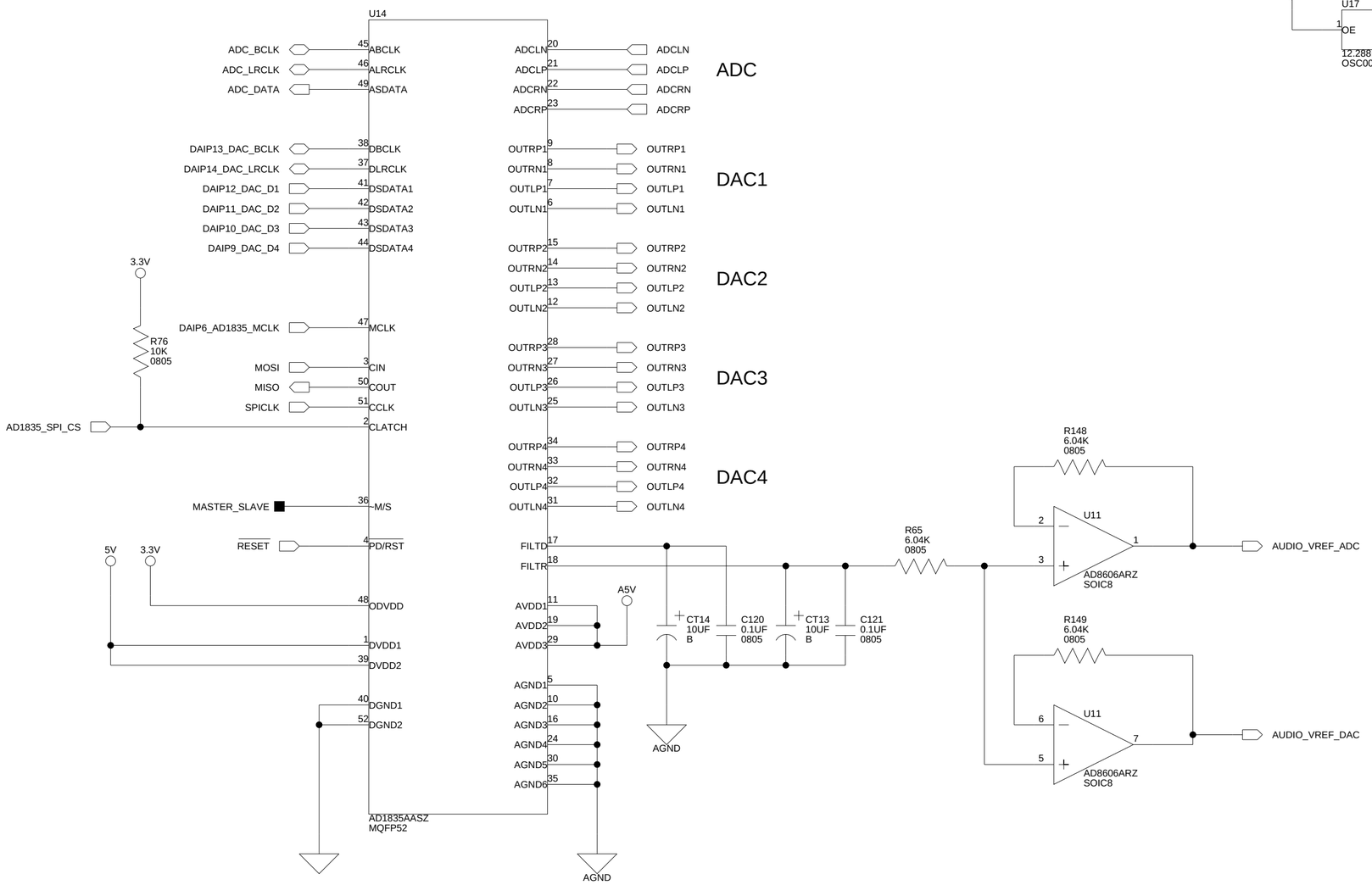


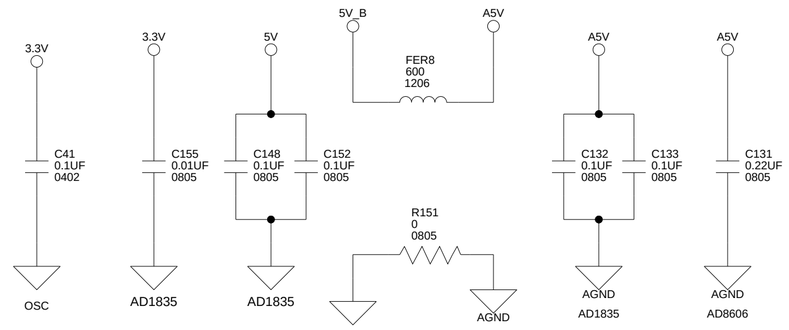


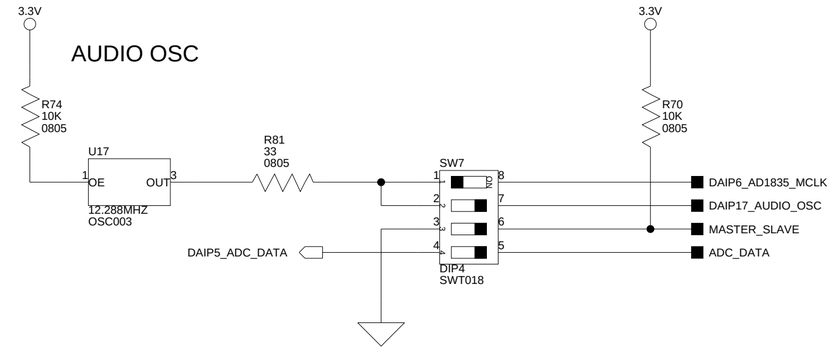
ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
Title	ADSP-21262 EZ-KIT Lite MEMORY	
Size C	**Board No.** A0174-2002	**Rev** 2.0C
Date 5-18-2007_14:12	**Sheet** 3 **of** 11	



AD1835 AUDIO CODEC







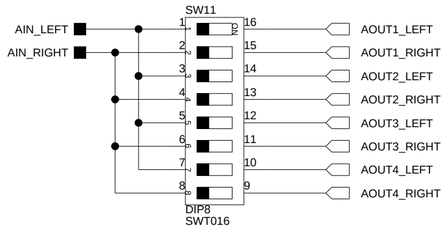
SW7: CODEC SETUP SWITCH
(Default: 1=OFF, 2=ON, 3=ON, 4=ON)

1-2	Connects or disconnects the audio oscillator depending on how the system is setup. See users manual for more information.
3	OFF = AD1835 is SLAVE ON = AD1835 is MASTER
4	Disconnects ADC_DATA signal from driving the corresponding DAI signal. Useful if using this DAI pin for another purpose.

DISCONNECTS SIGNALS FROM SPI FLASH AND AD1835

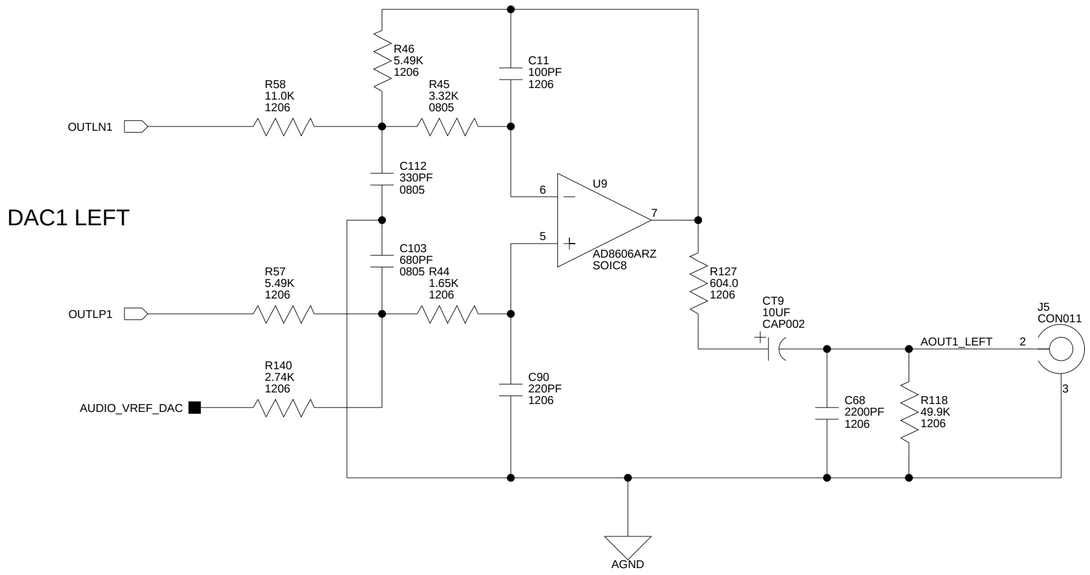
(Default= All ON)

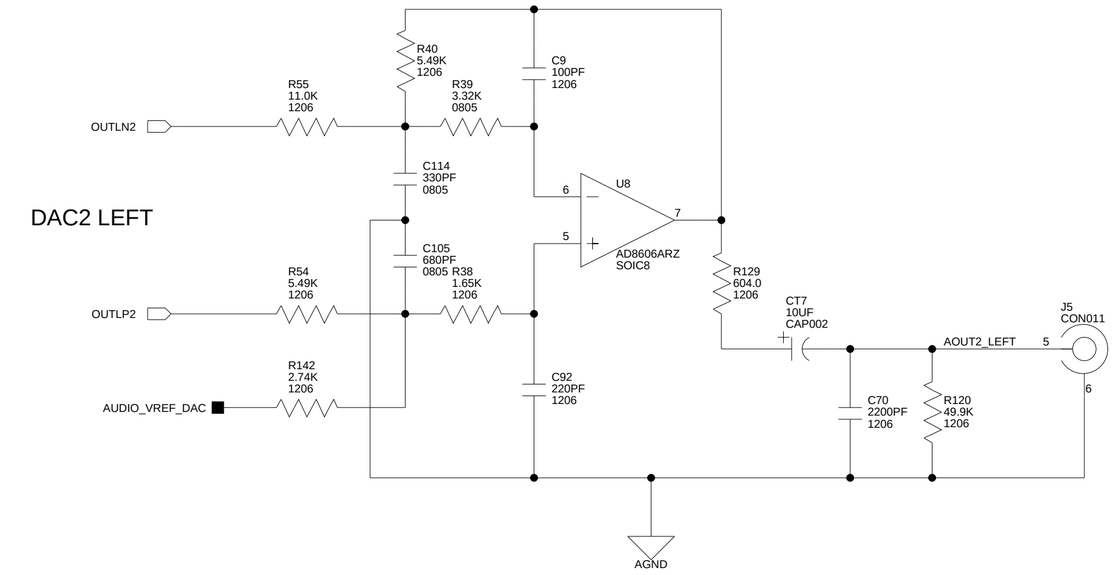
Loopback Test Switch
(Default= All OFF)
For Test Purposes Only

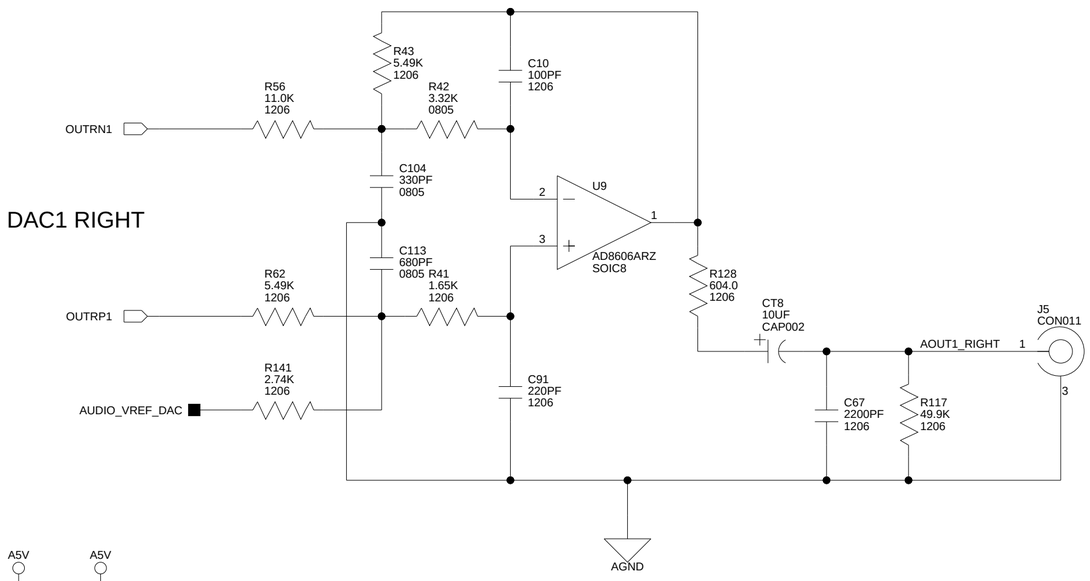


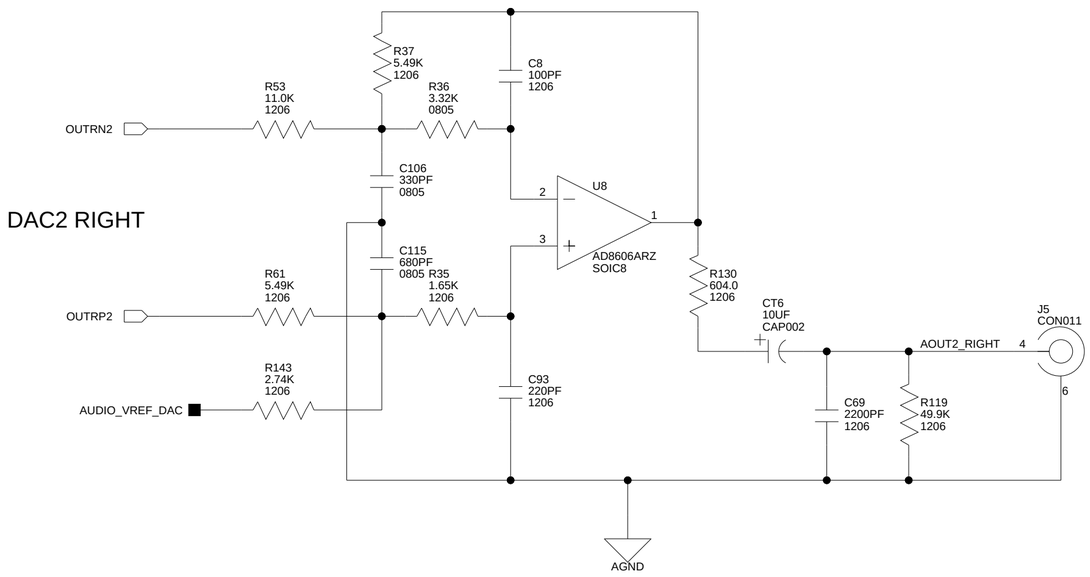
ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

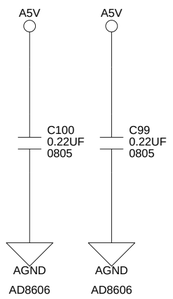
Title	ADSP-21262 EZ-KIT Lite ANALOG AUDIO	
Size: C	Board No.: A0174-2002	Rev: 2.0C
Date: 5-18-2007_14:12	Sheet: 4 of 11	





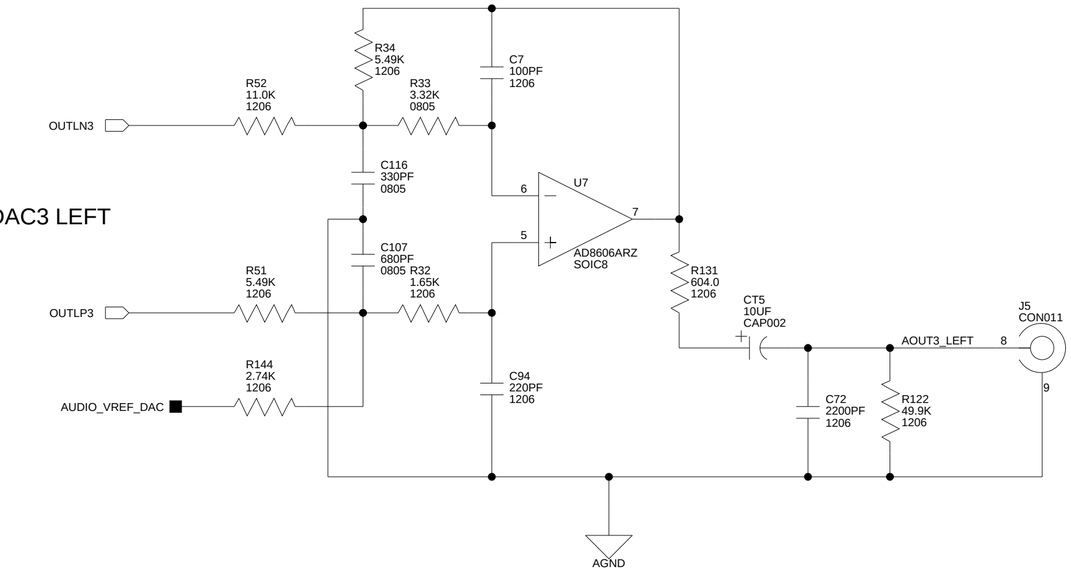




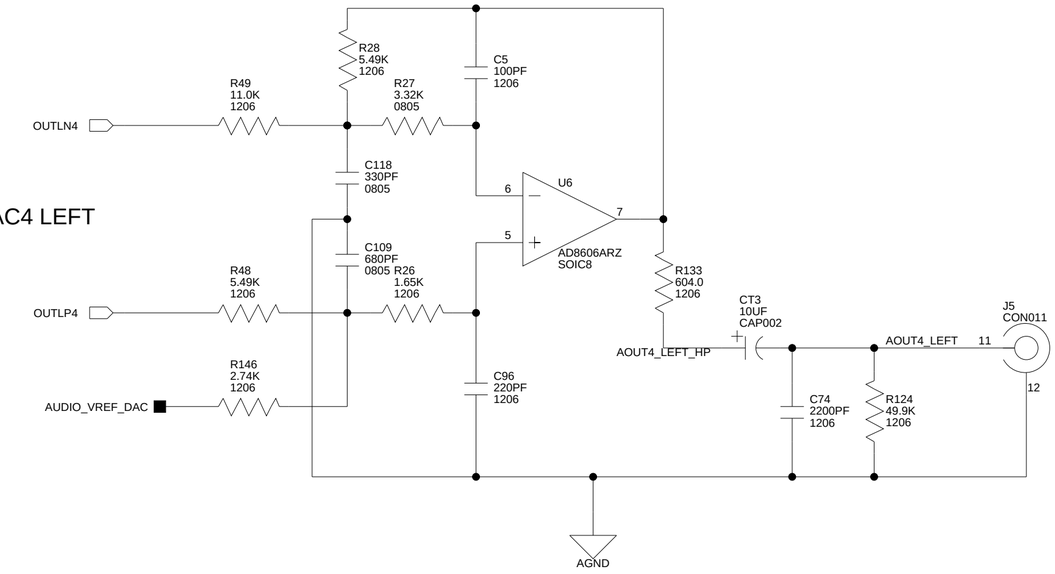


ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
Title	ADSP-21262 EZ-KIT Lite AUDIO OUT 1	
Size C	**Board No.** A0174-2002	**Rev** 2.0C
Date 5-18-2007_14:12	**Sheet** 5 **of** 11	

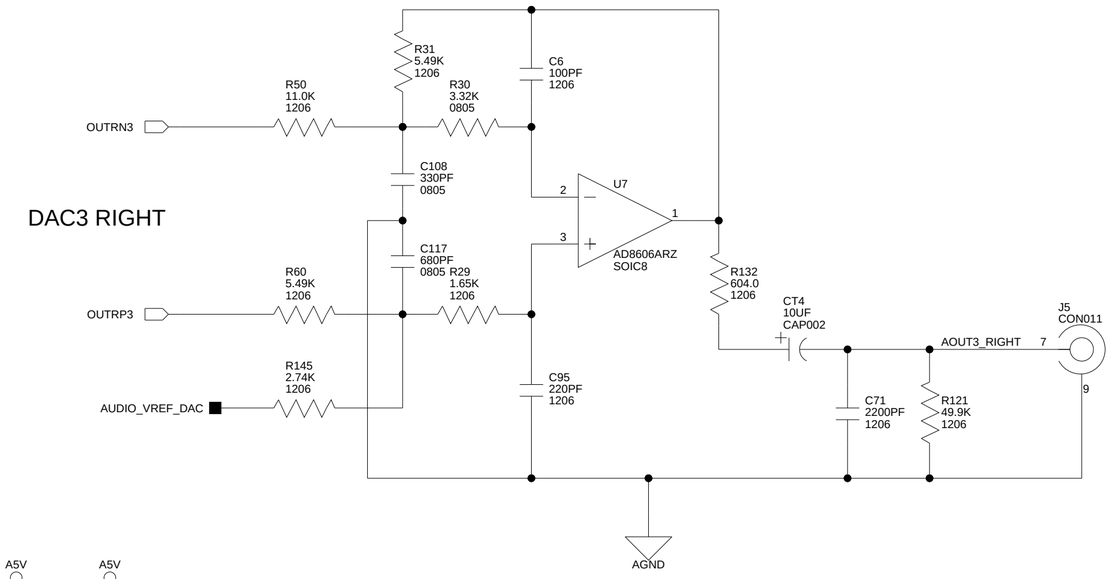
DAC3 LEFT



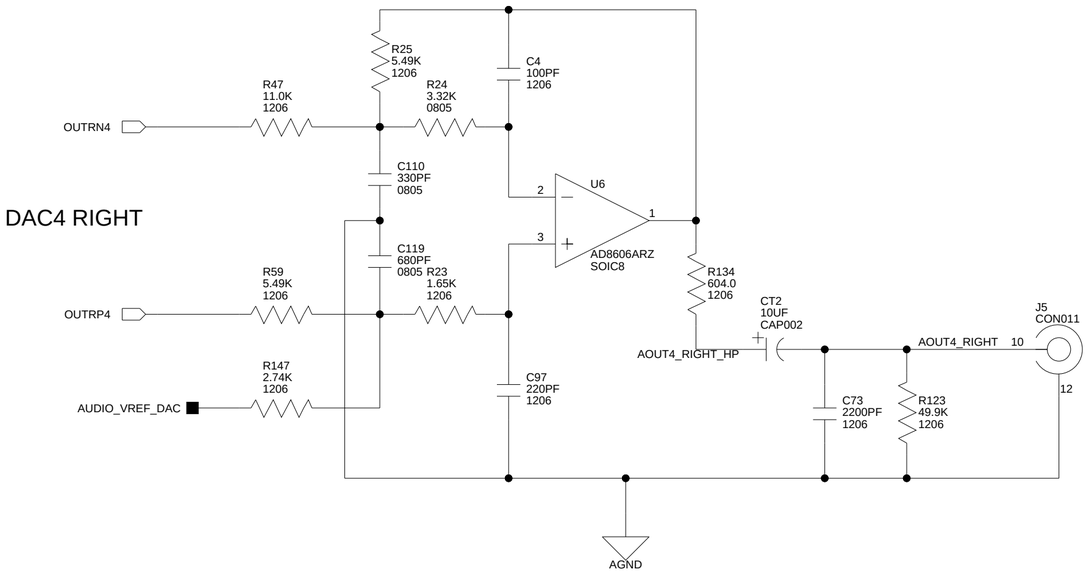
DAC4 LEFT

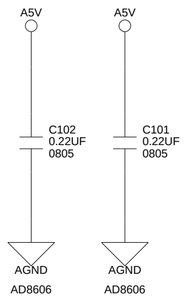


DAC3 RIGHT



DAC4 RIGHT





ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
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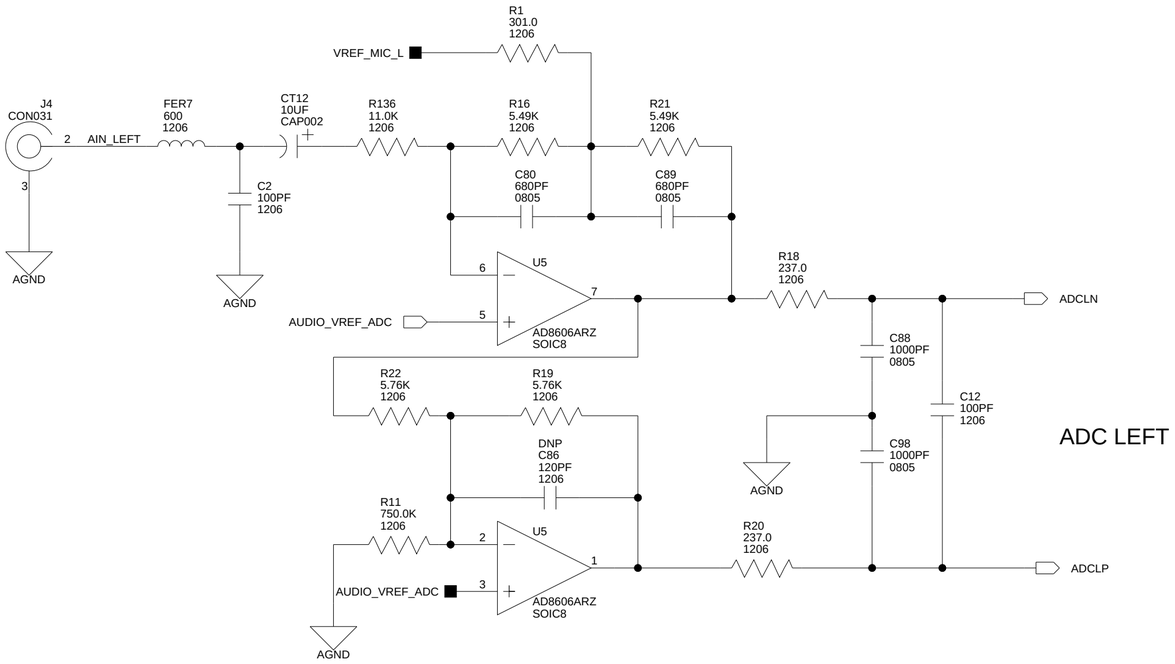
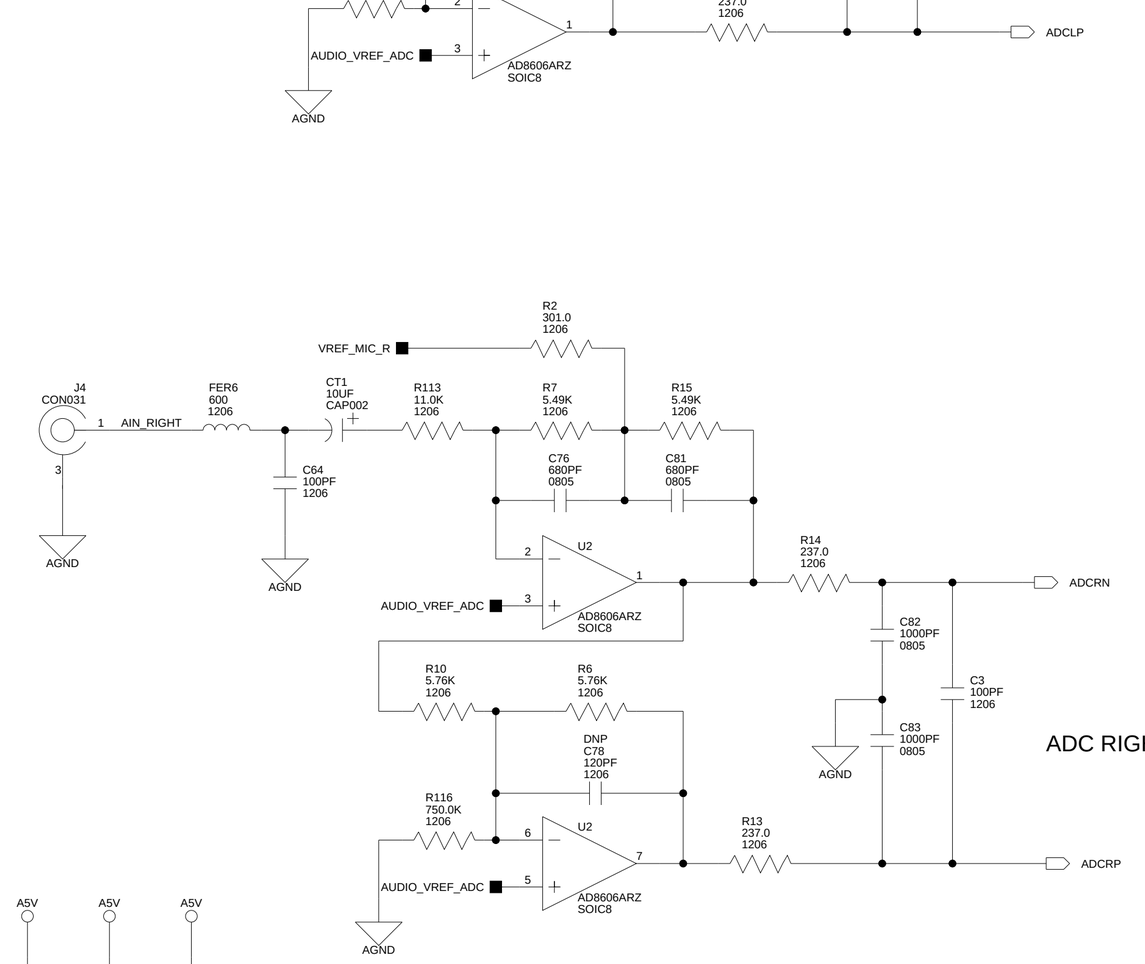
Title	ADSP-21262 EZ-KIT Lite AUDIO OUT 2		
Size C	**Board No.** A0174-2002		**Rev** 2.0C
Date 5-18-2007_14:12		**Sheet** 6 **of** 11	



ADC LEFT



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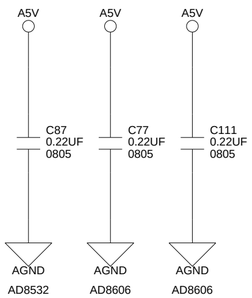
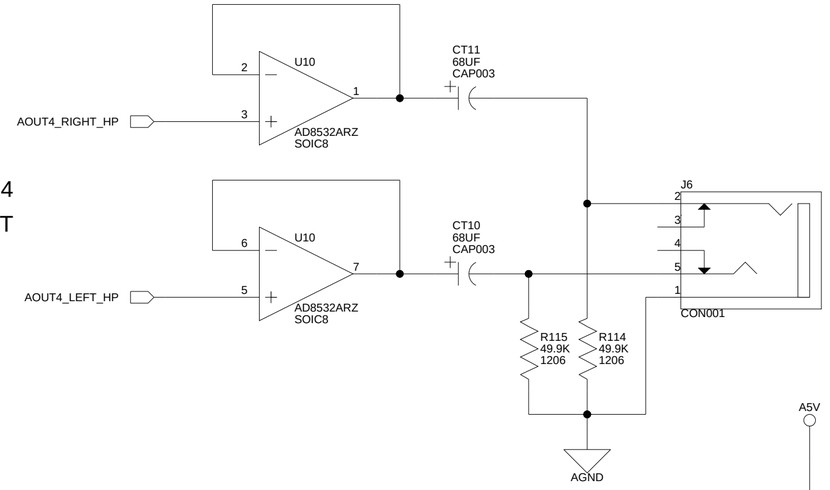
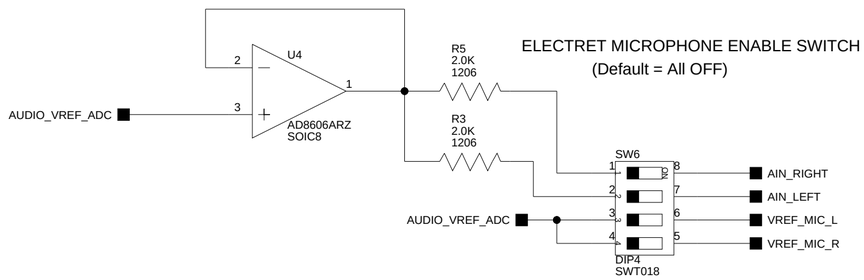


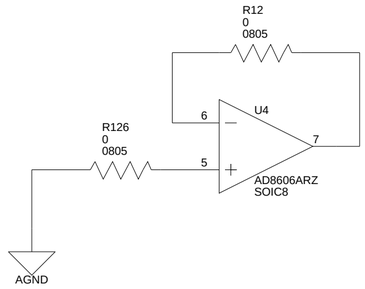
DAC4

HEADPHONE OUT





WHEN USING AN ELECTRET MICROPHONE
PLACE ALL SWITCHES IN ON POSITION



ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
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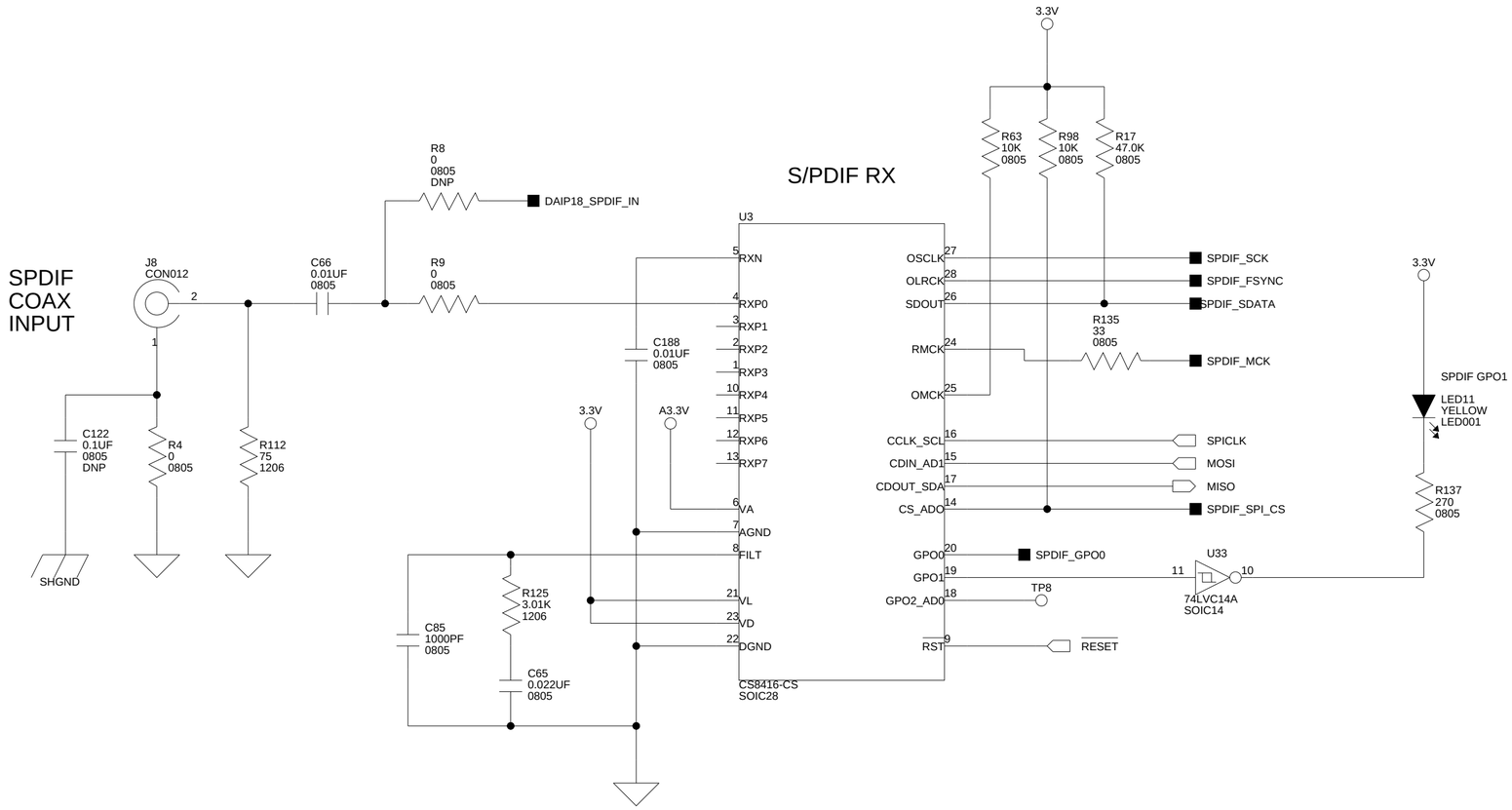
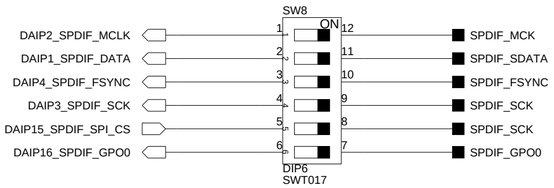
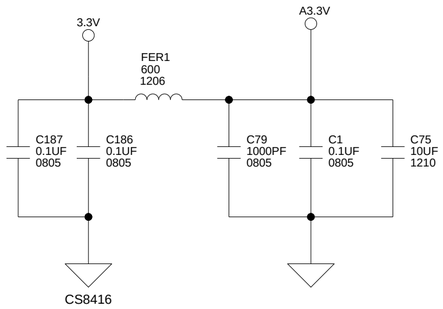
Title	ADSP-21262 EZ-KIT Lite AUDIO IN/HEADPHONE OUT	
Size C	**Board No.** A0174-2002	**Rev** 2.0C
Date 5-18-2007_14:12	**Sheet** 7 **of** 11	







SW8: SPDIF SIGNAL DISABLE
(Default: ALL = ON)

1-6	Used to disconnect signals of the SPDIF inteface from the corrisponding DAI signals. Useful if using DAI signals for another purpose.

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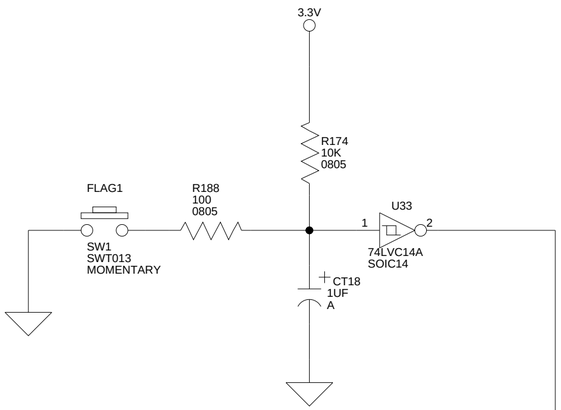
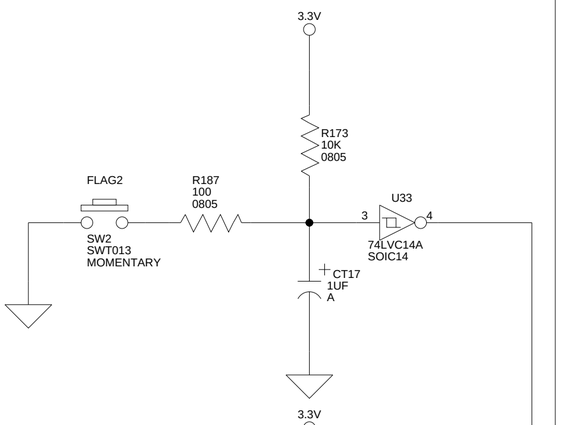
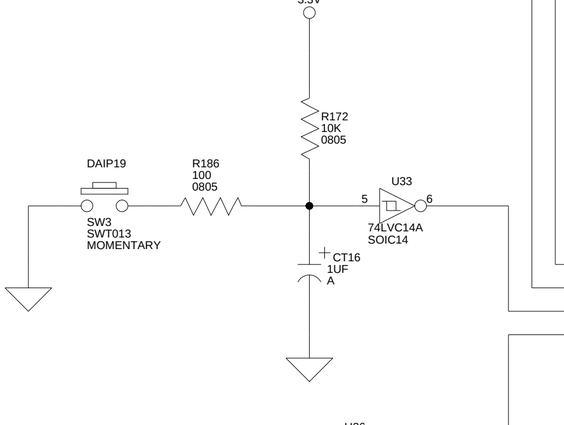
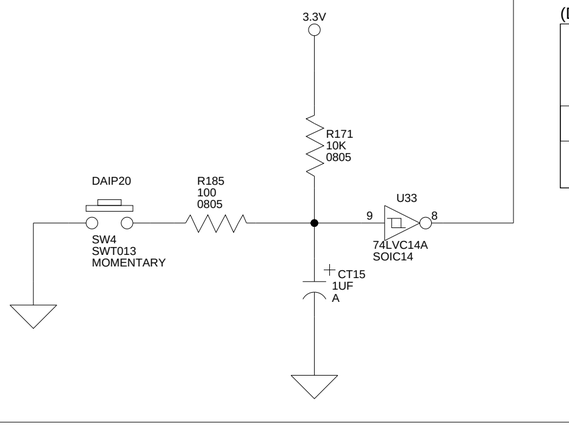
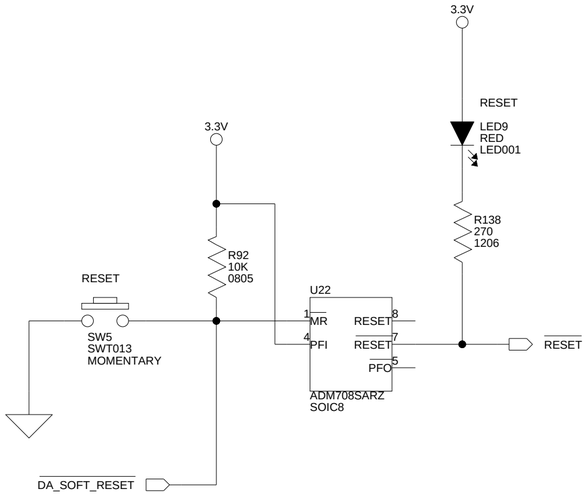
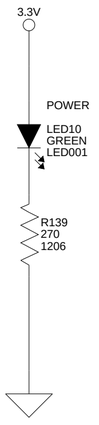


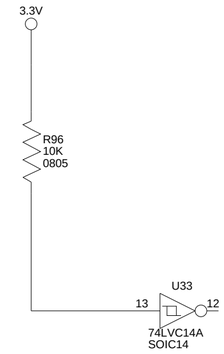


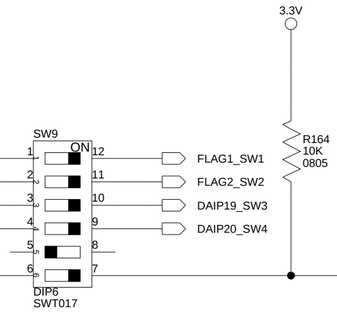


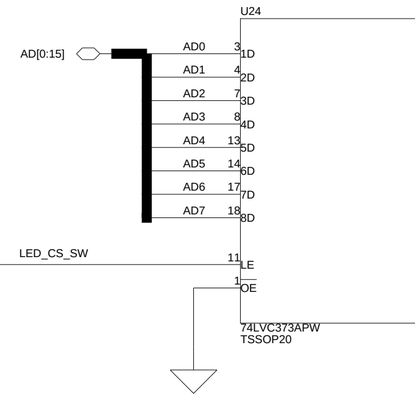


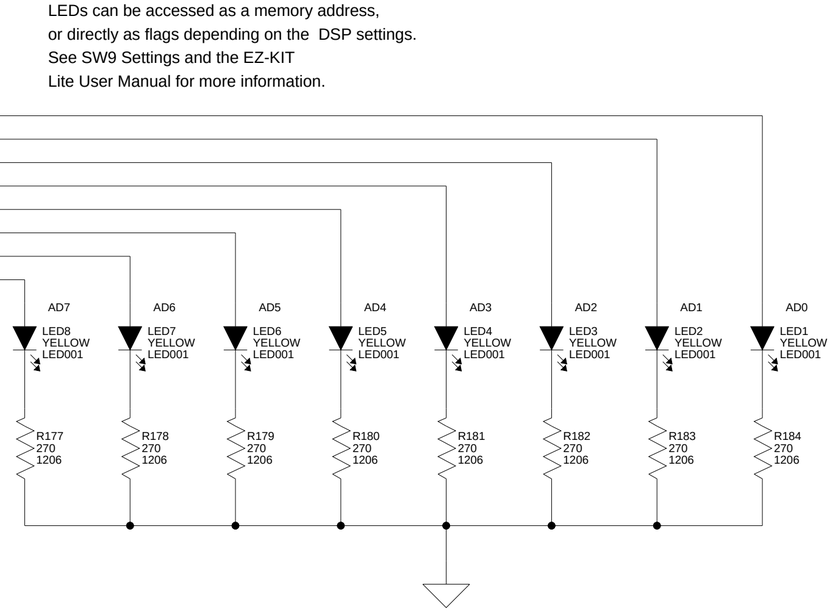








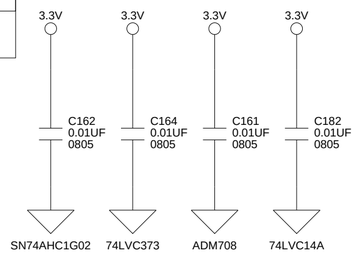




LEDs can be accessed as a memory address,
or directly as flags depending on the DSP settings.
See SW9 Settings and the EZ-KIT
Lite User Manual for more information.

SW9: PUSH BUTTON ENABLE SWITCH
(Default = All ON, except position 5)

1-4	Used to stop the pushbuttons from driving the corrisponding DSP signal. Useful if using these DSP signals for another purpose.
5	Not Used
6	OFF = LEDs function as flags ON = LEDs are accessed at a memory address



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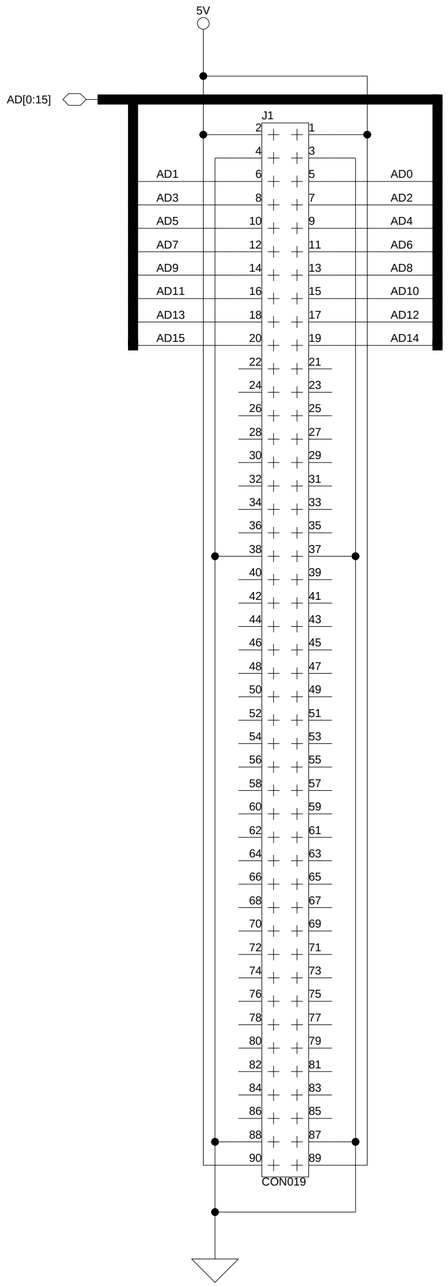
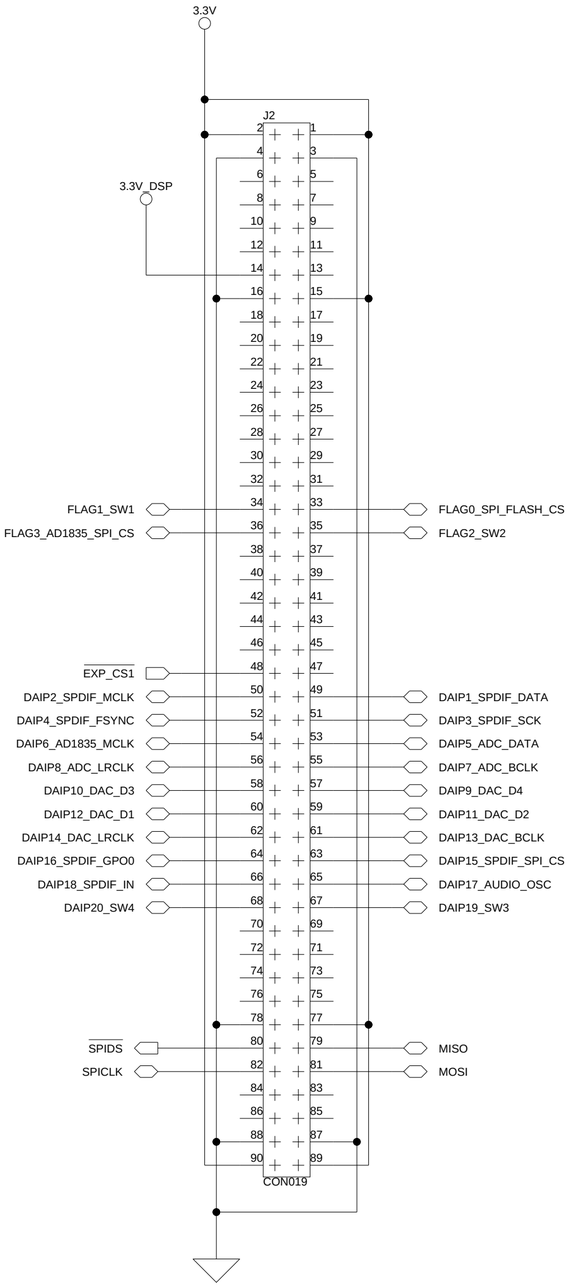
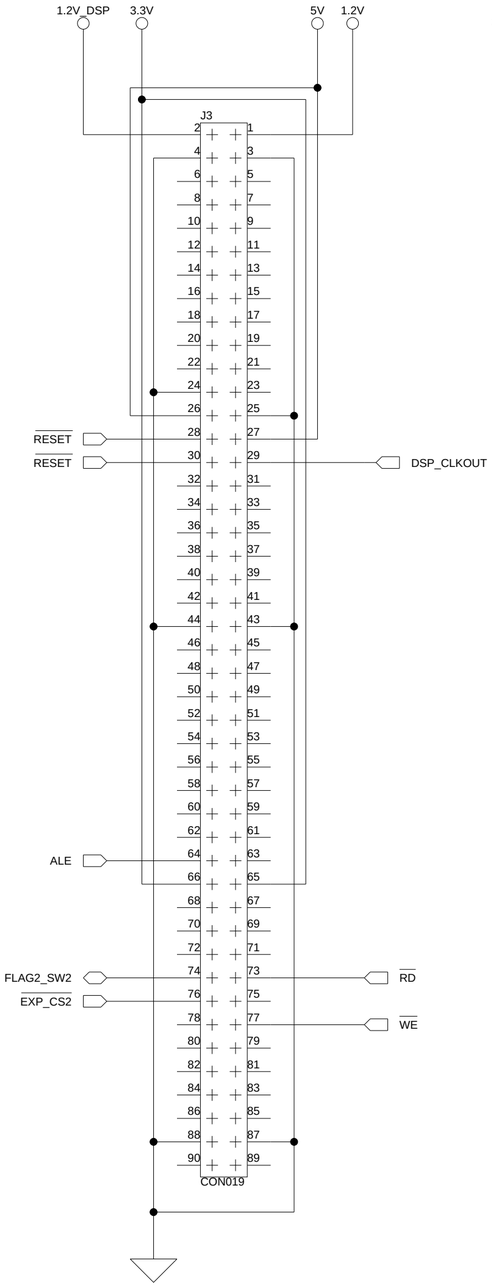
EXPANSION INTERFACE (TYPE A)



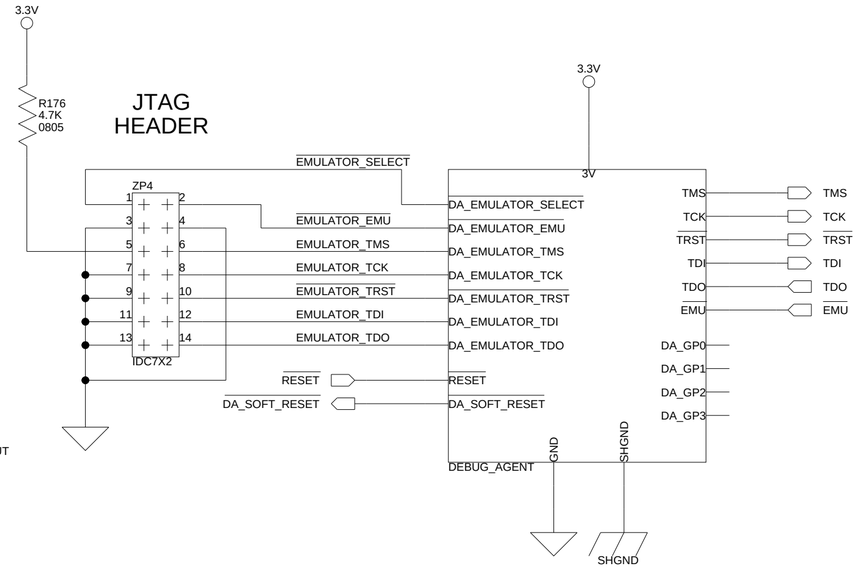




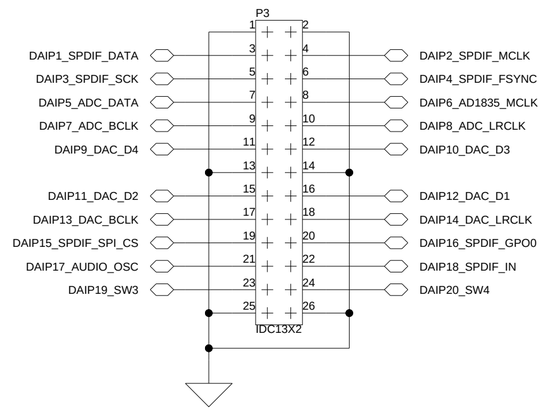
All USB interface circuitry is considered proprietary and has been omitted from this schematic.

When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at http://www.analog.com

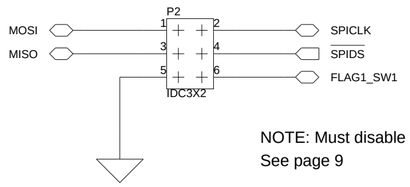
JTAG HEADER



DAI HEADER



SPI HEADER



NOTE: Must disable SW1 when using this pin as SPI select.
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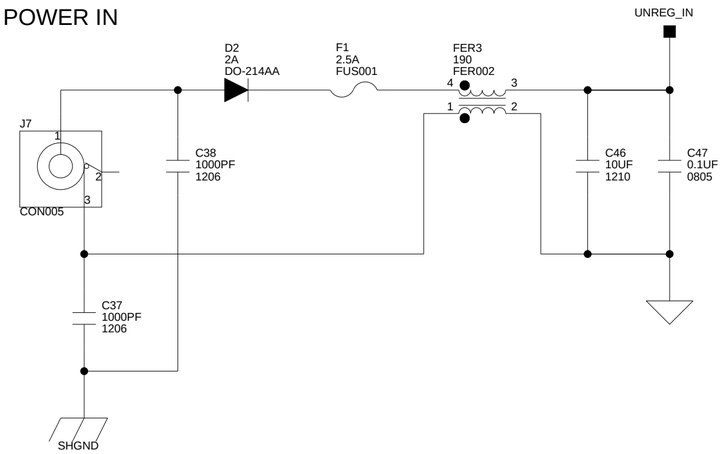
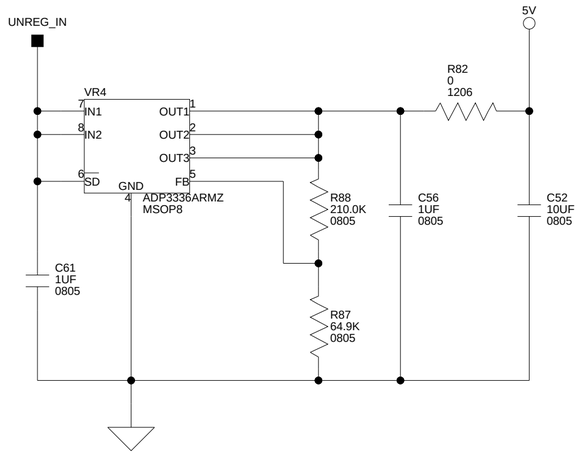
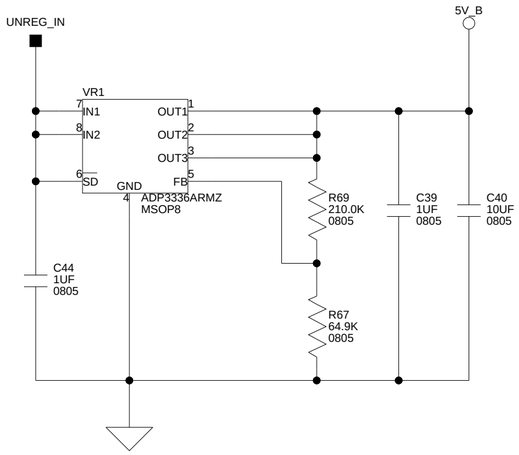
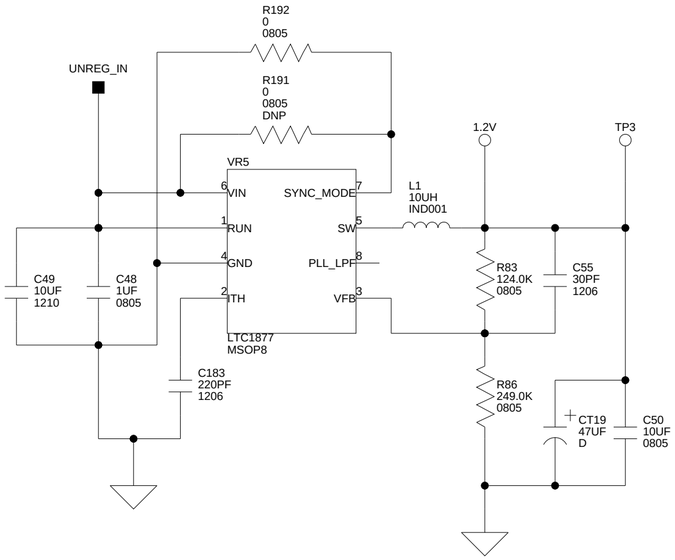
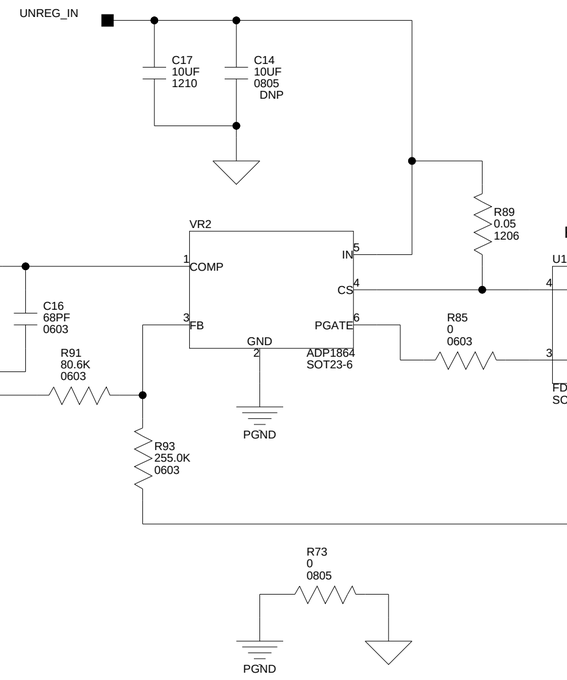
POWER IN

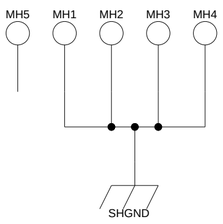


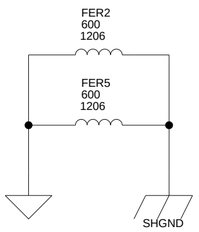


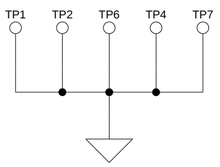












M5 RUBBER FOOT MSC009 | M1 RUBBER FOOT MSC009 | M2 RUBBER FOOT MSC009 | M3 RUBBER FOOT MSC009 | M4 RUBBER FOOT MSC009

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