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Estimating Power Dissipation for ADSP-21262S SHARC® DSPs

Contributed by C. Coughlin *December 2, 2003*

Introduction

This EE-Note discusses power consumption of the ADSP-21262S SHARC® DSPs based on characterization data measured over power supply voltage, core frequency (CCLK) and ambient operating temperature (T_A). The intent of this document is to assist board designers in estimating their power budget for power supply design and thermal relief designs using the ADSP-21262S DSP.

The ADSP-21262S DSP is a member of the SIMD SHARC family of DSPs featuring Analog Devices' Super Harvard Architecture. Like other SHARC DSPs, the ADSP-21262S is a 32-bit processor optimized for high-precision signal processing applications. The DSP operates at core clock frequencies up to 200MHz with the core operating at 1.2V (V_{DDINT}) and the I/O operating at 3.3V (V_{DDEXT}).

Total power consumption has two components: internal circuitry (i.e. the core and PLL) and switching of external output drivers (i.e. the I/O). The following sections detail how to derive both of these components for estimating total power consumption.

Estimating Internal Power Consumption

The internal power consumption (on the V_{DDINT} supply) is dependent on the instruction execution sequence and the data operands involved. The data sheet[2] provides current consumption figures for discrete activity levels. Mapping system application code to specified values provides a means of estimating internal power consumption for an ADSP-21262S DSP in a given application.

Internal Power Vector Definitions and Activity Levels

The following power vector definitions define the levels of activity that apply to the internal power vectors shown in Table 1:

- **$I_{DD-IDLE}$** V_{DDINT} supply current for Idle activity. Idle activity is the core executing the IDLE instruction only, without core memory accesses, DMA, or interrupts.
- **$I_{DD-INLOW}$** V_{DDINT} supply current for Low activity. Low activity is the core executing a single-function instruction fetched from internal memory with no core memory accesses and no DMA.
- **$I_{DD-INHIGH}$** V_{DDINT} supply current for High activity. High activity is the core executing a multifunction instruction fetched from internal memory, with 4 core memory accesses per CLKIN cycle (DMx64) and DMA through 3 SPORTs running @ 50MHz. The DMA is chained to itself (running continuously) and does not use interrupts. The bit pattern for each core memory access and DMA is random.
- **$I_{DD-INTYP}$** Same code as High activity, however, operating under nominal power

supply conditions (V_{DDINT} = 1.2V) and T_A = +25°C.

- **$I_{DD-INPEAK}$** V_{DDINT} supply current for Peak activity. Peak activity is the core executing a multifunction instruction fetched from internal memory and/or cache, with 8 core memory accesses per CLKIN cycle (DMx64, PMx64) and DMA through 6 SPORTs running @ 50MHz. The DMA is chained to itself (running continuously) and does not use interrupts. The bit pattern for each core memory access is random, and the DMA bit pattern is worst case.

Table 1 lists the maximum internal current consumption for the DSP at different levels of activity. These figures represent the worst case I_{DDINT} as measured across process, voltage, temperature, and frequency (PVTF). From these internal activity levels (and from an understanding of the program flow using profiling or some other method), you can calculate a worst-case weighted-average of power consumption for each ADSP-21262S DSP in a system.

Vector	**Test Conditions** (worst case except where noted) [1]	**I_{DDINT} (A)** [2]	**I_{DDINT} (A)** [3]
$I_{DD-IDLE}$	T_A = +70°C, V_{DDINT} = Max, CCLK = Max	0.70	0.70
$I_{DD-INLOW}$	T_A = +70°C, V_{DDINT} = Max, CCLK = Max	0.85	0.85
$I_{DD-INHIGH}$	T_A = +70°C, V_{DDINT} = Max, CCLK = Max	1.00	1.00
$I_{DD-INTYP}$	T_A = +25°C, V_{DDINT} = 1.2V, CCLK = 200MHz	0.50	0.50
$I_{DD-INPEAK}$	T_A = +70°C, V_{DDINT} = Max, CCLK = Max	1.26	1.06

Table 1: Maximum Internal Current Consumption per Vector Type

1 Worst-case conditions: T_J < +125°C, V_{DDEXT} = 3.47V, V_{DDINT} = 1.26V, CCLK = 200MHz; does not apply to $I_{DD-INTYP}$

2 Worst case across process, voltage, temperature and frequency (PVTF) for 136-ball mBGA package option. See "Estimating Total Power Consumption and Power Budget" for more information pertaining to the power budget and the mBGA package option.

3 Worst case across process, voltage, temperature and frequency (PVTF) for 144-lead LQFP package option. See "Estimating Total Power Consumption and Power Budget" for more information pertaining to the power budget and the LQFP package option.

Operation	**Low Activity**	**High Activity**	**Peak Activity**
Instruction Type	Single Function	Multifunction	Multifunction
Instruction Fetch	Internal Memory	Internal Memory	Internal Memory, Cache
Core Memory Access [4]	None	4 per t_{CK} cycle (DMx64)	8 per t_{CK} cycle (DMx64, PMx64)
DMA Transmit Int to Ext	N/A	3 SPORTs running @ 50 MHz	6 SPORTs running @ 50MHz
Data Bit Pattern for core Memory Access and DMA	N/A	Random	Worst case

Table 2: Activity Level Definitions

4 t_{CK} = CLKIN; Core clock ratio 8:1

Table 2 summarizes low, high and peak activity levels corresponding to the vectors listed in Table 1.

The average current consumption for an ADSP-21262S device in a specific application is calculated according to the following formula, where "%" is the percentage of the time that the application spends in that state.

% Peak Activity Level * $I_{DD-INPEAK}$

% High Activity Level * $I_{DD-INHIGH}$

% Low Activity Level * $I_{DD-INLOW}$

% Idle Activity Level * $I_{DD-IDLE}$

Total Current for V_{DDINT} (I_{DDINT})

Equation 1: Internal Current (IDDINT) Calculation

Estimated average internal power consumption (P_{DDINT}) can then be calculated as follows:

$$P_{DDINT} = V_{DDINT} \times I_{DDINT}$$

Equation 2: Internal Power (PDDINT) Calculation

For example, after profiling the application code for a particular system, activity is determined to be proportioned a:

Peak Activity Level 30%

High Activity Level 30%

Low Activity Level 20%

Idle Activity Level 20%

Example 1: Internal System Activity Levels

Using the percentages in this example and the currents provided for each activity level in Table 1 (mBGA package used for this example), a value for the worst case average internal current consumption of a single processor is estimated as follows:

30% * 1.26

30% * 1.00

20% * 0.85

20% * 0.70

I_{DDINT} = 0.988 A

Example 2: Internal Current Estimation Example

Therefore, an estimate of the average internal power for the processor can be calculated from Example 2 as follows:

P_{DDINT} = 1.20 V x 0.988 A = 1.1856 W

Example 3: Internal Power Estimation

Estimating External Power Consumption

The external power consumption (on the V_{DDEXT} supply) is dependent on the switching of the output pins. The magnitude of the external power depends on:

- The number of output pins (O) that switch during each cycle
- The maximum frequency (f) at which the output pins can switch
- The voltage swing of the output pins (V_{DDEXT})
- The load capacitance of the output pins (C_L)

In addition to the input capacitance of each device connected to an output, the total load capacitance includes the capacitance (C_{OUT}) of the DSP pin itself which is driving the load. The parallel port address/data pins (AD15-0) can transfer data at 1/3 the DSP core clock rate. This corresponds to a maximum switching frequency of 33MHz for AD15-0 and 66MHz for /WR at a core clock rate of 200MHz. In addition, the serial ports can operate up to 1/8 the DSP core clock rate. This corresponds to a maximum switching frequency of 12.5MHz for SDATA and a

maximum switching frequency of 25MHz for SCLK at a core clock rate of 200MHz.

Equation 3 shows how to calculate the average external current (I_{DDEXT}) using the above parameters:

$$I_{DDEXT} = O \times f \times V_{DDEXT} \times C_L$$

Equation 3: External Current (IDDEXT) Calculation

Estimated average external power consumption (P_{DDEXT}) can then be calculated as:

$$P_{DDEXT} = V_{DDEXT} \times I_{DDEXT}$$

Equation 4: External Power (P_{DDEXT}) Calculation

Using the sample configuration shown in Figure 1, we can estimate the external current and thereby the external power consumption with the following assumptions:

- DSP core running at 200MHz (CCLK)
- 64K x 16-bit external memory, C_L = 10pF [9]
- 16-bit external latch (used to hold the address when accessing external memory), C_L = 10pF [5]
- AD15-0 can transfer data at a rate of 1/3 * CCLK, with 50% of the pins switching
- External memory write cycles can occur at a rate of 1/6 * CCLK (32-bit transfer to 16-bit external memory)
- DAI configured to transmit and receive 32-bit words at 1/8 * CCLK, C_L = 10pF [5]
- Output capacitance of DSP pin, C_{OUT} = 4.7pF

Using Equation 3, I_{DDEXT} can then be calculated for each class of pins that can drive as shown in Table 3.

[9] Trace capacitance is ignored

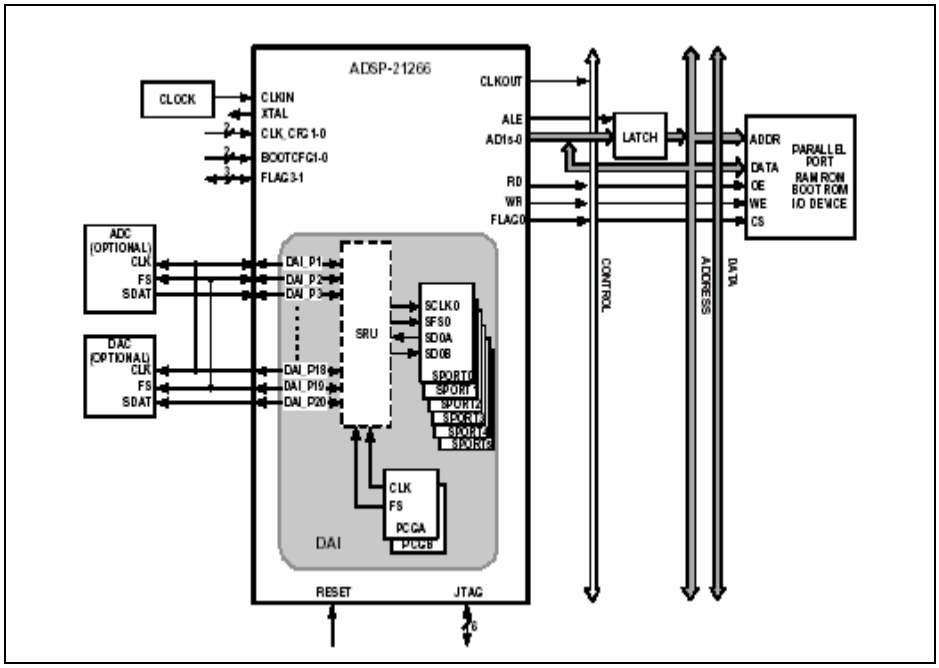


Figure 1: ADSP-2126x System Sample Configuration

Pin Type	No. of Pins	Switching (%)	F (MHz)	V_{DDEXT} (V)	C (pF)	I_{DDEXT} (A)
AD15-0	16	50	66.67	3.3V	4.7 + (2 x 10)	0.0434
$\overline{RD}$	1	0	n/a	3.3V	4.7 + (1 x 10)	0.0000
$\overline{WR}$	1	100	33.33	3.3V	4.7 + (1 x 10)	0.0016
ALE	1	100	33.33	3.3V	4.7 + (1 x 10)	0.0016
FLAG0	1	0	n/a	3.3V	4.7 + (1 x 10)	0.0000
DAI_P18 (SCLK)	1	100	50	3.3V	(2 x 4.7) + (2 x 10)	0.0048
DAI_P19 (FS)	1	100	1.5	3.3V	(2 x 4.7) + (2 x 10)	0.0001
DAI_P20 (SDATA)	1	100	25	3.3V	4.7 + (1 x 10)	0.0012

Table 3: External Current (I_{DDEXT}) Summary for Figure 1.

Summing the individual currents from Table 3, the total external current (I_{DDEXT}) for the example configuration shown in Figure 1 is 0.0527 A. Using this current, the estimated average external power can then be calculated as:

$$\mathbf{P_{DDEXT} = 3.3\ V \times 0.0527\ A}$$

$$\mathbf{= 0.1739\ W}$$

Example 4: External Power (P_{DDEXT}) Calculation

At T_A = +70°C, the P_{TOTAL} for any ADSP-2126x should not exceed 1.95W in the mBGA or 1.69W in the LQFP package for proper DSP operation. Power consumption greater than these limits (1.95W or 1.69W) could result in permanent damage to the DSP.

$$\mathbf{T_J = P_{TOTAL} \times \theta_{JA} + T_A}$$

Equation 5: Junction Temperature (T_J) Calculation

Table 4 contains examples of power supply currents that satisfy the total power budget for an ADSP-2126x DSP in an mBGA package operating at T_A = +70°C. Power is calculated using V_{DDMAX} for each power supply:

I_{DDINT} (A)	I_{DDEXT} (A)	AI_{DD} (A)	P_{DDINT} (W)	P_{DDEXT} (W)	P_{PLL} (W)	P_{TOTAL} (W)
0.9	0.231	0.01	1.134	0.8016	0.0126	1.95
1.0	0.195	0.01	1.260	0.6774	0.0126	1.95
1.1	0.159	0.01	1.386	0.5514	0.0126	1.95
1.2	0.123	0.01	1.512	0.4254	0.0126	1.95

Table 4: Power Supply Currents and Total Power Budget

** Note: the total power budget (P_{TOTAL}) can be increased by reducing the ambient operating temperature (T_A). However, the user must insure that the maximum junction temperature (T_J), as defined by Equation 6, does not exceed +125°C.

For additional information regarding the power budget and its relationship to the thermal characteristics of the ADSP-2126x DSP, see the Thermal Characteristics section of ADSP-2126x data sheet.

Estimating Total Power Consumption and Power Budget

For a particular system, the total power budget is equal to the sum of the individual components:

$$P_{TOTAL} = P_{DDINT} + P_{DDEXT} + P_{PLL}$$

Equation 6: Total Power (P_{TOTAL}) Calculation

where:

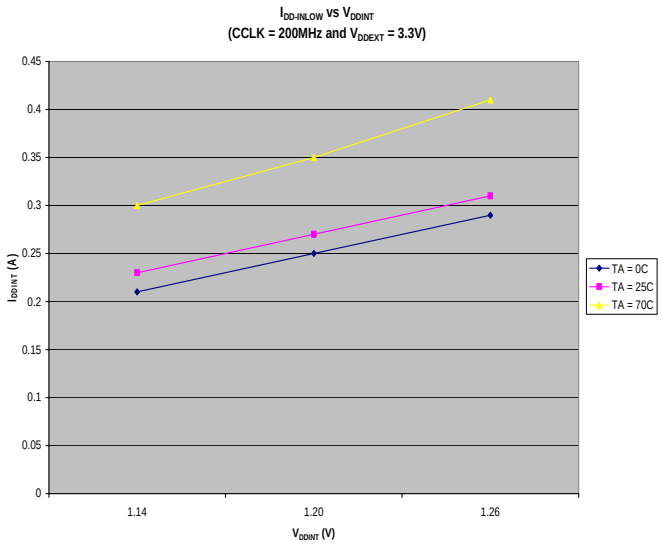
P_{DDINT}	Average internal power consumption as defined by Equation 2
P_{DDEXT}	Average external power consumption as defined by Equation 4
P_{PLL}	Power consumption due to the PLL as defined by (AI_{DD} x AV_{DD}) where the max value for AI_{DD} and AV_{DD} is listed in the data sheet

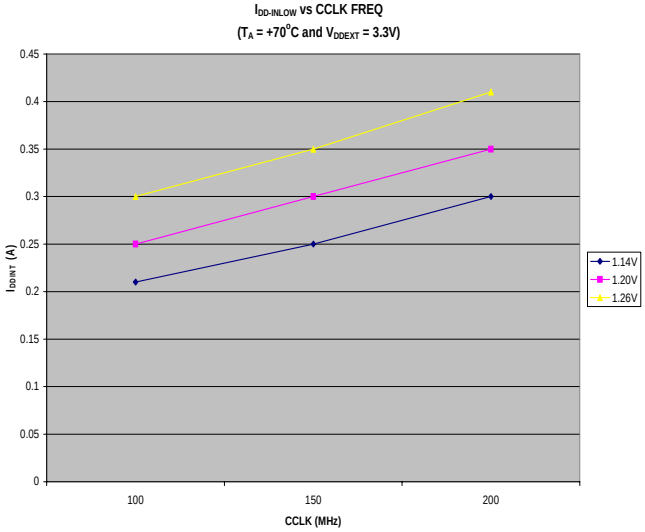
For ADSP-2126x DSPs, the total power budget is limited to 1.95W (mBGA package) and 1.69W (LQFP package). The power budget is determined by the package thermal resistance (θ_{JA}), 28.2°C/W for the mBGA and 32.5°C/W for the LQFP, a maximum operating temperature (T_A) of +70°C and a maximum junction temperature (T_J) of +125°C. Equation 5 shows the relationship between these three parameters and power:

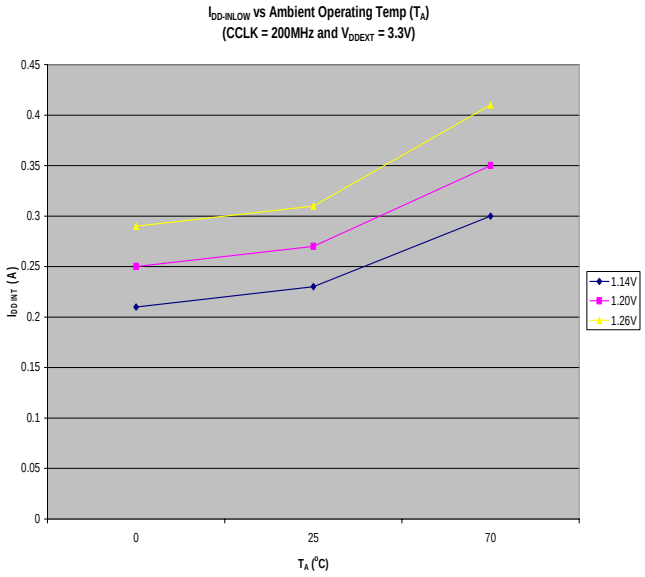
I_{DDINT} versus Voltage, Frequency and Operating Temperature

The following section contains graphs of I_{DDINT} for various activity levels versus the specified ranges of processor core voltage (V_{DDINT}), operating frequency (CCLK) and ambient operating temperature (T_A). Each of these curves represent the mean value for I_{DDINT} across process, voltage, temperature and frequency (PVTF). These graphs provide the system designer with data showing the effect of core voltage, processor operating frequency and ambient operating temperature on internal power consumption (**P_{DDINT}**). With this information, a system can be designed to meet the power budget requirements of an ADSP-2126x DSP as discussed in the previous section of this EE-Note.

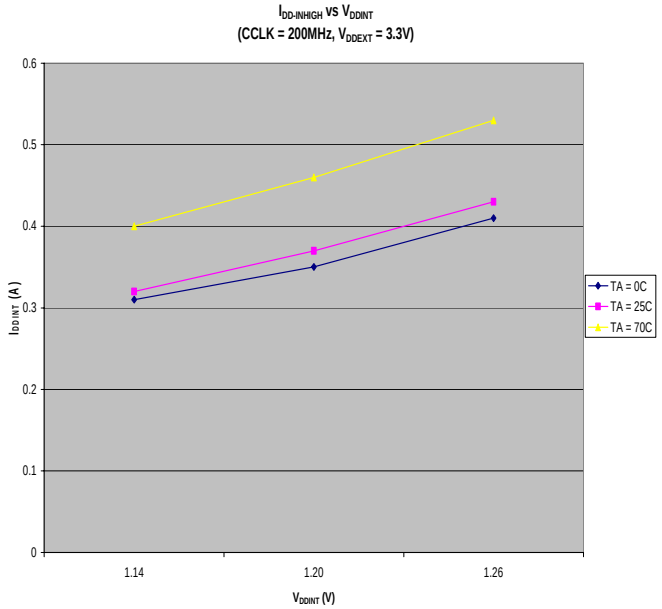
$I_{DD\text{-}INLOW}$ versus. Voltage, Frequency and Operating Temperature



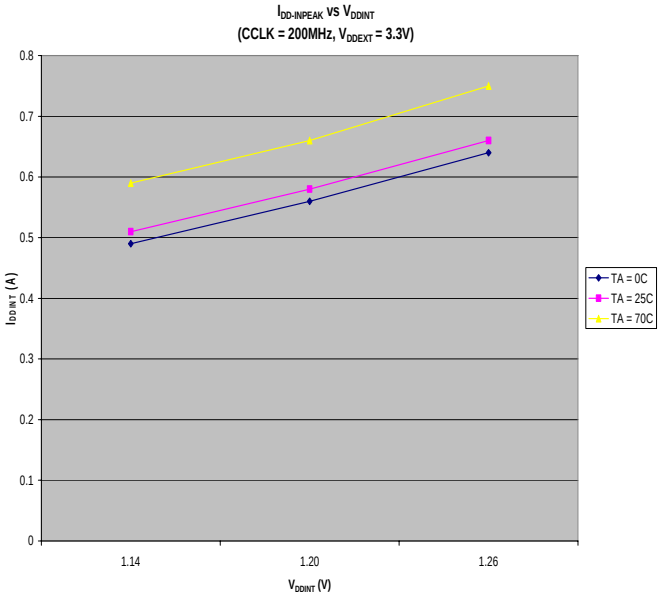


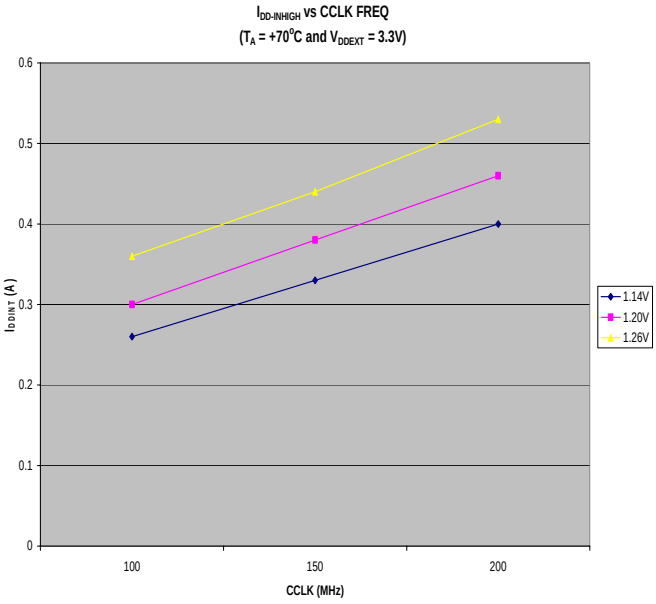


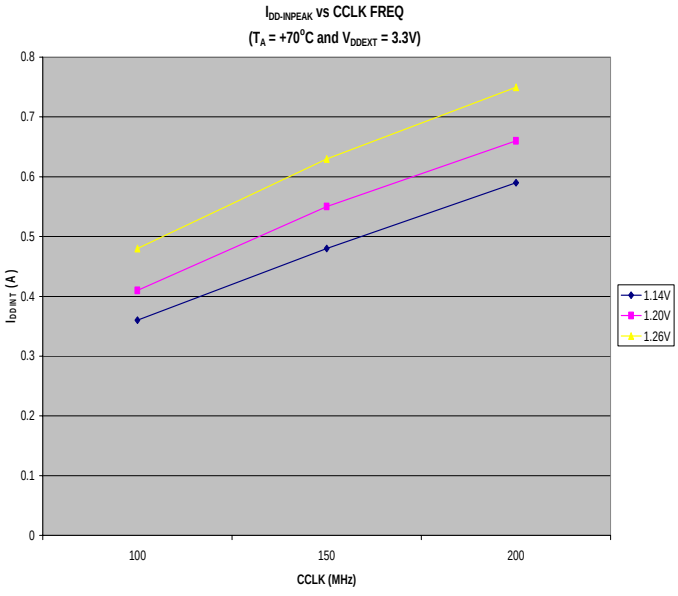
$I_{DD\text{-}INHIGH}$ versus Voltage, Frequency and Operating Temperture

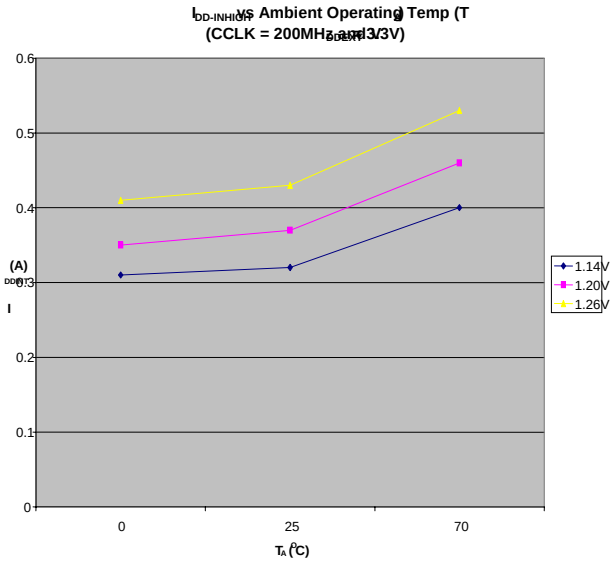


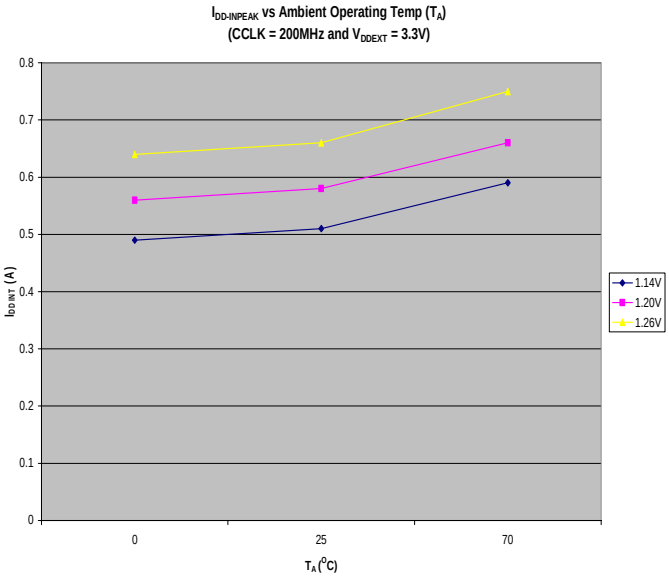
$I_{DD\text{-}INPEAK}$ versus Voltage, Frequency and Operating Temperature











References

[1] ADSP-2126x SHARC DSP Hardware Reference. December 2003. Analog Devices, Inc.

[2] ADSP-21262 SHARC DSP Microcomputer Data Sheet. Rev. 0. December 2003. Analog Devices, Inc.

Document History

Version	Description
December 02, 2003 by R. Murphy	Initial Release