

ABOUT ADSP-21266 SILICON ANOMALIES

These anomalies represent the currently known differences between revisions of the SHARC ADSP-21266 product and the functionality specified in the ADSP-21266 data sheets and the Hardware Reference books.

SILICON REVISIONS

A silicon revision number with the form "-x.x" is branded on all parts (see the data sheet for information on reading part branding). The silicon revision can also be electronically read by reading the **REVPID** register either via JTAG or DSP code.

The following DSP code can be used to read the register:

```
<UREG> = REVPID;
```

Silicon REVISION	REVPID[7:4]
0.2	0010

ANOMALY LIST REVISION HISTORY

The following revision history lists the anomaly list revisions and major changes for each anomaly list revision.

Date	Anomaly List Revision	Data Sheet Revision	Additions and Changes
12/28/2006	I	B	Removed anomalies: 06000027 - This information is added to the HRM
11/24/2006	H	B	Added anomalies: 06000027
10/17/2006	G	B	Document Format update
08/17/2006	F	B	Modified anomalies: 06000012
06/21/2006	E	B	Modified anomalies: 06000022
03/14/2006	D	B	Added anomalies: 06000022

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SUMMARY OF SILICON ANOMALIES

The following table provides a summary of ADSP-21266 anomalies and the applicable silicon revision(s) for each anomaly.

No.	ID	Description	0.2
1	06000006	FLG0-3 pins are unusable when CLK source for SPI Module is disabled	x
2	06000009	Type 1 Instruction (Dual-access) failing if reference is to a memory mapped register	x
3	06000012	Incorrect number of loop iterations for counter based loops with PMDA access	x
4	06000016	Conditional RTI in SIMD not evaluated properly	x
5	06000018	Pin Sensitivity (RD_B, DAI_P[20:1])	x
6	06000020	Indirect jumps or calls followed by Long Word accesses using PM bus can vector to an unknown location	x
7	06000021	Parallel Port Bus Contention	x
8	06000022	SPI can generate spurious clock for an additional word when used in receive DMA mode at maximum SPICLK frequency	x

Key: x = anomaly exists in revision
 . = Not applicable

DETAILED LIST OF SILICON ANOMALIES

The following list details all known silicon anomalies for the ADSP-21266 including a description, workaround, and identification of applicable silicon revisions.

1. 06000006 - FLG0-3 pins are unusable when CLK source for SPI Module is disabled:

DESCRIPTION:

The ADSP-2126x DSP gives the user the ability to disable the on chip core clock to various peripheral modules in order to conserve power. This is configured in the PMCTL register. When the clock signal for the SPI module is disabled, the pins* for FLG0-3 are unusable until the clock is re-enabled. These pins are used by the SPI module as device selects in SPI Master mode.

*Note that the FLG0-3 pins share functionality with other signals, configurable in the SYSCTL Register. Pin function is as follows: FLG0 or IRQ0, FLG1 or IRQ1, FLG2 or IRQ2, FLG3 or TIMEXP. For more details on this functionality please consult the System Design Chapter of the ADSP-2126x Hardware Reference Manual.

WORKAROUND:

None

APPLIES TO REVISION(S):

0.2

2. 06000009 - Type 1 Instruction (Dual-access) failing if reference is to a memory mapped register:

DESCRIPTION:

When using a type1 instruction, if one of the instructions is accessing memory-mapped IOP registers, the access will fail. For example:

```
DM(I4,M5)=R9, PM(I12,M13)=R11 //Where I12 points to a memory-mapped register
```

The list of effected memporry-mapped registers is given below.

IOAS, IOAE, PSA1S, PSA1E, PSA2S, PSA2E, PSA3S, PSA3E, PSA4S, PSA4E, OSPID, EEMUIN, EEMUSTAT, EEMUOUT, SYSCTL, BRKCTL, REVPIID, DMA1S, DMA1E, DMA2S, DMA2E, PMA1S, PMA1E and EEMUSTAT.

WORKAROUND:

1. Do not use a dual-access instruction to access memory-mapped registers.

2. For Type 1 instructions where both accesses are writes, the anomaly can be avoided by using the DM bus to access the memory-mapped register. Multi-function instructions with writes only have only failed when the PM bus is used to access the memory-mapped registers. Reads will continue to fail regardless of bus used.

For example, both writes below will pass:

```
DM(I4,M5)=R9, PM(I12,M13)=R11 //Where I4 points to a memory-mapped register
//and I12 does not.
```

APPLIES TO REVISION(S):

0.2

3. 06000012 - Incorrect number of loop iterations for counter based loops with PMDA access:

DESCRIPTION:

There are a few scenarios where loop instructions do not execute as expected:

Case 1:

In the rare situation of a one instruction loop with only one iteration, with a PM data memory access, the loop will iterate twice instead of once.

Case 2:

In a one instruction loop with two iterations, with a PM data memory access, the loop will iterate three times instead of twice if the Cache Disable bit is set (CADIS bit in Mode2 register).

Case 3:

In a two instruction loop with one iteration, if the second instruction is a pm data memory access, the loop will iterate twice instead of once.

Case 4:

In a one instruction loop with three iterations, with a PM data memory access, the loop will iterate twice instead of three times if any interrupt related branching happens during the loop's termination period.

Case 5:

In a one instruction loop with four or more iterations, with a PM data memory access, the loop will iterate one less (LCNTR-1) time instead of LCNTR times if any interrupt related branching happens during the loop's termination period and if the Cache Disable bit is set (CADIS bit in the Mode2 register).

WORKAROUND:**Case 1:**

Use the DM bus instead of the PM bus.

Case 2:

1. Use the DM bus instead of the PM bus.
2. Clear the CADIS bit in Mode2 (cleared by default).

Case 3:

1. Use the dm bus instead of the pm bus.
2. Move the PM access to the first instruction of the loop.

Case 4:

1. Use the DM bus instead of the PM bus.
2. Instead of using a single instruction loop with three iterations, explicitly write the instruction three times.

Case 5:

1. Clear the CADIS bit in the Mode2 register (cleared by default).
2. Use the DM bus instead of the PM bus.
3. Unroll the loop, for example one instruction 32 iteration loop can be changed to two instruction 16 iteration loop. There is no problem if the number of instructions is more than one in the loop.

Note: The workaround for the cases 1,2 and 3 of the anomaly is taken care by the tools from the November 2004 update of the Visual DSP++ 3.5 version. The C/C++ compiler "-workaround 2126x-anomaly-4" switch should be used to workaround the anomaly for this Visual DSP++ 3.5 update. For all the Visual DSP++ 4.5 and Visual DSP++ 4.0 versions the workaround for these cases is taken care automatically by the tools. The workaround for the cases 4 and 5 is taken care on the November 2006 update of the Visual DSP++ 4.5 version.

The compiler will generate code that avoids the anomaly condition and all the run-time libraries have been rebuilt to avoid the anomaly. For more details on the tools working, please refer the Visual DSP++ Release Notes in the following links on the external website:

http://download.analog.com/tools/patches/VisualDSP++3.5_32-BitApril2005Update_Release_Note.pdf.

http://www.analog.com/UploadedFiles/Associated_Docs/170024276VisualDSP_45_Update_Release_Note.pdf.

APPLIES TO REVISION(S):

0.2

4. 06000016 - Conditional RTI in SIMD not evaluated properly:

DESCRIPTION:

A conditinal RTI in SIMD mode will not execute as expected. Consider the example:

```
IF COND RTI (DB); //Note that the DB modifier is not needed to cause the
                  //anomalous behavior.
```

The above instruction in SIMD mode should be executed when COND in both PEx and PEy processing elements are true.

The DSP's behavior in executing the instruction is as follows:

- 1) Branches to the address stored at the top of the PC stack.
- 2) Pops the status stack if the ASTATx/y and MODE1 status registers registers have been pushed - if the interrupt was IRQ2-0 or the timer interrupt.
- 3) Clears the appropriate bit in the interrupt mask pointer (IMASKP) register.

The behavior seen with respect to the conditons in PEx and PEy areas follows:

- a. When conditon in PEx and PEy both are false then this instruction is not executed. This is expected.
- b. When PEx is false and PEy is true, then action 1 does not take place but actions 2 and 3 take place. This is anomalous. In this case none of the above actions should be taken.
- c. When PEx is true, and PEy is false then same as case b.
- d. When PEx is true, and PEy is true then all three actions take place. This is expected.

WORKAROUND:

None

APPLIES TO REVISION(S):

0.2

5. 06000018 - Pin Sensitivity (RD_B, DAI_P[20:1]):**DESCRIPTION:**

There is some sensitivity to noise on the RD_B, SPORTx_CLK, and SPORTx_FS signals of the ADSP-2126x processors. This has the potential to cause errors during parallel port read operations including booting, and sport issues when the sport is driving the sport clock & frame sync and an external device is driving the data. (The SPORT signals are routed through the signal routing unit (SRU) to the DAI_P[20:1] pins.)

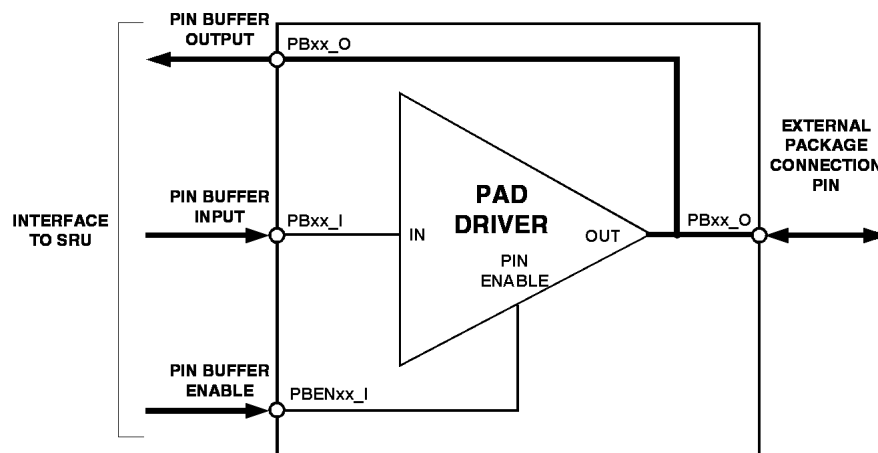
WORKAROUND:**RD_B:**

1. Failures were not seen in memory reads where the RD_B trace length was kept to approximately 7 cm. However, this pin is still susceptible and external capacitance may be needed for memory reads to function properly with other board designs.

SPORTx_CLK & SPORTx_FS:

1. In certain cases, by programming the SRU CLK and FS registers, the reflection sensitivity issue in these signals can be avoided. Consider this Sport Clock example: (The Frame Sync configuration is analogous) In its default routing, the SRU maps the signal from the DAI pin (PBxx_O) back to the Sport Clock Input (SPORTxCLK_I), as well as routing the sport clk output (SPORTxCLK_O) to the Pin Buffer Input (PBxx_I). This connection of PBxx_O to SPORTxCLK_I opens a vulnerability to a glitch coming in even though the Sport is driving the clock as an output.

By programming the Signal Routing Unit (SRU) to remove this input path, we can avoid this vulnerability.



In the figure, by default SPORTxCLK_I would be connected to PBxx_O and SPORTxCLK_O would be routed to PBxx_I. The workaround is to leave the routing of SPORTCLKx_I to PBxx_I as before, providing the sport clock off-chip, but also routing it directly back to SPORTCLKx_I to give the state machine it's signal. This effectively closes off the external access to SPORTCLK_I. For more information about the SRU, consult the DAI Chapter of the ADSP-2126x Hardware Reference Manual.

2. Use the Precision Clock Generator or an external device to generate the Sport Clock and Frame Sync.

APPLIES TO REVISION(S):

0.2

6. 06000020 - Indirect jumps or calls followed by Long Word accesses using PM bus can vector to an unknown location:

DESCRIPTION:

Indirect jumps or calls followed immediately by instructions with a Long Word access using the PM bus (or invalid instruction) can jump to an unexpected location.

For example, in the following sequences of instructions will cause the processor to vector to an unexpected location:
(where $Ic = I15-I8$, $Md = M15-8$)

```
| jump | (Md,Ic);
| call |
```

```
PM ( |Md,Ic      | ) = ureg(LW);
     |Ic,Md      |
     |<addr32>   |
     |<data32>,Ic|
```

```
| jump | (Md,Ic);
| call |
```

```
ureg      = PM ( |Md,Ic      | )(LW);
             |Ic,Md      |
             |<addr32>   |
             |<data32>,Ic|
```

```
| jump | (Md,Ic);
| call |
```

```
invalid instruction;
```

Note that anomaly will occur if the Call or Jump is conditional as well.

WORKAROUND:

1. Place one nop just after the jump or call instruction.
2. Use the DM bus instead of PM for the data access.
3. Use either a PC-relative Jump/Call, or use a direct address.

```
i.e.  jump (pc,12); -or- call (pc,12);
      jump (<addr32>); -or- call (<addr32>);
```

4. If possible, do not use the optional (LW) modifier in the data access.

APPLIES TO REVISION(S):

0.2

7. 06000021 - Parallel Port Bus Contention:

DESCRIPTION:

A bus contention issue has been identified on the ADSP-2126x Parallel Port. When crossing an external memory address page while using DMA-READ transfers, an ALE cycle is inserted to update the upper address bits held by the external latch. When the Parallel Port transitions from a Read-cycle to an ALE cycle, insufficient time was provided to allow the external SRAM or FLASH to tri-state its bus. The bus tri-state from /OE de-assertion timing is typically longer for Flash than for SRAM devices, this necessitates a separate examination for both the SRAM and FLASH cases. (Timing information assumes a 200 MHz core clock rate)

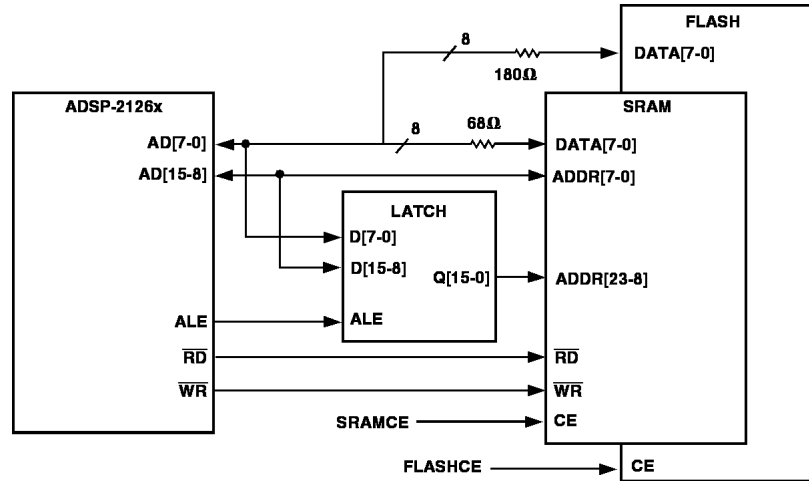
WORKAROUND:

a) SRAM CONTENTION :

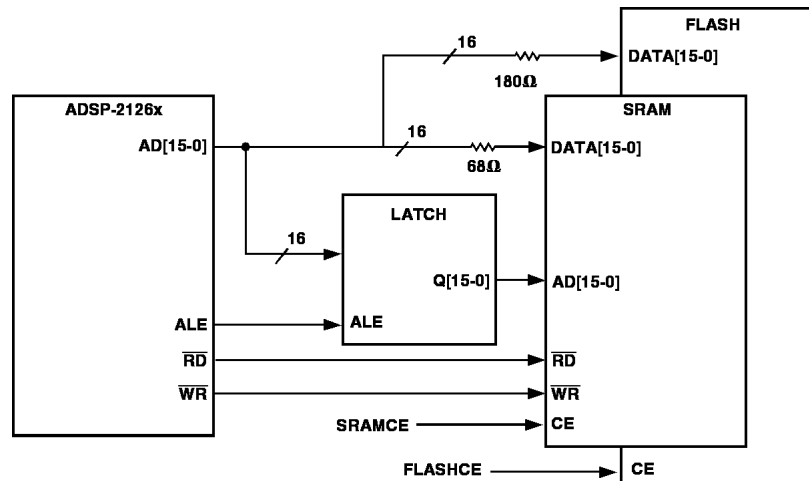
Hardware based work-around:

A typical 8ns SRAM will require 5-7ns to tri-state from /OE de-assertion. The ADSP-2126x only provides for approximately 4.0 ns; therefore, a 3.0ns contention possibility exists. At this time the recommended work-around is to place series resistors before the SRAM data lines, as shown in the diagram below. This resistor will limit the maximum pin current to about 22mA, while still providing sufficiently fast rise-fall rates to meet timing requirements. Our recommendation is 68-Ohms. This option will operate at full speed and require no software changes.

Memory Read—Parallel Port 8-Bit:



Memory Read—Parallel Port 16-Bit:



b) SRAM CONTENTION:

Software based work-around (1):

A Parallel Port hold cycle can be enabled, which will provide an additional 6.5ns for the external device to disable (A bus hold cycle is selected by setting the PPBHC bit in the PPCTL Register). This option will incur an additional 5ns per SRAM transfer, which will lower the overall external bandwidth; otherwise this option will be transparent to software.

Software based work-around (2):

Structure software to always ensure DMA transfers in a 256 byte (or smaller) external burst (in 8-bit mode), this will avoid an ALE cycle after a read. This option will require software to be written such that external pages will never be crossed by DMA access; however, it will allow full speed operation within a page.

c) FLASH CONTENTION:

Hardware based work-around:

A typical FLASH memory has a bus tri-state from OE disable time of 30ns. Bench testing of several FLASH devices revealed that this disable time is typically less than 10ns. However, to ensure safe operation under worst case specifications, the maximum specified FLASH disable must be accommodated. Should the FLASH truly require 30ns to tri-state, it would still be driving the bus during the falling edge of ALE, which strobes the upper addresses into the latch. So unlike the SRAM case above, for FLASH it is also necessary to ensure that valid logic levels are presented to the latch by the AD[15:0] lines during contention. To accomplish this, larger resistors need to be used; our recommendation is 180 Ohms. This resistor value is larger than typically encountered for the purpose of reducing reflections along digital lines; however, since the FLASH is a rather slow device, the rise/fall time delay induced will be commensurately small. To ensure proper operation, the delay incurred by this resistor should be accounted for by adding an additional wait state; simulations with a single FLASH indicate delays of less than 5ns. If these resistor values cannot be accommodated, it is possible to place a tri-state buffer in the data path of the FLASH, as its pass-through delay is relatively insignificant; unfortunately, the turn-off time of such buffers will probably exceed the required 2.5ns, and thus necessitate smaller series resistors between the ADSP-2126x device and the buffer to avoid excessive pad current.

d) FLASH CONTENTION:

Software based work-around:

The Parallel Port Bus Hold Cycle is too short to be effective for FLASH. The method of performing DMAs on a 256 byte (or smaller) external bursts (in 8-bit mode) is recommended when making FLASH accesses. Be advised that during parallel port booting, the processor uses 8-bit mode with consecutive DMA reads, and so contention will be present.

APPLIES TO REVISION(S):

0.2

8. 06000022 - SPI can generate spurious clock for an additional word when used in receive DMA mode at maximum SPICLK frequency:

DESCRIPTION:

SPI can generate spurious clock for an additional word when the following three conditions are met:

1. The SPI is configured for 32-bit, receive master DMA mode and performs back to back DMA transfers.
2. The SPI DMA is disabled and re-enabled between back to back DMA transfers without disabling the SPI itself.
3. The SPI is operated at the maximum SPICLK frequency (SPIBAUD = 2).

When the above three conditions are met, SPI can generate clock for an additional word even after the FIFO and the receive buffer is full. This clock for another word can cause the receive buffer overflow error which will result in loss of the additional received data word.

WORKAROUND:

1. Do not disable the SPI DMA between back to back DMA transfers.
2. If the application demands disabling SPI DMA between back to back DMA transfers then the sequence given below must be followed:
 - Disable the SPI DMA
 - Disable the SPI
 - Clear the FIFO and the receive buffer
 - Configure the DMA descriptors and Enable the SPI
 - Enable the SPI DMA

APPLIES TO REVISION(S):

0.2