



Interfacing AD7865 Parallel ADCs to ADSP-2136x SHARC® Processors

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Introduction

This application note explains how to interface parallel ADCs to ADSP-21365 SHARC® processors. The parallel ADC considered in this application note is the AD7865. The two schemes described in this application note to interface an AD7865 with an ADSP-21365 are the parallel port interface and the parallel data acquisition port (PDAP) interface. This application note also provides example code to demonstrate how the SHARC processor's parallel port and PDAP can be programmed to receive data from an AD7865 in DMA mode.

About AD7865 ADCs

The AD7865 is a fast, low-power, four-channel simultaneous sampling 14-bit A/D converter that operates from a single 5 V supply. The device contains a 2.4 μ s successive approximation ADC, four track/hold amplifiers, 2.5 V reference, on-chip clock oscillator, signal conditioning circuitry, and a high-speed parallel interface. The input signals on four channels are sampled simultaneously. This preserves the relative phase information of the signals on the four analog inputs.

The device allows any subset of the four channels to be converted, maximizing the throughput rate on the selected sequence. The channels to be converted can be selected via hardware (channel select input pins) or via software (programming the channel select register).

The high-speed parallel interface also allows interfacing to 3 V processors.

AD7865 Product Highlights

- The AD7865 features four track/hold amplifiers and a fast (2.4 μ s) ADC, allowing simultaneous sampling and conversion of any subset of the four channels.
- The AD7865 operates from a single 5 V supply and consumes only 115 mW (typical), making it ideal for low-power and portable applications.
- The AD7865 offers a high-speed parallel interface for easy connection to microprocessors, microcontrollers, and digital signal processors.
- The AD7865 is offered in three versions, each with different analog input ranges. The AD7865-1 offers the standard industrial ranges of ± 10 V and ± 5 V; the AD7865-2 offers a unipolar range of 0 V to 2.5 V (or 0 V to 5 V); and the AD7865-3 offers the common signal processing input range of ± 2.5 V.
- The device features very tight aperture delay matching between the four input sample and hold amplifiers.

AD7865 ADC Applications

AD7865 applications include:

- AC motor control

- Uninterruptible power supplies
- Industrial power meters/monitors
- Data acquisition systems
- Communications

About ADSP-21365 Processors

The third generation of SHARC processors, which includes the ADSP-21262, ADSP-21266, ADSP-21267, ADSP-21364, and ADSP-21365 derivatives, offers increased performance, audio and application-focused peripherals, and new memory configurations capable of supporting the latest surround-sound decoder algorithms. All devices are pin compatible and are completely code compatible with all prior SHARC processors. The newest members of the SHARC family are based on a single-instruction, multiple-data (SIMD) core, which supports both 32-bit fixed-point and 32-/40-bit floating-point arithmetic formats, making them particularly suitable for high-performance audio applications.

The ADSP-21365 derivative offers the highest performance – 300 MHz / 1800 MFLOPs. This level of performance makes the ADSP-21365 particularly well suited to address the increasing requirements of the professional and automotive audio market segments. In addition to its high-performance core, the ADSP-21365 includes additional value-added peripherals such as an S/PDIF transmitter/ receiver, 8-channel asynchronous sample rate converter, and hardware digital transmission content protection (DTCP) encryption/ decryption block.

Third-generation SHARC processors also integrate application-specific peripherals that simplify hardware design, minimize design risks, and ultimately reduce time to market. Grouped together and broadly named the digital audio interface (DAI), these functional blocks may be connected to each other or to external pins via the software programmable signal routing unit (SRU). The SRU is an innovative architectural feature that enables complete and flexible routing

among DAI blocks. Peripherals connected through the SRU include (but are not limited to) SPORTs, SPI ports, S/PDIF Tx/Rx, DTCP accelerator, and an 8-channel asynchronous sample rate converter block.

Interfacing AD7865 via Parallel Port

This application note employs a high-speed parallel 14-bit ADC for the interface. A single conversion start signal ($/\text{CONVST}$) simultaneously places all the track/holds into hold mode and initiates the conversion sequence for the selected channels. The $/\text{EOC}$ signal indicates the end of each individual conversion in the selected conversion sequence. The BUSY signal indicates the end of the conversion sequence. Data is read from the AD7865 via a 14-bit parallel data bus using its $/\text{CS}$ and $/\text{RD}$ signals. All four ADC channels are selected in hardware. When the $\text{H\#}/\text{S SEL}$ pin is a logic 0, the AD7865 conversion sequence selection is controlled via the SL1-SL4 input pins and uses an internal clock.

For the sake of simplicity in this application note, the flag pin (FLG0) has been used to select the $/\text{CS}$ of the AD7865 instead of the entire Address latch and decode logic (refer to the blue ellipse in [Figure 1](#)). The address latch and address decode logic is required in any practical system where multiple devices like memory, I/O devices, and so on share the processor's parallel port.

Refer to the functional block diagram in [Figure 1](#) for interfacing details.

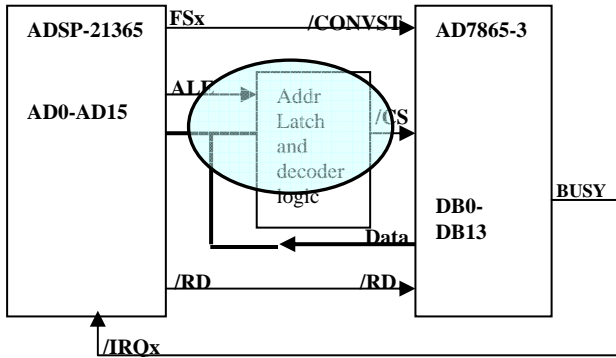


Figure 1. Functional Block Diagram – ADSP-21365 and AD7865 Interface via Parallel Port

A low-to-high transition on the /CONVST input places all of the track/holds into hold mode and starts conversion on the selected channels. Frame sync of SPORT0 is used to generate a /CONVST signal for the ADC. The serial port is configured to transmit with frame sync as data independent frame sync. The SPORT frame sync frequency is determined by the value loaded in the DIV0 register. An initial dummy write to the SPORT TXSP0A register is required to start continuous frame sync on the FS0 signal. The BUSY signal from AD7865 indicates the end of conversion on

all the selected ADC channels. The falling edge of BUSY triggers an interrupt. The interrupt is configured to be edge sensitive. Parallel port DMA is configured in the interrupt service routine and the DMA is initiated.

The ADSP-21365 parallel port must be configured for a 16-bit mode. Two received 16-bit words are packed and transferred to the internal memory as a single 32-bit word; therefore, the DMA completion status is checked to verify the completion of DMA and data rearrangement is carried out before exiting the external interrupt (IRQ1) service routine. The external address modifier (EMPP) value used in the example code is “1”; however, an external address modifier of “0” can be used as a special case for reading FIFOs, offering higher throughput.

Refer to the timing diagram in Figure 2 for reading after the conversion sequences. Figure 3 shows a screen capture of various signals.

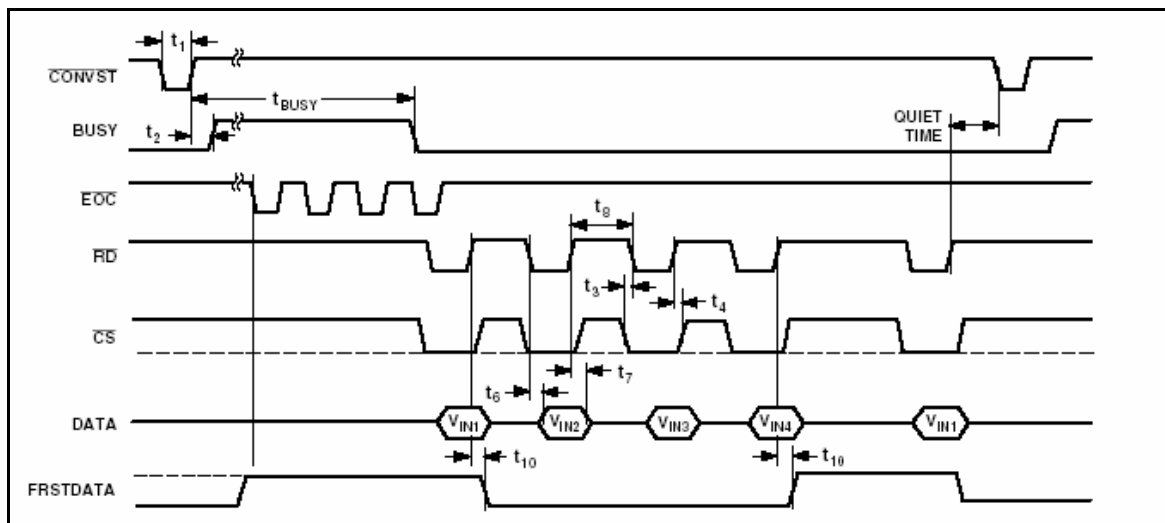


Figure 2. Timing Diagram, Reading After the Conversion Sequences



Figure 3. Timing Diagram, Reading After the Conversion Sequences

Interfacing the AD7865 via PDAP

The parallel data can be acquired through the parallel data acquisition port (PDAP), which provides a means of moving high bandwidth data to the core’s memory space. Channel 0 of the input data port (IDP) can be configured to receive parallel data. For details about the PDAP, refer to chapter 6 “Input Data Port” of “ADSP-2136x SHARC Processor Hardware Reference”. Refer to Figure 4 for PDAP timing details.

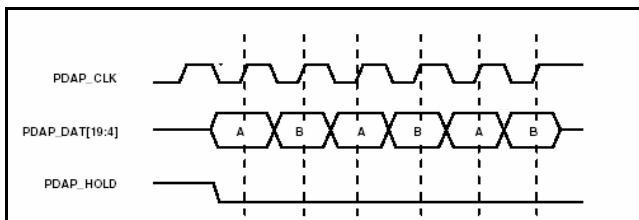


Figure 4. PDAP Timing Diagram

The PDAP_DAT[4:19] signals can be mapped to the processor’s parallel port or the DAI pins. In this application, the PDAP_DAT[4:19] signals are mapped to the DAI pins. As shown in Figure 4, when the PDAP_HOLD signal is held at logic “LOW”, the data is latched on rising edges of PDAP_CLK. The PDAP_HOLD signal is internally held at logic “LOW” and hence, is not shown in the interface block diagram of Figure 6. The /EOC signal from the AD7865 is provided as PDAP_CLK to the ADSP-21365. The conversion results are read after each individual channel data is ready. Refer to the timing diagram in Figure 5 for details on reading during the conversion.

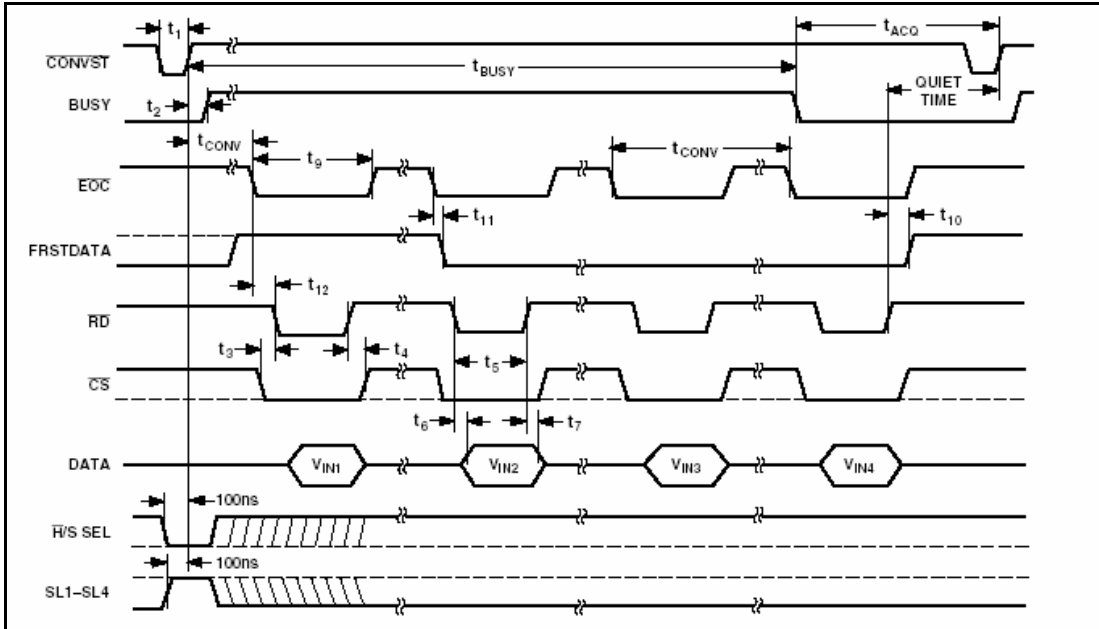


Figure 5. Timing Diagram for Reading During Conversion

The $\overline{\text{EOC}}$ is also connected to the $\overline{\text{RD}}$ signal of the AD7865 to provide $\overline{\text{RD}}$ pulses to the ADC. The PDAP latches valid channel data on the rising edges of the $\overline{\text{EOC}}$ pulses. The $\overline{\text{CS}}$ of the AD7865 and the PDAP_HOLD of the ADSP-21365 are permanently connected to logic “LOW”. The frame sync (FS0) of SPORT0 acts as $\overline{\text{CONVST}}$ for the ADC.

Refer to the block diagram in Figure 6 for interface details. The screen captures in Figure 7 and Figure 8 were taken with a logic analyzer while receiving data on the PDAP.

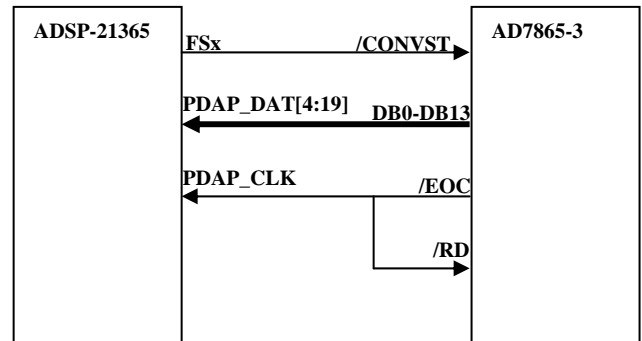


Figure 6. Functional Block Diagram – ADSP-21365 and AD7865 Interface via PDAP

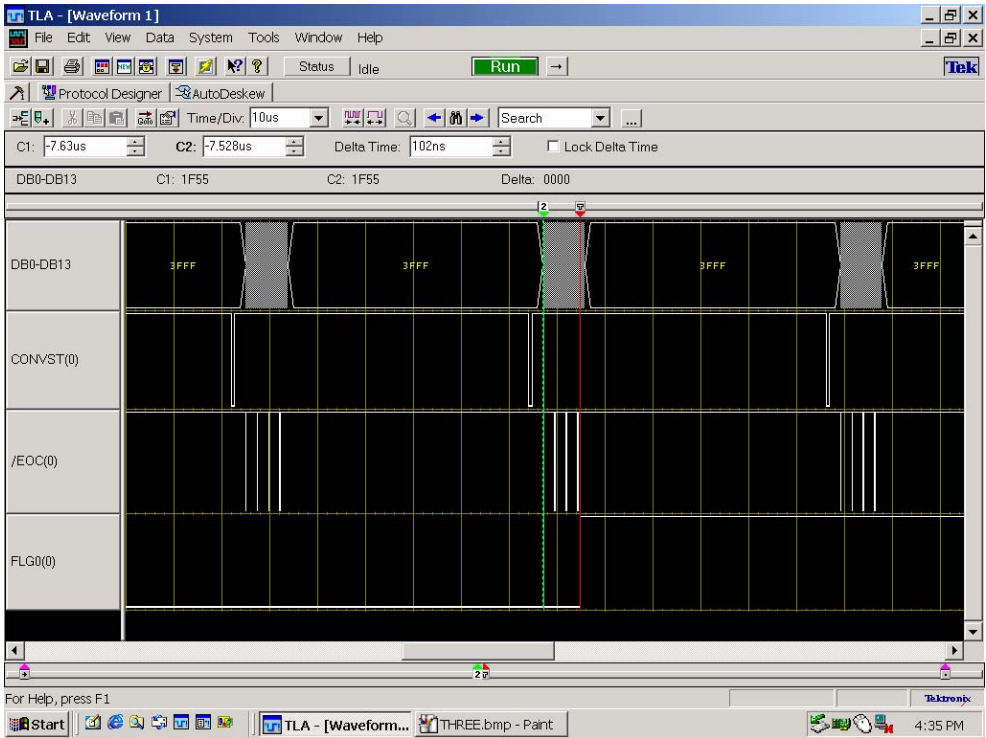


Figure 7. Timing Diagram 1 for Reading During Conversion

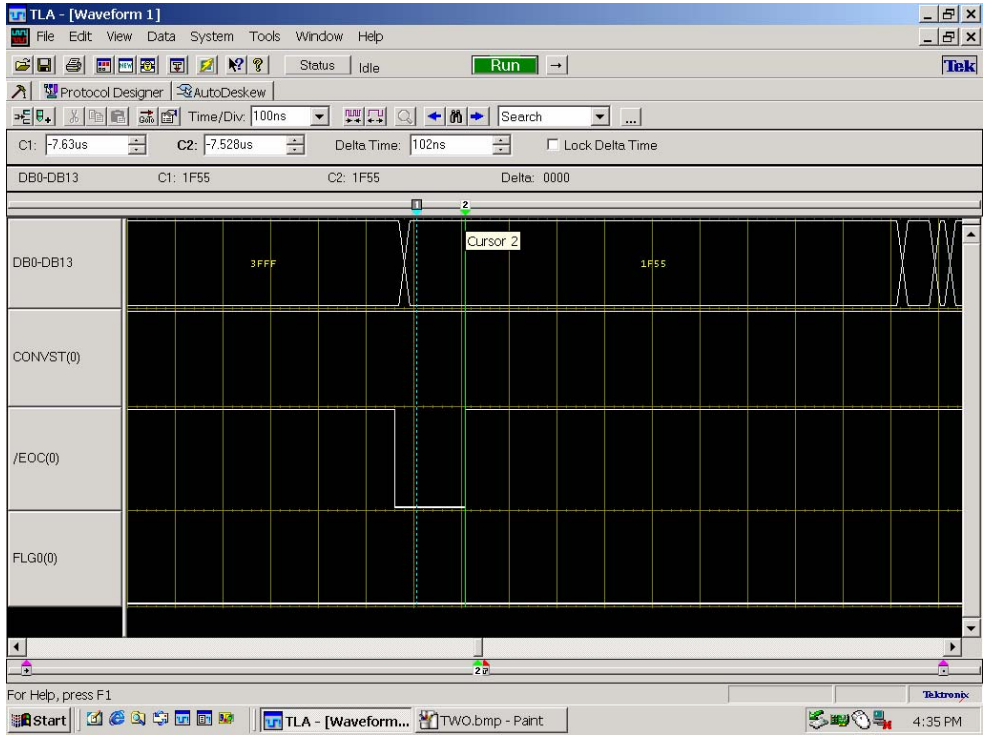


Figure 8. Timing Diagram 2 for Reading During Conversion

Note that the `FLG0` signal is used only for debugging and to trigger the logic analyzer. This signal is not required in an actual application.

Conclusion

This application note shows that parallel ADCs like the AD7865 can be interfaced gluelessly to ADSP-2136x processors on the parallel port or parallel data acquisition port (PDAP) and the converted data can be received in DMA mode.

Appendix

Project files are included in a ZIP file attached to this application note.

References

- [1] *ADSP-2136x SHARC Processor Hardware Reference*. Revision 0.2, October 2004, Analog Devices, Inc.
- [2] *ADSP-21365 Evaluation System Board Schematics*. Analog Devices, Inc.
- [3] *AD7865 Technical Data Sheet*. Rev B. Analog Devices, Inc.

Document History

Revision	Description
<i>Rev 1 – December 17, 2004 by Aseem Vasudev Prabhugaonkar</i>	Initial Release