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Estimating Power Dissipation for ADSP-21371 SHARC® Processors

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Introduction

This EE-Note discusses power consumption of ADSP-21371 SHARC® processors based on characterization data measured over power supply voltage, core frequency (CCLK), and junction temperature (T_J). The intent of this document is to assist board designers in estimating their power budget for power supply design and relief designs using ADSP-21371 processors.

ADSP-21371 processors are members of the SIMD SHARC family of processors, featuring Analog Devices Super Harvard architecture. Like other SHARC processors, the ADSP-21371 processor is a 32-bit processor optimized for high-precision signal processing applications.

ADSP-21371 processors are offered in the commercial temperature range at core clock frequencies of 100-266 MHz. The 266 MHz processors operate at a core voltage of 1.2 V (V_{DDINT}) and at an I/O voltage of 3.3 V (V_{DDEXT}).

The total power consumption of the ADSP-21371 processor is the sum of the power consumed for both of the power supply domains (V_{DDINT} and V_{DDEXT}). The total power consumption has two components: one due to internal circuitry (i.e., the core and the PLL), and the other due to the switching of external output drivers (i.e., the I/O). The following sections detail how to derive both of these components for estimating total power consumption based on different dynamic activity levels, I/O activity, power supply settings, core frequencies, and environmental conditions.

Estimating Internal Power Consumption

The total power consumption due to internal circuitry (on the V_{DDINT} supply) is the sum of the static power component and dynamic power component of the processor's core logic. The dynamic portion of the internal power is dependent on the instruction execution sequence, the data operands involved, and the instruction rate. The static portion of the internal power is a function of temperature and voltage; it is not related to processor activity.

Analog Devices provides current consumption figures and scaling factors for discrete dynamic activity levels. System application code can be mapped to these discrete numbers to estimate the dynamic portion of the internal power consumption for an ADSP-21371 processor in a given application.

Internal Power Vector Definitions and Activity Levels

The following power vector definitions define the dynamic activity levels that apply to the internal power vectors shown in Table 2.

- $I_{DD\text{-}IDLE}$ V_{DDINT} supply current for idle activity. Idle activity is the core executing the IDLE instruction only, with no core

memory accesses, no DMA, and no interrupts.

- $I_{DD\text{-}INLOW}$ V_{DDINT} supply current for low activity. Low activity is the core executing a single-function instruction fetched from internal memory, with no core memory accesses, no DMA, and no activity on the external port.
- $I_{DD\text{-}INHIGH}$ V_{DDINT} supply current for high activity. High activity is the core, executing a multi-function instruction fetched from internal memory and/or cache, with 16 core memory accesses per `CLKIN` cycle (based on a `CLKCFG1-0` setting of 16:1 and DMx64 i.e., long word accesses on DM bus) and DMA through three SPORTs running at 33.3 MHz, SDRAM DMA at 133 MHz and one SPI DMA at 4.16 MHz. The DMAs are chained to themselves (running continuously) and do not use interrupts. The bit pattern for each core memory access and DMA is random.
- $I_{DD\text{-}INPEAK}$ V_{DDINT} supply current for peak activity. Peak activity is the core, executing a multi-function instruction fetched from internal memory and/or cache, with 32 core memory accesses per `CLKIN` cycle (based on a `CLKFG1-0` setting of 32:1 and DMx64, PMx64, i.e., long word accesses simultaneously occurring on both DM and PM buses), DMA through six SPORTs and two SPIs running at 33.3 MHz, SDRAM DMA at 133 MHz, and one UART DMA at 8.33 MHz. Also, two PCGs are configured to generate clocks at 133 MHz. The DMAs are chained to themselves (running continuously) and do not use interrupts. The bit pattern for each core memory access and DMA is random.

  The test code used to measure $I_{DD\text{-}INPEAK}$ represents worst-case processor operation. This activity level is not sustainable under normal application conditions.

- $I_{DD\text{-}INPEAK\text{-}TYP}$ V_{DDINT} supply current for *typical* peak activity. *Typical* peak activity is the core executing a multi-function instruction fetched from internal memory and/or cache, with 32 core memory accesses per `CLKIN` cycle (DMx64, PMx64), DMA through six SPORTs running at 33.3 MHz, DMA through one SPI running at 665 kHz, and SDRAM accesses through the external port running at 133 MHz. The bit pattern for each core memory access, and DMA and SDRAM access is random. SDRAM accesses are split between 60% reads and 40% writes.

Table 1 summarizes the idle, low, high, peak and *typical* peak dynamic activity levels corresponding to the internal power vectors listed above and in Table 2.

Operation	Idle	Low	High	Peak	Peak (Typical)
Instruction Type	IDLE	Single-function	Multi-function	Multi-function	Multi-function
Instruction Fetch	Int Memory	Int Memory	Int Memory, Cache	Int Memory, Cache	Int Memory, Cache
Core Memory Access [1]	None	None	16 per tCK cycle[2]	32 per tCK cycle[3]	32 per tCK cycle[3]
DMA / Switching Frequencies Ext Port / SDRAM SPORTs SPI UART PCG	 SDCLK only N/A N/A N/A N/A	 SDCLK only N/A N/A N/A N/A	 133 MHz 3 @ 1/8*CCLK 1 @ 1/64*CCLK N/A N/A	 133 MHz 6 @ 1/8*CCLK 2 @ 1/8*CCLK 1 @ 1/64*CCLK 2 @ 1/2*CCLK	 60/40 RD/WR 6 @ 1/8*CCLK 1 @ 1/400*CCLK N/A N/A
Data Bit Pattern for Core Memory Access and DMA	N/A	N/A	Random	Random	Random
Ratio – Continuous Instruction Loop to SDRAM Control Code	N/A	100% Instruction Loop	100% Instruction Loop	100% Instruction Loop	50::50 60::40 70::30

Table 1. Dynamic activity level definitions

Estimating I_{DDINT} Dynamic Current, $I_{DD\text{-}DYN}$

Two steps are involved in estimating the dynamic power consumption due to the internal circuitry (i.e., on the V_{DDINT} supply). The first step is to determine the dynamic baseline current, and the second step is to determine the percentage of activity for each discrete power vector with respect to the entire application.

I_{DD} Baseline Dynamic Current, $I_{DD\text{-}BASELINE\text{-}DYN}$

The ADSP-21371 $I_{DD\_BASELINE\_DYN}$ current graph is shown in Figure 1 (Appendix A contains a larger image of this graph). Note that the $I_{DD\_BASELINE\_DYN}$ current is derived using the $I_{DD\text{-}INHIGH}$ dynamic activity level vs. core frequency. Each curve in the graph represents a baseline I_{DDINT} dynamic current for a specified power supply setting. Using the curve specific to the application, the baseline dynamic current ($I_{DD\_BASELINE\_DYN}$) for the V_{DDINT} power supply domain can be estimated at the operating frequency of the processor in the application. For example, with the core operating at 1.2 V (V_{DDINT}) and a frequency of 266 MHz, the corresponding baseline dynamic current ($I_{DD\_BASELINE\_DYN}$) for the V_{DDINT} power supply domain would be approximately 0.444 A.

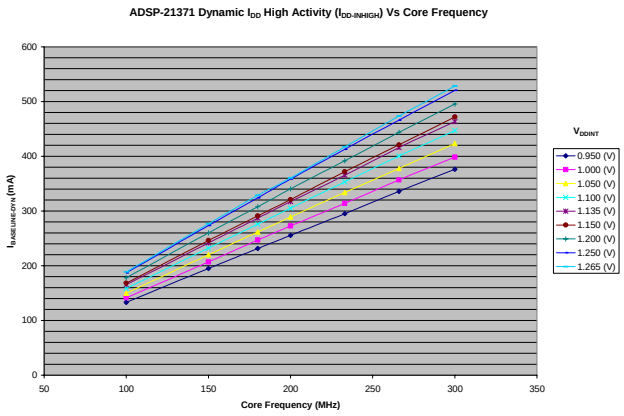

Figure 1. Baseline I_{DDINT} dynamic current

[1] tCK = CLKIN; Core clock ratio 16:1

[2] DMx64 Access

[3] DMx64 Access, PMx64 Access

The ADSP-21371 processor is *not* specified for operation at all values of V_{DDINT} shown. These curves are for reference only. Refer to the data sheet for actual specifications.

I_{DD} Dynamic Current Running Your Application

Table 2 lists the scaling factor for each activity level, used to estimate the dynamic current for each specific application. With knowledge of the program flow and an estimate of the percentage of time spent at each activity level, the system developer can use the baseline dynamic current ($I_{DD\_BASELINE\_DYN}$) shown in Figure 1 and the corresponding activity scaling factor from Table 2 to determine the dynamic portion of the internal current ($I_{DD\text{-}DYN}$) for each ADSP-21371 processor in a system.

Power Vector	Activity Scaling Factor (ASF)
$I_{DD\text{-}IDLE}$	0.22
$I_{DD\text{-}INLOW}$	0.42
$I_{DD\text{-}INHIGH}$	1.00
$I_{DD\text{-}INPEAK}$	1.26
$I_{DD\text{-}INPEAK\text{-}TYP}$ 50::50 60::40 70::30	 0.87 0.94 1.02

Table 2. Internal power vectors and dynamic scaling factors

The ADSP-21371 dynamic current consumption in a specific application is calculated according to the following formula, where "%" is the percentage of the overall time that the application spends in that state:

(% *Peak Typical activity level* x $I_{DD\text{-}INPEAK\text{-}TYP}$ *ASF* x $I_{DD\_BASELINE\_DYN}$)
(% *Peak activity level* x $I_{DD\text{-}INPEAK}$ *ASF* x $I_{DD\_BASELINE\_DYN}$)
(% *High activity level* x $I_{DD\text{-}INHIGH}$ *ASF* x $I_{DD\_BASELINE\_DYN}$)
(% *Low activity level* x $I_{DD\text{-}INLOW}$ *ASF* x $I_{DD\_BASELINE\_DYN}$)
+(% *Idle activity level* x $I_{DD\text{-}IDLE}$ *ASF* x $I_{DD\_BASELINE\_DYN}$)

= *Total Dynamic Current for* V_{DDINT} ($I_{DD\text{-}DYN}$)

Equation 1. Internal dynamic current ($I_{DD\text{-}DYN}$)

For example, after profiling the application code for a particular system, activity is determined to be proportioned as follows.

(0% Peak Typical Activity Level)
(50% Peak Activity Level)
(40% High Activity Level)
(10% Low Activity Level)
(0% Idle Activity Level)

Figure 2. Internal system activity levels

Using the activity scaling factor (*ASF*) provided for each activity level in Table 2 (and the core operating at 1.2 V (V_{DDINT}) and 266 MHz), a value for the dynamic portion of the internal current consumption of a single processor can be estimated as follows.

*(50% **x 1.26 x** 0.444)*
*(40% **x 1.00 x** 0.444)*
*+(10% **x 0.42 x** 0.444)*

$I_{DD\text{-}DYN}$ = *0.476 A*

Figure 3. Internal dynamic current estimation

Therefore, the total estimated dynamic current on the V_{DDINT} power supply in this example is 0.476 A.

Estimating I_{DDINT} Static Current, $I_{DD\text{-}STATIC}$

The ADSP-21371 $I_{DD\text{-}STATIC}$ current graph is shown in Figure 4 (Appendix B contains a larger image of this graph). The static current on the V_{DDINT} power supply domain is a function of temperature and voltage but is *not* a function of frequency or activity level. Therefore, unlike the dynamic portion of the internal current, the static current does not need to be calculated for each discrete activity level or power vector. Using the static current curve corresponding to the application (i.e., at the specific V_{DDINT}), the baseline static current ($I_{DD\text{-}STATIC}$) can be estimated vs. junction temperature (T_J) of the ADSP-21371 processor (see Appendix C for estimating T_J).

For example, in an application with the core operating at 1.2 V (V_{DDINT}) and the ADSP-21371 processor at a junction temperature (T_J) of +105°C, the corresponding baseline static current ($I_{DD\text{-}STATIC}$) for the V_{DDINT} power supply domain would be approximately 0.454 A.

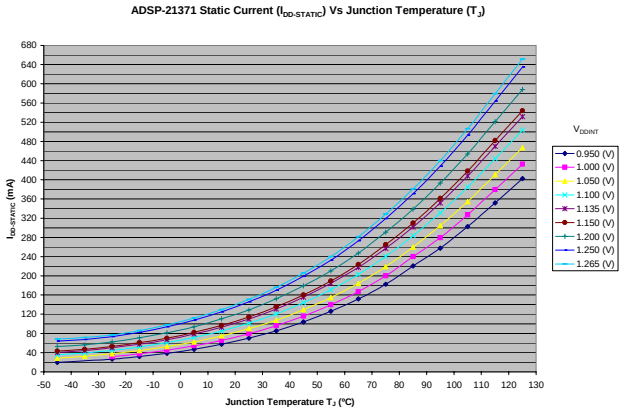

Figure 4. Baseline I_{DDINT} static current

The ADSP-21371 processor is *not* specified for operation at all values of V_{DDINT} or junction temperatures shown. These curves are for reference only. Refer to the data sheet for actual specifications.

The ADSP-21371 static power is constant for a given voltage and temperature. Therefore, it is simply added to the total estimated dynamic current when calculating the total power consumption due to the internal circuitry of the ADSP-21371 processor. Note that the $I_{DD\text{-}STATIC}$ current shown in Figure 4 represents the worst-case static current as measured across the wafer fabrication process for the ADSP-21371 device.

Estimating Total I_{DDINT} Current

The total current consumption due to the internal core circuitry (I_{DDINT}) is the sum of the dynamic current component and the static current component as shown in Equation 2.

$$I_{DDINT} = I_{DD\text{-}DYN} + I_{DD\text{-}STATIC}$$

Equation 2. Internal core current (I_{DDINT}) calculation

Continuing with the example (the processor operating at 1.2 V and 266 MHz, and with the code as profiled), assume that the resulting junction temperature (T_J) is estimated to be +105°C. The total internal current consumed by the processor core under these conditions would then be:

$$I_{DDINT} = 0.476 + 0.454 = 0.930 \text{ A}$$

Equation 3. Total internal core current estimation

Total Estimated Internal Power, P_{DDINT}

The resulting internal power consumption (P_{DDINT}) is given by Equation 4.

$$P_{DDINT} = V_{DDINT} \text{ x } I_{DDINT}$$

Equation 4. Internal power (P_{DDINT}) calculation

Using Equation 4, the total estimated internal power consumed by the processor in the application described in this example would be:

$$P_{DDINT} = 1.20 \text{ V x } 0.930 \text{ A} = 1.116 \text{ W}$$

Equation 5. Total internal power (P_{DDINT}) estimation

Estimating External Power Consumption

The external power consumption (on the V_{DDEXT} supply) is dependent on the switching of the output pins. The magnitude of the external power depends on:

- The number of output pins that switch during each cycle, *O*
- The maximum frequency at which the output pins can switch, *f*
- The voltage swing of the output pins, V_{DDEXT}
- The load capacitance of the output pins, C_L

In addition to the input capacitance of each device connected to an output, the total load capacitance should include the capacitance

(C_{OUT}) of the processor pin itself, which is driving the load.

The SDRAM controller is capable of running up to 133 MHz and can run at various frequencies, depending on the programmed SDRAM clock (SDCLK) to core clock (CCLK) ratio.

The maximum read/write throughput of the asynchronous memory interface (AMI) is one 32-bit word per 3 SDCLK cycles (wait state of 2). This corresponds to a maximum switching frequency of 22.2 MHz for ADDR23-0 and DATA31-0 during SDRAM writes and writes to external asynchronous memories.

In addition, the serial ports (SPORTs) and serial peripheral interface (SPI) can operate up to one-eighth (1/8) the processor core clock rate (CCLK). With a core clock of 266 MHz, this corresponds to a maximum switching frequency of 16.6 MHz for SDATA and MOSI/MISO, and a maximum switching frequency of 33.3 MHz for SCLK and SPICLK.

Equation 6 shows how to calculate the average external current (I_{DDEXT}) using the above parameters:

$$I_{DDEXT} = O \times f \times V_{DDEXT} \times C_L$$

Equation 6. External current (I_{DDEXT}) calculation

The estimated average external power consumption (P_{DDEXT}) can be calculated as follows.

$$P_{DDEXT} = V_{DDEXT} \times I_{DDEXT}$$

Equation 7. External power (P_{DDEXT}) calculation

For a sample configuration shown in Figure 5, we can estimate the external current and thereby the external power consumption with the following assumptions:

- Processor core running at 266 MHz (CCLK)
- 64K x 32-bit external SRAM, C_L = 10 pF (trace capacitance ignored)
- Writes to external memory occur with WS=2

  During external memory writes, 50% of the ADDR23-0 and DATA31-0 pins are switching
- DAI configured as SPORT transmitting and receiving 32-bit words at 1/8*CCLK, C_L = 10 pF (trace capacitance ignored)
- DPI configured as SPI master transmitting and receiving 32-bit words at 1/8*CCLK, C_L = 10 pF (trace capacitance ignored)
- Output capacitance of processor pin, C_{OUT} = 4.7 pF

The external current (I_{DDEXT}) (Equation 6) can be calculated for each class of pins that can drive and is shown in Table 3.

Summing the individual currents from Table 3, the total external current (I_{DDEXT}) for the sample configuration would be 0.062 A.

Using this current, the estimated average external power is calculated as:

$$P_{DDEXT} = 3.3 \text{ V} \times 0.062 \text{ A} = 0.205 \text{ W}$$

Equation 8. External power (P_{DDEXT}) calculation

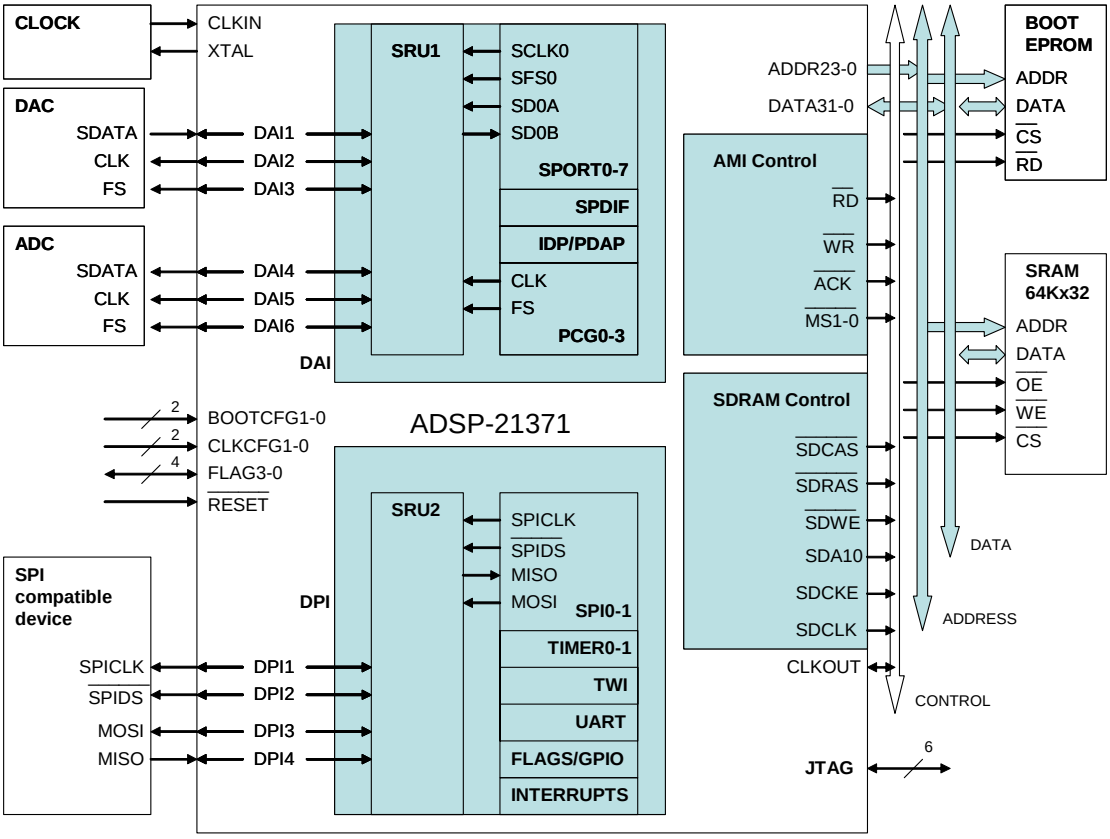

Figure 5. ADSP-21371 system example configuration

Pin Type	No. of Pins	% Switching	x f	x V_{DDEXT}	x C	I_{DDEXT}
ADDR[23:0]	24	50	22.2 MHz	3.3V	4.7pF + 2*10pF	0.021714
DATA[31:0]	32	50	22.2 MHz	3.3V	4.7pF + 2*10pF	0.028952
$\overline{RD}$	1	0	n/a	3.3V	4.7pF + 10pF	0.000000
$\overline{WR}$	1	100	44.4 MHz	3.3V	4.7pF + 10pF	0.002154
MS[1:0]	1	0	n/a	3.3V	4.7pF + 10pF	0.000000
SDCLK	1	100	133 MHz	3.3V	4.7pF	0.002063
DAI_P1 (SDATA)	1	100	16.6 MHz	3.3V	4.7pF + 10pF	0.000805
DAI_P2 (SCLK)	1	100	33.3 MHz	3.3V	4.7pF + 10pF	0.001615
DAI_P3 (FS)	1	100	1.0 MHz	3.3V	4.7pF + 10pF	0.000049
DAI_P4 (SDATA)	1	100	16.6 MHz	3.3V	4.7pF + 10pF	0.000805
DAI_P5 (SCLK)	1	100	33.3 MHz	3.3V	4.7pF + 10pF	0.001615
DAI_P6 (FS)	1	100	1.0 MHz	3.3V	4.7pF + 10pF	0.000049
DPI_P1 (SPICLK)	1	100	33.3 MHz	3.3V	4.7pF + 10pF	0.001615
DPI_P2 (SPIDS)	1	0	n/a	3.3V	4.7pF + 10pF	0.000000
DPI_P3 (MOSI)	1	100	16.6 MHz	3.3V	4.7pF + 10pF	0.000805
DPI_P4 (MISO)	1	0	n/a	3.3V	4.7pF + 10pF	0.000000

Table 3. External current (I_{DDEXT}) summary for Figure 5.

Total Power Consumption

For a particular system, the total power consumption becomes the sum of its individual components, the power consumed by the internal circuitry, and the power consumed due to the switching of the I/O pins, as follows:

$$P_{TOTAL} = P_{DDINT} + P_{DDEXT}$$

Equation 9. Total power (P_{TOTAL}) calculation

Where:

P_{DDINT} = Internal power consumption as defined by Equation 5

P_{DDEXT} = External power consumption as defined by Equation 8

For example, assuming that the processor in the previous example is operating at 1.2 V, 266 MHz, and code as profiled in Figure 2, and also assuming the resulting junction temperature (T_J) has been estimated to be +105°C (see Appendix B for estimating T_J), the total estimated power consumed would be:

$$P_{TOTAL} = 1.116\ W + 0.205\ W = 1.321\ W$$

Equation 10. Total power (P_{TOTAL}) calculation for the sample configuration in Figure 5 and running code described in the example

Appendix A

The ADSP-21371 $I_{DD\_BASELINE\_DYN}$ current graph is shown in Figure 6 (also in Figure 1). The $I_{DD\_BASELINE\_DYN}$ current is derived using the $\boldsymbol{I_{DD\text{-}INHIGH}}$ dynamic activity level vs. core frequency. Each curve in the graph represents a baseline I_{DDINT} dynamic current for a specified power supply setting.

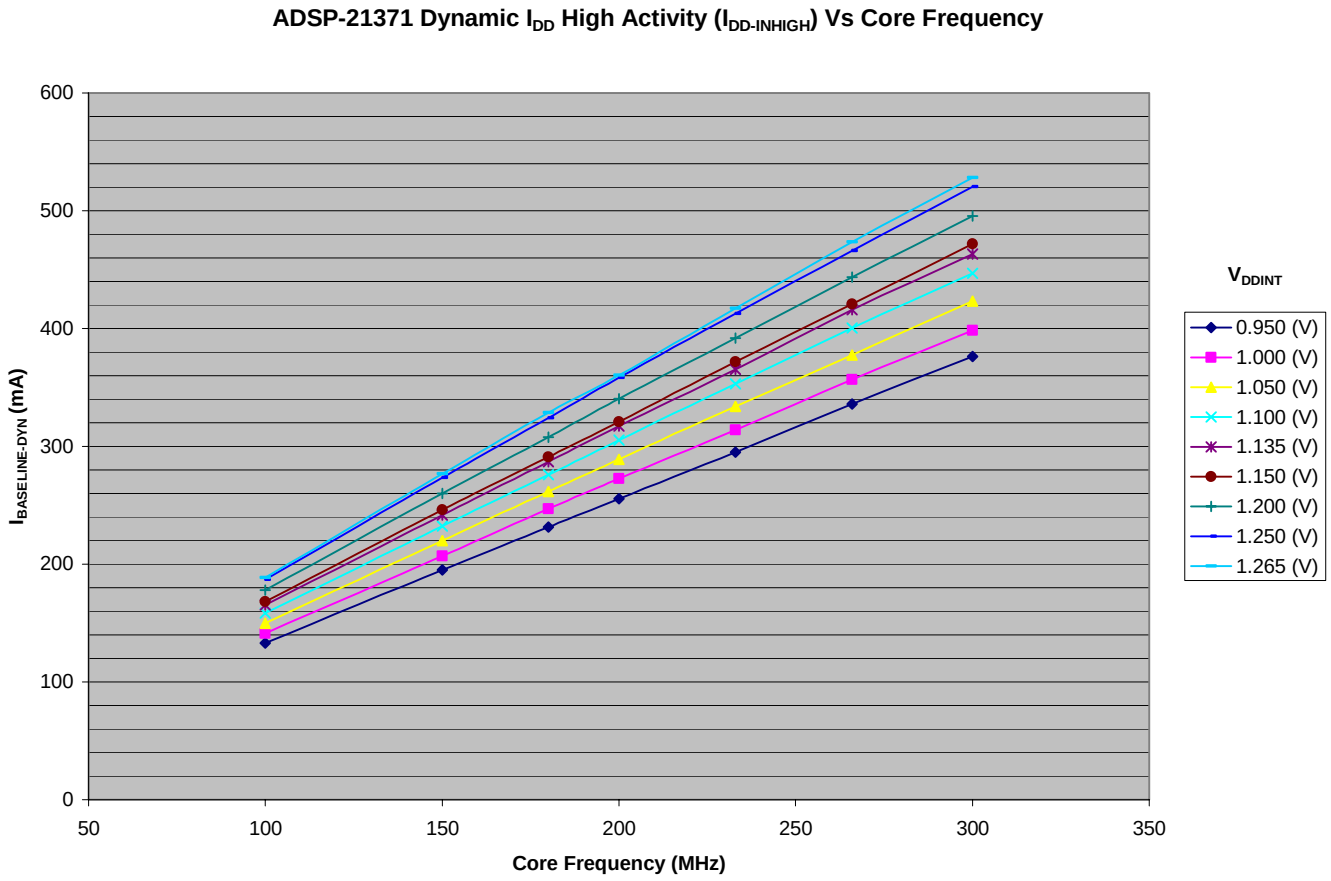

Figure 6. $I_{DD\_BASELINE\_DYN}$ graph

The ADSP-21371 processor is *not* specified for operation at all values of V_{DDINT} shown. These curves are for reference only. Refer to the data sheet for actual specifications.

Appendix B

The ADSP-21371 $I_{DD\text{-}STATIC}$ current graph is shown in Figure 7 (also in Figure 2). The static current on the V_{DDINT} power supply domain is a function of temperature and voltage and is *not* a function of frequency or activity level. Each curve in the graph represents a baseline I_{DDINT} static current for a specified power supply measured at various junction temperatures (T_J). The $I_{DD\text{-}STATIC}$ current graph (Figure 7) represents the worst-case static currents as measured across the wafer fabrication process for the ADSP-21371 processor.

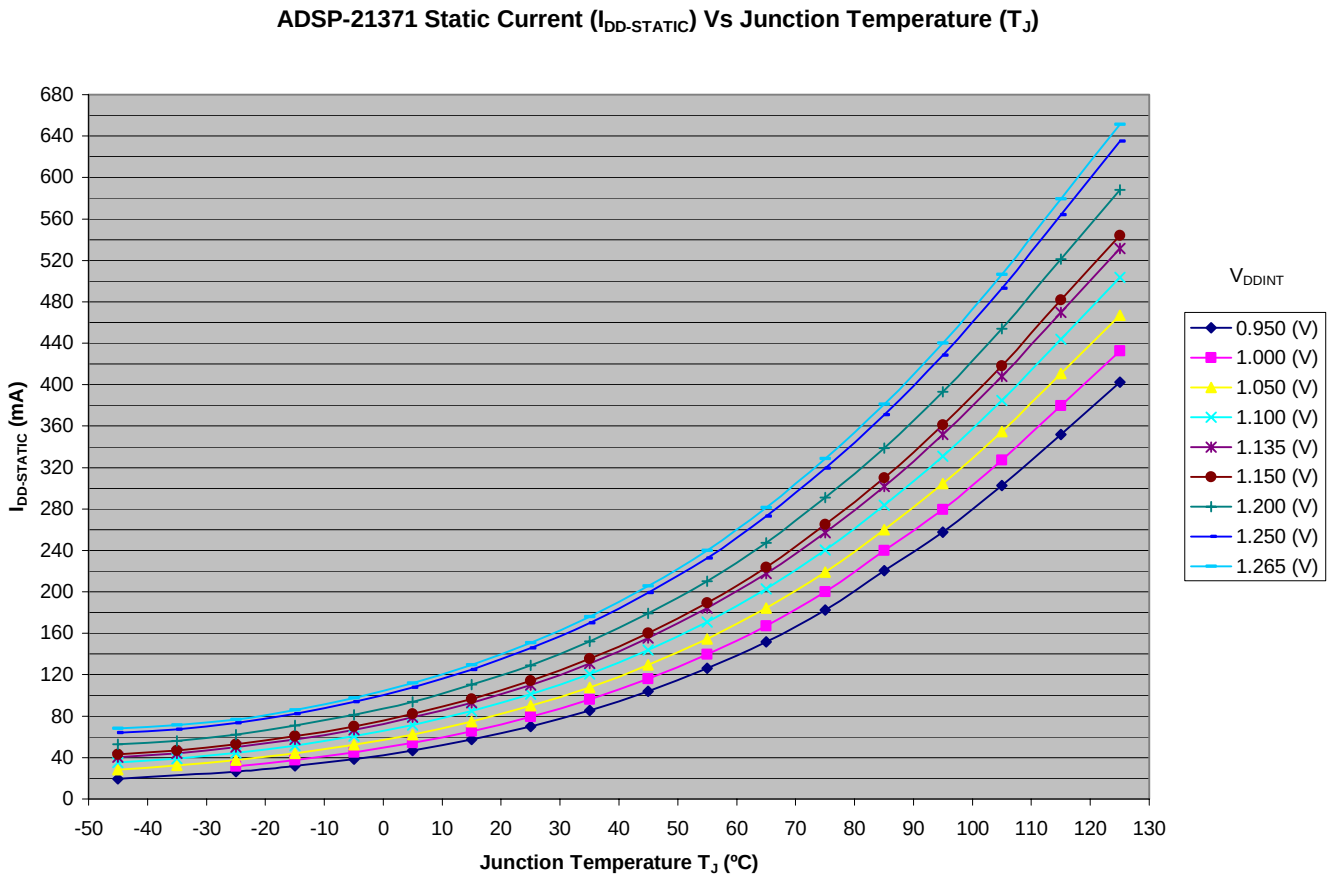

Figure 7. $I_{DD\text{-}STATIC}$ graph

The ADSP-21371 processor is *not* specified for operation at all values of V_{DDINT} or T_J shown. These curves are for reference only. Refer to the data sheet for actual specifications.

Appendix C

Correct functional operation of the ADSP-21371 processor is guaranteed when the junction temperature of the device does not exceed the allowed junction temperature (T_J) as specified in the data sheet. For the ADSP-21371 processor, the total power budget is limited by the maximum allowed junction temperature (T_J) as specified in the data sheet.

The ABSOLUTE MAXIMUM RATINGS table in the ADSP-21371 processor data sheet states that exposure to junction temperatures greater than +125^{O}C for extended periods of time may affect device reliability.

To determine the junction temperature of the device while on the application printed circuit board (PCB), use the following equation found in the THERMAL CHARACTERISTICS section of the data sheet:

$$T_J = T_T + (P_{TOTAL} \times \psi_{JT})$$

Equation 11. Junction temperature (T_J) calculation

Where:

T_T = Package temperature (^{o}C) measured at the top center of the package

P_{TOTAL} = Total power consumption (Watts) as defined in Equation 9

ψ_{JT} = Junction-to-top (of package) characterization parameter (^{o}C/W)

Under natural convection, ψ_{JT} for a thin plastic package is relatively low. This means that under natural convection conditions, the junction temperature (T_J) is typically just a little higher than the temperature at the top-center of the package (T_T). The die is physically separated from the surface of the package by only a thin region of plastic mold compound. Unless the top of the package is forcibly cooled by significant airflow, there will be very little difference between T_T and T_J. However, note that ψ_{JT} is affected by airflow, and the values for ψ_{JT} under various airflow conditions are listed in the THERMAL CHARACTERISTICS section of the ADSP-21371 processor data sheet for the 208-lead MQFP package.

The THERMAL CHARACTERISTICS section of the data sheet also provides thermal resistance (θ_{JA}) values for the 208-lead MQFP package. Data sheet values for θ_{JA} are provided for package comparison and PCB design considerations only and are not recommended for verifying T_J on an actual application PCB.

References

[1] *ADSP-21371 SHARC Processor Data Sheet*, Rev.0, June 2007. Analog Devices, Inc

[2] *ADSP-21368 SHARC Processor Hardware Reference*, Revision 1.0, September 2006. Analog Devices, Inc.

[3] *Estimating Power for the ADSP-21369 SHARC Processors (EE-299)*, Rev 1, December 2006. Analog Devices Inc.

Document History

Revision	Description
Rev 1 – July 19, 2007 *by Manna Kalakotla and Gururaj K*	Initial release