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Migrating from ADSP-21065L to ADSP-21375 SHARC® Processors

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Introduction

This EE-Note highlights relevant details when migrating from ADSP-21065L SHARC® processors to ADSP-21375 SHARC processors. This document addresses processor capabilities and throughput, development tools, and hardware design issues. It is beneficial for the reader to be familiar with each processor's data sheet.

Hardware Differences

Packages

ADSP-21375 processors are offered in the same 208-lead MQFP package as ADSP-21065L devices. This simplifies production logistics and footprint concerns. Although ADSP-21375 processors are pin compatible with both the ADSP-21367 and ADSP-21369 processors, it is not pin compatible with ADSP-21065L parts.

ADSP-21368 processors are offered only in SBGA, not in MQFP.

Power Supplies

ADSP-21065L processors must be supplied with 3.3 V. ADSP-21375 processors use a dual-supply scheme with 3.3 V I/O, and with 1.2 V to power both the core and on-chip PLL.

CLKIN Source

ADSP-21065L processors can use a crystal or crystal oscillator to supply its `CLKIN`. The `CLKIN` frequency is multiplied by two to run the Core Clock (`CCLK`).

ADSP-21375 processors have an on-chip PLL, which provides a high-quality clock pulse to the core; The PLL provides a wide range of multipliers and dividers, allowing you to select from a multitude of crystal or crystal oscillator frequencies, and to multiply up to the desired `CCLK` rate. This feature can also be used to minimize power dissipation during idle periods by lowering the `CCLK` rate when full throughput is not required. Specific `CLKIN` sources that target particular even multiples of sample rates can now be targeted for high-precision audio applications.

Enhancements

Faster Core

ADSP-21375 processors run at 266 MHz, which is considerably faster than the ADSP-21065L processor's 66 MHz. To access internal memory at this rate, the ADSP-21375 pipeline has five stages (the ADSP-21065L has only three stages).

ADSP-21375 processors are fully source-code-compatible with earlier SHARC devices. ADSP-21065L source code can be optimized easily to take advantage of the ADSP-21375 processor's architectural enhancements and to leverage the new processor's internal memory structure.

SIMD

ADSP-21065L processors are single-instruction, single data (SISD) machines. Their single processing element and SHARC architecture provides 66 MIPS, 66 MMACS, and 132 MFLOPS of performance.

Single-instruction, multiple data (SIMD) is an architecture enhancement that was introduced in the ADSP-2116x SHARC family. SIMD provides a second identical processing element, which can effectively double performance. When combined with the increased (266 MHz) core instruction rate, ADSP-21375 processors can perform at 266 MIPS, 533 MMACS, and 1.596 GFLOPS.

Internal Memory

ADSP-21065L processors have two independent dual-ported blocks of on-chip RAM. Although ADSP-21375 processors contain the same amount of memory, it is not dual-ported. Instead, it has four blocks of internal memory, and each block can be configured for different combinations of code and data. Using the four memory blocks and the separate on-chip buses, ADSP-21375 processors can perform two data transfers from the core and one data transfer from the I/O processor in a single cycle.

ROM Space

Both ADSP-21065L and ADSP-21375 processors include 500 Kbits of internal memory space. Optionally, the ADSP-21375 may be purchased with an additional 2 Mbits of on-chip, mask-programmable ROM. This ROM can be manufactured by Analog Devices to contain your customized user instructions or data. Several security features are also available to provide protection for custom IP. For more information, contact your local ADI sales office.

Software Considerations

ADSP-21375 processors are code-compatible at the assembly level with all previous SHARC processors. To maximize processor performance, be aware of the following considerations.

Assembly Language Loops Optimizations

Because of the additional two pipeline stages, short counter-based (`LCNTR`) loops may incur up to three cycles of overhead.

To avoid this overhead, a loop of length one must iterate at least four times, a loop of length two must iterate at least two times, and a loop of length three must iterate at least two times.

Memory Organization Optimization

One bus only (DM, PM, or IOP) can access each of the four memory blocks in a given cycle. To maximize efficient use of memory, do not place DMA-serviced buffers in memory blocks that are used frequently for core (DM/PM-bus) accesses. Use block 2 and block 3 to hold ping-pong DMA buffers. Perform core accesses to one block, while DMA transfers occur on the other block. For filters such as FIRs, place instructions and coefficients in the same block. This is the same methodology suggested for other devices such as those in the ADSP-21364 generation of SHARC processors.

New Peripherals

ADSP-21375 processors include a slew of additional peripheral interfaces compared those on ADSP-21065L processors. These peripherals allow the ADSP-21375 to interface to a wide variety of devices and permit enhanced data I/O between these devices and other external peripheral devices.

DAI / DPI

The digital audio interface (DAI) refers to a group of 20 device pins you configure via software to enable various groups of ADSP-21375 peripherals. This approach allows the processor to contain many peripherals, yet maintains a manageable number of pins. The following peripherals are available within the DAI.

Input Data Port (IDP)

The IDP, which is configurable as eight channels of I^2S serial data (or as seven channels plus a 20-bit-wide synchronous parallel data acquisition port), provides an additional input path to the ADSP-21375 core. Each data channel, which has its own DMA channel, is independent of the ADSP-21375 processor's SPORTs.

Precision Clock Generators

The ADSP-21375 processor's phase-locked loop (PLL) provides clocking for the processor core. Although the performance specifications of the PLL are appropriate for the core, they have not been optimized or specified for precision data converters on which jitter causes time quantization errors and distortion.

When using precision converters, you can use the precision clock generators (PCGs) to generate a clock and frame sync pair that are not derived from the core PLL. As a unit, the PCG takes its clock input from the `CLKIN` source (before the core PLL) or from a DAI pin (allowing an external source). A SPORT can also be used in slave mode, and the PCG can supply its `SCLK` and `FSYNC` signals; this effectively removes the SPORT from the core PLL clock domain.

DPI Functions

The digital peripheral interface (DPI) functions like the DAI, but contains an additional set of peripheral ports.

Serial Peripheral (Compatible) Interface (SPI)

The ADSP-21375 SHARC processor contains two Serial Peripheral Interface (SPI) ports. The SPI is an industry-standard synchronous serial link, enabling the ADSP-21375 SPI-compatible port to communicate with other SPI compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting master and slave modes. The SPI port can operate in a multi-master environment by interfacing with up to four other SPI compatible devices, either acting as a master or slave device. The ADSP-21375 SPI-compatible peripheral implementation also features programmable baud rate, clock phase, and polarities. The ADSP-21375 processor's SPI port uses open drain drivers to support a multi-master configuration and to avoid data contention. The ADSP-21375 can boot from a device connected to the SPI port.

UART

ADSP-21375 processors provide a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data.

Two-Wire Interface (TWI)

The TWI is a bi-directional two-wire, I^2C-compatible serial bus used to move 8-bit data while maintaining compliance with the I2C bus protocol.

Pulse Width Modulation (PWM)

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate center-aligned or edge-aligned PWM waveforms. In addition, it

can generate complementary signals on two outputs in paired mode, or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

General-Purpose (GP) Timers

In addition to the core timer, there are two GP Timers within the DPI that provide PWM generation, pulse width count/capture, and external event watchdog capabilities.

In addition to the added peripherals, some existing peripherals have been enhanced.

I/O Processor

24 Channels of DMA

Compared to ADSP-21065L processors, ADSP-21375 processors provide additional DMA channels with which to move data into and out of the device. These channels (shown in **bold**) complement its additional peripherals.

Type	Number
SPORT	8
DMA	2
External Port	2
IDP	**8**
SPI	**2**
Memory-to-Memory	**2**
UART	**2**

Table 1. ADSP-21375 DMA Channels

Memory-to-Memory DMA

Besides using the I/O Processor to DMA instructions or data to/from internal memory via the external port or peripheral ports, ADSP-21375 processors can DMA a block of data from one internal memory location to another. This feature maximizes the flexibility of using the four-block internal memory structure.

Serial Ports

In addition to doubling the number of synchronous serial ports and increasing throughput to 50 Mbits/s, the ADSP-21375 SPORTs have been enhanced. Besides DSP serial, I^2S, and TDM mode, the ADSP-21375 SPORTs also includes left-justified sample-pair and packed I^2S modes.

TDM/multi-channel mode is now more flexible, allowing any SPORT pair to be used together. The SPORTs have error-detection logic that can detect framing errors, and can share a dedicated error interrupt. The SPORTs can also be used with the ADSP-21375's Precision Clock Generators in high-precision applications.

External Port

SDRAM Controller

133 MHz Operation

Although the ADSP-21375 processor's instruction rate has increased to 266 MHz (compared to the ADSP-21065L), its supported SDRAM speed is also increased to 133 MHz. Like the ADSP-21065L, the ADSP-21375 can address up to 128 MB of SDRAM, and has two `SDCLK` pins to support banks with multiple SDRAM devices without the need for off-chip clock buffers.

External Execution

Similar to ADSP-21065L processors, the ADSP-21375 processors can execute instructions directly from external SDRAM from bank 0. In addition to the faster SDRAM clock, the instruction execution throughput has been enhanced.

The ADSP-21065L requires four `SDCLK` cycles to execute one instruction in 32-bit mode. Because of its 16-bit SDRAM bus, the ADSP-21375 can execute two instructions in six `SDCLK` cycles. Even with 133-MHz SDRAM, this is still a

considerable improvement despite having half the bus width.

DQM

ADSP-21065L processors can support SDRAM `DQM` (Data Byte Mask Control) logic, which allows a processor to block write operations, protecting SDRAM contents while the bus is used for other purposes.

ADSP-21375 processors do not drive the SDRAM `DQM` signal. The `DQM` signal on the SDRAM device (if applicable) can be tied inactive. Refer to the SDRAM manufacturer's data sheet for more information.

Host Port

The ADSP-21065L provides host processor support within its external port, including signals used in bus arbitration that permit glueless connections to standard microprocessor buses. The ADSP-21375 does *not* include this host processor interface and cannot share its bus with other SHARC processors or microprocessors.

Development Tools

VisualDSP++

ADSP-21065L processors continue to be supported in current and upcoming versions of the VisualDSP++® development tools. ADSP-21375 processors require VisualDSP++ version 4.0 (November 2005 update) or newer versions. Many improvements have been made to the development toolset, including enhanced linker support, numerous compiler improvements (including C++ support), code profiling features, and advanced debugging features. More information about VisualDSP++ tools is available at:

http://www.analog.com/processors/resources/crosscore.

Emulators

ADSP-21065L processors were supported by several in-circuit-emulators (ICEs) including the EZ-ICE®, Mountain-ICE™, Apex-ICE™, Summit-ICE™, and Trek-ICE™.

ADSP-21375 processors are supported by the new High-Performance PCI (HPPCI), HP-USB, and USB emulators. ADSP-21065L parts are also supported by this new family of emulators. For the latest information on Analog Devices emulators, refer to our Web site.

Evaluation Platform

The ADSP-21065L EZ-KIT Lite® evaluation board provides an excellent platform for evaluation of (and code development for) ADSP-21065L processors. This EZ-KIT Lite includes an AD1819 stereo codec, an EMAFE interface for use with Analog Devices ADC Evaluation Boards, and an RS-232 interface, which permits limited debugging capability with a PC without an Emulator.

The ADSP-21375 EZ-KIT Lite provides many additional features such as an AD1835 96-kHz 24-bit stereo codec, serial flash memory, SDRAM, SRAM, an RS-232 transceiver, and an enhanced expansion interface for use with Analog Devices EZ-Extender cards for additional functionality. It also uses a USB-based interface to allow the use of VisualDSP++ without an Emulator with full debug capabilities (but with less performance). Unlike the ADSP-21065L EZ-KIT Lite, the USB debug agent on the ADSP-21375 EZ-KIT Lite is not constrained in memory usage and processor functionality.

	ADSP-21375	ADSP-21065L
Processing elements	2 (SIMD)	1 (SISD)
Instruction rate	266 MHz	66 MHz
Serial Ports	4 (with new packed I2S mode)	2
SPI	2	n/a
RAM	0.5 Mbit	0.5 Mbit
ROM	2M bit	n/a
SDRAM controller	16-bit, 133 MHz	32 bits wide, 66 MHz
Package(s)	208-lead MQFP[1]	208-lead MQFP, 196-ball MBGA
Power supplies	Core = 1.2 V, I/O = 3.3 V	Core = I/O = 3.3 V
DMA controller	24 channels	10 channels
UART	1 (full duplex)	n/a
PWM output	16	1

Table 2. Summary of Features for ADSP-21375 vs. ADSP-21065L SHARC Processors

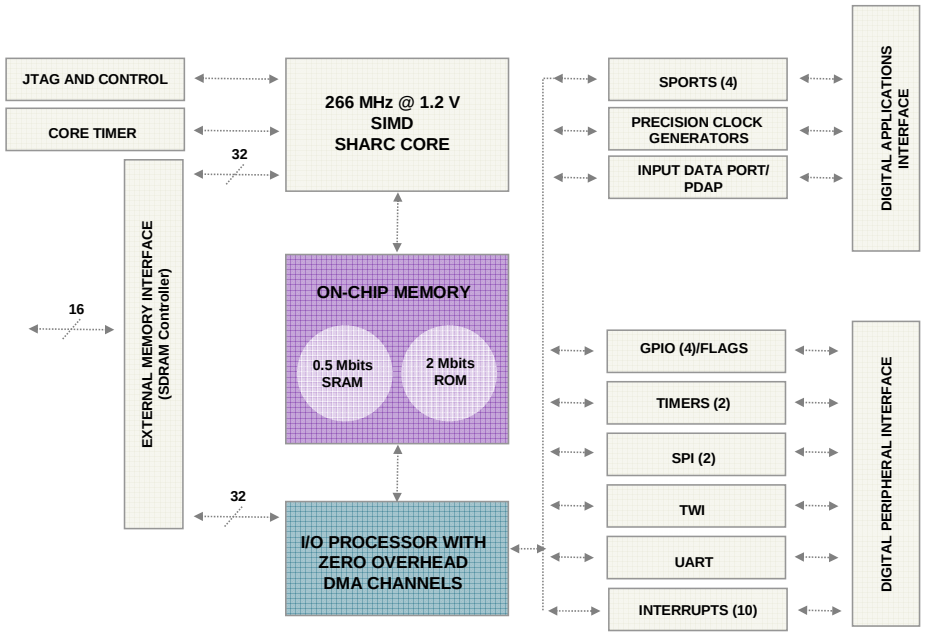

Figure 1. ADSP-21375 Processor Block Diagram

[1] The ADSP-21375 is offered in a lead-free package and is not pin-compatible with the ADSP-21065L

Document History

Revision	Description
Rev 2 – March 15, 2006 *by R. Murphy*	Added Table 2
Rev 1 – November 10, 2005 *by R. Murphy*	Initial Release