



SDRAM Selection Guidelines and Configuration for ADI Processors

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Introduction

This EE-Note is intended to help the user select and configure a suitable Synchronous Dynamic Random Access Memory (SDRAM) device to interface with Analog Devices Inc. (ADI) processors and DSPs.

The different factors involved in choosing the appropriate memory component depending on the Processor or DSP used will be discussed in this document. Additionally, some programming examples on how to configure the SDRAM controller will be shown.

Please note that, although the concepts explained throughout this note apply to all ADI processors and DSPs that have an On-Chip SDRAM Controller, the programming examples described in this document are based on the ADSP-TS201S TigerSHARC® and the ADSP-BF533 Blackfin® processors.

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ADI Processors and DSPs

Several Analog Devices processors and DSPs have been designed with an on-chip SDRAM controller:

- The ADSP-21065L and ADSP-21161N SHARC DSPs.
- The ADSP-TS101S, ADSP-TS201S, ADSP-TS202S and ADSP-TS203S TigerSHARC processors.
- The ADSP-BF531, ADSP-BF532, ADSP-BF533 and ADSP-BF535 Blackfin processors.

Having an On-Chip SDRAM Controller allows to *gluelessly* interface to SDRAM memory devices without the necessity of incorporating additional components to the system, resulting in a cost-effective solution.

SDRAM Specifications

There are several factors that need to be considered when selecting an SDRAM device to interface with ADI's processors or DSPs, which are common across all families:

- Supported operating voltage
- Maximum supported operating frequency
- Maximum supported memory
- I/O size and number of banks
- Column Address Strobe (CAS) latency
- Refresh rate
- Burst length
- Page size
- Initialization sequence

All these characteristics are defined in the SDRAM device datasheet and must meet the specifications of the on-chip SDRAM controller of the processor being used in order to be able to gluelessly interface to it.

Choosing the appropriate SDRAM

As an example, let's examine the ADSP-TS201S TigerSHARC and the ADSP-BF533 Blackfin processors and their compatibility with different SDRAM devices.

The ADSP-TS201S TigerSHARC Processor On-Chip SDRAM Controller

Before an SDRAM device can be selected, the user needs to understand the features and specifications of the chosen processor.

SDRAM Controller Features

With the factors previously explained in mind, these are the relevant ADSP-TS201S processor on-chip SDRAM controller characteristics for choosing the appropriate memory device:

- Supported operating Voltage
 - 3.3 and 2.5 V
- Maximum supported operating Frequency
 - 125 MHz
- Maximum supported memory
 - 256 Mbytes (64 M x 32 bits or 32 M x 64 bits) per external SDRAM bank
- Number of internal SDRAM banks
 - 2 or 4 banks.
- Column Address Strobe (CAS) latency
 - Programmable value: 1 to 3 system clock cycles (SCLK)
- Refresh rate
 - Programmable value: 32 to 64 ms.
- Burst Length
 - Full page burst
- Page size
 - Programmable value to: 256, 512 or 1024 words.
- Initialization sequence
 - Programmable sequence: MRS⇒REF, or REF⇒MRS.

For the aid of this example, devices A and B have been selected. Are these two SDRAM devices compatible with the ADSP-TS201S

TigerSHARC Processor? Let's look at the different specifications to be met:

SDRAM Features	ADSP-TS201S SDRAM Controller	SDRAM "A" 1 Meg x 32 x 4 banks	OK	SDRAM "B" 4 Meg x 32 x 2 banks	OK
Voltage	2.5 or 3.3 V	3.3 V	✓	3.3 V	✓
Max. Frequency	125 MHz	143/166 MHz	✓	100/133 MHz	✓
Max. Mem. Size	64 Mx32 or 32 Mx64 (256 Mbytes) per external SDRAM bank	16 Mbytes	✓	32 Mbytes	✓
Supported I/O	x32, x64	x32	✓	x32	✓
Number of SDRAM Banks	2 or 4 banks	4 banks	✓	2 banks	✓
CAS Latency	1 to 3 cycles	1 to 3 cycles	✓	1 to 3 cycles	✓
Refresh Rate	32 and 64 ms	64 ms	✓	64 ms	✓
Burst Length	Full-page burst	1,2,4,8 or Full-page	✓	1	✗
Page Size	256, 512, and 1024	256	✓	2048	✗
Init. Sequence	MRS⇒REF or REF⇒MRS	REF⇒MRS	✓	MRS⇒REF	✓

Table 1. ADSP-TS201S TigerSHARC Processor and SDRAMs compatibility

As it can be seen from the table above, device B does not meet all specifications: it only supports burst length of one (and not full page burst) and its page size is 2048 words (which is bigger than the maximum supported page size of 1024 words).

On the other side, it can be seen that device A meets all requirements, and therefore, it can be properly interfaced to the ADSP-TS201S TigerSHARC Processor.

Setting up the SDRAM Controller

Now that a compatible SDRAM device has been selected (SDRAM A), the next step is to properly configure the SDRAM control register

(SDRCON) according to the memory specifications given in Table 1.

SDRCON

The initial value of the SDRCON register after reset is zero, meaning that the SDRAM is disabled. The bit descriptions for this register are shown in Figure 1. Note that although this is a 32-bit register, only the lower 16-bits are shown. The upper 16-bits are reserved and should always be set to zero.

For more details, please refer to *SDRAM Interface* chapter of the *ADSP-TS201 TigerSHARC Processor Hardware Reference*.

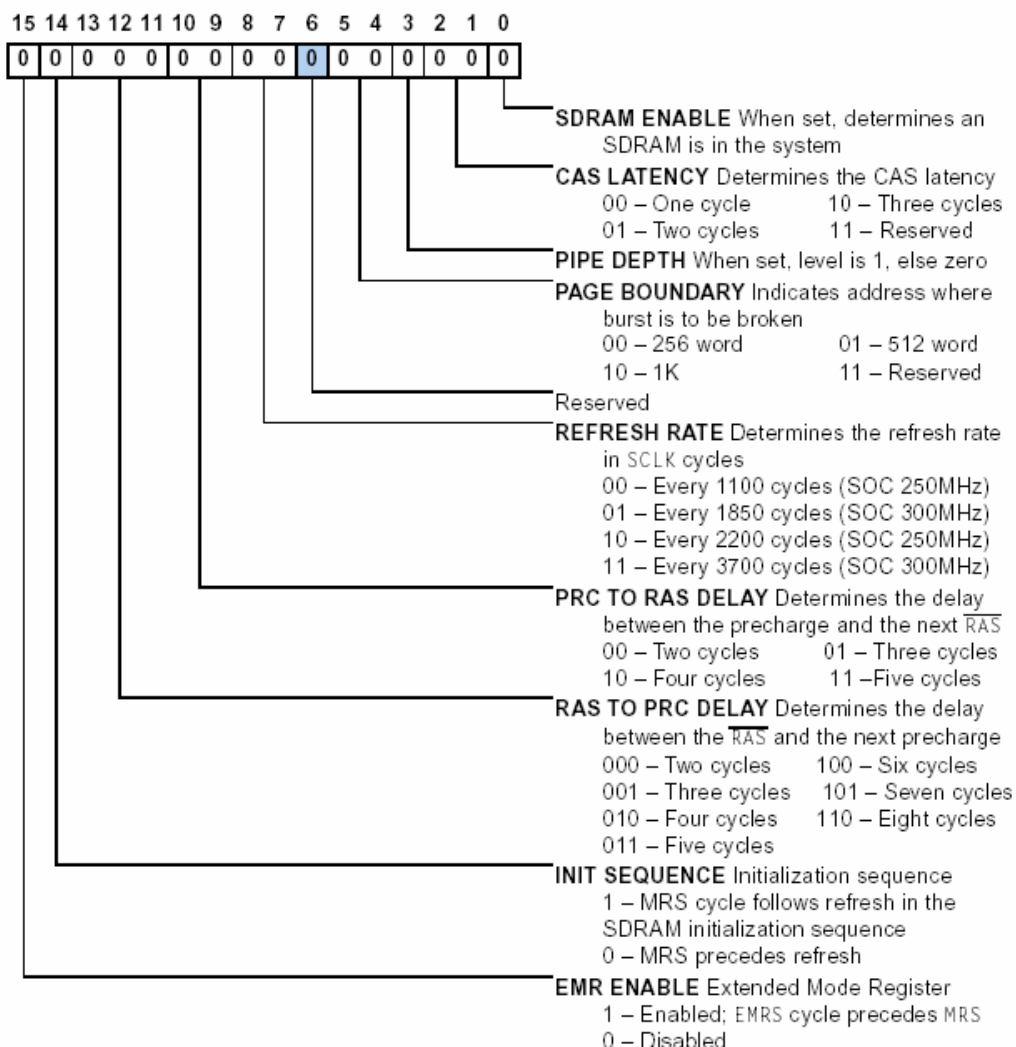


Figure 1. ADSP-TS201S SDRAM Control Register (SDRCON)

So how do we correctly set up the SDRAM Control register (SDRCON)? Let's have a look at a typical SDRAM device datasheet to determine the settings for the different bits:

- **SDRAM ENABLE.** This bit must be set when SDRAM is present in the system (**SDRCON_ENBL**).



To use the above bit definition (**SDRCON_ENBL**), the file *defTS201.h* should be included in the source code (see Code 1). This file comes with the VisualDSP++™ 32-bit Tools and can be found in the directory:

C:\...\AnalogDevices\VisualDSP\TS\include.


- **CAS LATENCY.** This parameter specifies the delay between a read command and the time data becomes available. It does not apply to write accesses. CAS Latency is generally specified in the datasheet as shown in Table 2.

SPEED	ALLOWABLE OPERATING FREQUENCY (MHz)		
	CAS LATENCY=1	CAS LATENCY=2	CAS LATENCY=3
-6	≤50	≤100	≤166
-7	≤50	≤100	≤143

Table 2. SDRAM "A" CAS Latency

Assuming the external port runs with a 100MHz system clock (SCLK), the selected CAS LATENCY is 2 (**SDRCON_CLAT2**).

Note that, as specified in Table 1, the maximum supported SCLK frequency by the ADSP-TS201S is 125 MHz. The selected frequency for this example, 100 MHz, corresponds to the default value of the ADSP-TS201S EZ-KIT Lite™.

 Some SDRAM timing specifications (*CL*, *tRAS*, *tRP*, etc) may vary depending on the speed grade of the SDRAM being used.

Settings in this particular example are optimized for a dedicated operating frequency (100 MHz) and speed grade part (-6). Variations in the clock frequency and/or speed grade of the SDRAM device also require modifying the parameter settings.

- **PIPE DEPTH.** In systems where several SDRAMs are used in parallel, and external buffers are needed, this bit should be enabled.

This is valid if the nominal capacitive pin loading is exceeded (30 pF/pin). In this particular example (ADSP-TS201S EZ-KIT Lite), there are only two SDRAMs where no buffering of the signals is needed (SDRAM pin capacitance $2 \times 5 \text{ pF} + 10 \text{ pF (PCB)} \approx 20 \text{ pF}$). Therefore, this bit should be cleared (**SDRCON_PIPE1**).

- **PAGE BOUNDARY.** These bits define the page size, in number of words, of the SDRAM's banks. This number corresponds to the number of addressable columns.

	4 Meg x 32
Configuration	1 Meg x 32 x 4 banks
Refresh Count	4K
Row Addressing	4K (A0-A11)
Bank Addressing	4 (BA0, BA1)
Column Addressing	256 (A0-A7)

Table 3. SDRAM "A" Specifications

As it can be seen in Table 3, the maximum number of addressable columns is 256 (A0-7). Thus, the page size should be configured to 256 (**SDRCON_PG256**).

- **REFRESH RATE.** These bits select the refresh counter to coordinate the Processor's SOC clock rate (SOCCLK) with the SDRAM device's required refresh rate.

The refresh count is provided in Table 3 as 4 K, and is also generally listed under the SDRAM features list as:

64 ms, 4,096-cycle refresh (15,6 μs/row)

With this in mind, the refresh rate is calculated as follows:

$$\text{Cycles} = \left(\text{SOCCLK} \cdot \frac{t_{REF}}{\text{Rows}} \right)$$

Where: *SOCCLK* = 250 MHz (default ADSP-TS201S EZ-KIT Lite value)
tREF = SDRAM refresh period
Rows = number of row addresses

Therefore,

$$\begin{aligned} \text{Refresh rate} &= 250 \text{ MHz} \times 15,6 \mu\text{s} \\ &= 3900 \text{ cycles} \end{aligned}$$

In order to be able to guarantee that this number is met, a refresh rate equal to or smaller than 3900 cycles should be selected. In this case, and since the processor's controller supports up to 3700 cycles only, this should be the selected refresh rate (**SDRCON_REF3700**).

- **PRC TO RAS DELAY.** This parameter determines the Precharge to RAS delay, which is typically given in the datasheet as *tRP*.

Table 4 illustrates some of the SDRAM timing specifications that can be found in the datasheet. As it can be seen, the device with speed grade -6 has $tRP_{min} = 18ns$. At

100 MHz, this gives a minimum time of 1.8 cycles. Therefore, tRP should be set to 2 cycles (**SDRCON_PC2RAS2**).

AC CHARACTERISTICS		-6		-7		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS
ACTIVE to PRECHARGE command	$tRAS$	42	120K	42	120K	ns
ACTIVE to ACTIVE command period	tRC	60		70		ns
AUTO REFRESH period	$tRFC$	60		70		ns
ACTIVE to READ or WRITE delay	$tRCD$	18		20		ns
Refresh period (4,096 rows)	$tREF$		64		64	ms
PRECHARGE command period	tRP	18		20		ns

Table 4. Relevant SDRAM “A” Timing Specifications

- **RAS TO PRC DELAY:** This parameter determines the RAS to Precharge delay, which is typically given in the datasheet as $tRAS$.

As shown in Table 4, this SDRAM device has $tRAS_{min} = 42 ns$. At 100 MHz, this gives a minimum time of 4.2 cycles. Therefore, $tRAS$ should be set to 5 cycles (**SDRCON_RAS2PC5**).

- **INIT SEQUENCE:** This bit determines the SDRAM initialization sequence at power up. From the *Initialization* section in the datasheet:

“[...] Once the 100 μ s delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied.

[...] Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for Mode Register programming.”

This means that the device minimum requirements after power up are:

$$PRE + 2 \times \text{Autorefresh} + MRS$$

When setting this bit to 1 the controller issues the following sequence of commands:

$$PRE + 8 \times \text{Autorefresh} + MRS$$

This meets the power-up timing specifications of the selected SDRAM. Therefore, this bit should be set (**SDRCON_INIT**).

- **EMR ENABLE.** This bit should only be set when interfacing to Low-Power SDRAM (2.5 Volts) devices. Otherwise, this bit should remain cleared.

From the datasheet *Features* list:

Single +3.3 V ± 0.3 V power supply

Therefore, since this is a standard SDRAM device, this bit should be cleared (**SDRCON_EMRS**).

Thus, with the above settings in mind, the SDRCON register should be set to:

```
#include <defts201.h>

xr0 = SDRCON_INIT          | SDRCON_RAS2PC5   | SDRCON_PC2RAS2   |
      SDRCON_REF3700      | SDRCON_PG256    | SDRCON_CLAT2     | SDRCON_ENBL;;
SDRCON = xr0;;
```

Code 1. SDRCON Settings using header file defts201.h

- 4 banks.
- Column Address Strobe (CAS) latency
 - Programmable value: 2 or 3 system clock cycles (SCLK)
- Refresh rate
 - Programmable value: 1 to 4095 system clock cycles (SCLK).
- Burst Length
 - Burst length of 1
- Page size

- Programmable value to: 512, 1024 2048 or 4096 bytes.
- Initialization sequence
 - Programmable sequence: MRS⇒REF, or REF⇒MRS.

For the aid of this example, devices C and D have been selected.

Are these two SDRAM devices compatible with the ADSP-BF533 Blackfin Processor? Let's look at the different specifications to be met:

SDRAM Features	ADSP-BF533 SDRAM Controller	SDRAM “C” 4 Meg x 16 x 2 banks	OK	SDRAM “D” 4 Meg x 16 x 4 banks	OK
Voltage	2.5 and 3.3 V	3.3 V	✓	3.3 V	✓
Max. Frequency	133 MHz	143/166 MHz	✓	100/143 MHz	✓
Max. Mem. Size	64 M x 16 (128 Mbytes)	16 Mbytes	✓	32 Mbytes	✓
Supported I/O	x16	x16	✓	x16	✓
Number of SDRAM Banks	4 banks	2 banks	✗	4 banks	✓
CAS Latency	2 or 3 cycles	1 to 3 cycles	✓	1 to 3 cycles	✓
Refresh Rate	Programmable (SDRRC)	64 ms	✓	64 ms	✓
Burst Length	1	Full-page	✗	1,2,4,8 or Full-page	✓
Page Size (bytes)	512, 1024, 2048 and 4096	2048	✓	1024	✓
Init. Sequence	MRS⇒REF or REF⇒MRS	REF⇒MRS	✓	MRS⇒REF	✓

Table 5. ADSP-BF533 Blackfin Processor and SDRAMs compatibility

As it can be seen from the table above, device C does not meet all specifications: it has 2 banks (4 banks supported only) and it supports full page burst (burst length of one supported only).

On the other side, it can be seen that device D meets all requirements, and therefore, it can be properly interfaced to the ADSP-BF533 Blackfin processor.

Setting up the SDRAM Controller

Now that a compatible SDRAM device has been selected (SDRAM D), the next step is to properly configure the different SDRAM control registers according to the memory specifications given in Table 5.

After a processor's hardware or software reset, the SDC clocks are enabled. However, the SDC must be configured and initialized.

In order to set up the SDC and start the SDRAM power-up sequence, the SDRAM Refresh Rate Control register (EBIU_SDRRC), the SDRAM Memory Bank Control register (EBIU_SDBCTL), and SDRAM Memory Global Control register (EBIU_SDGCTL) must be written, and a transfer must be started to SDRAM address space.

The following sections will briefly describe each one of the registers mentioned above as well as their bit descriptions.

EBIU_SDGCTL

The SDRAM Memory Global Control Register (SDGCTL) includes all programmable parameters associated with the SDRAM access timing and configuration.

The bit descriptions for EBIU_SDGCTL are shown in Figure 2 and Figure 3.

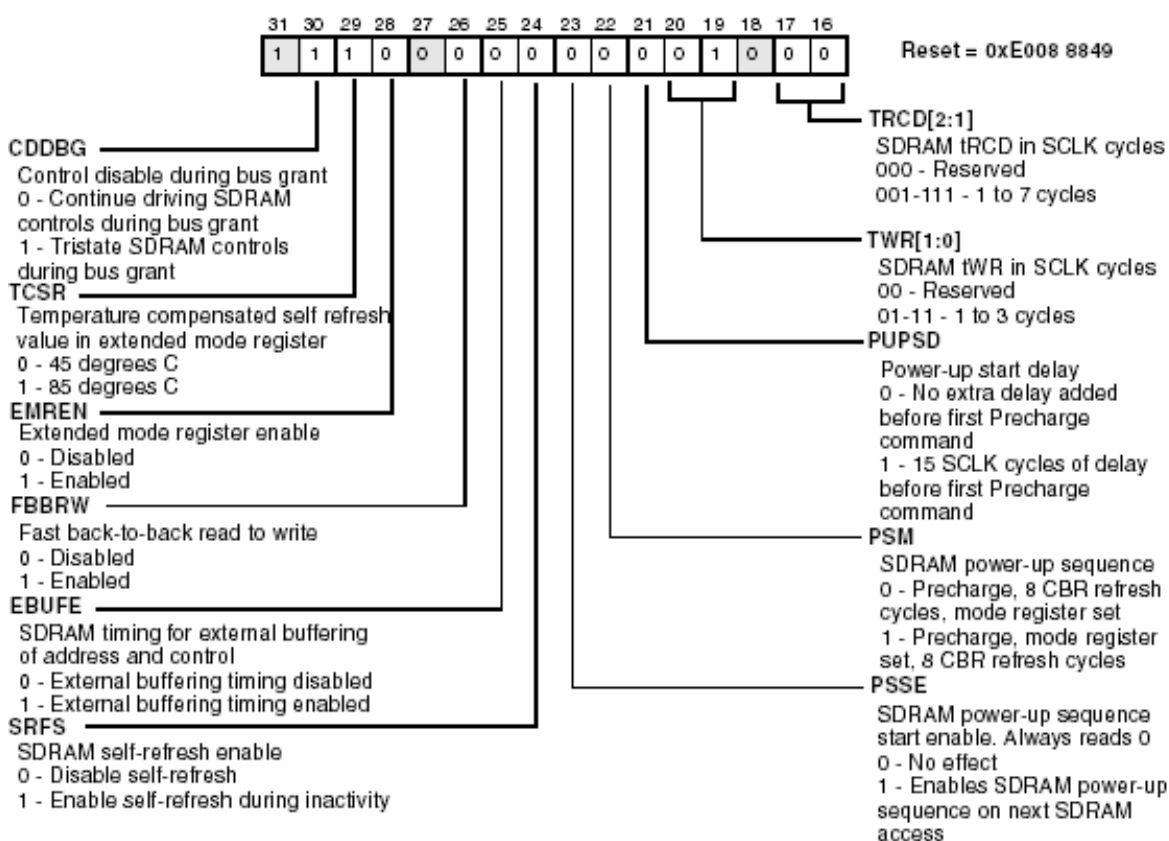


Figure 2. ADSP-BF533 SDRAM EBIU_SDGCTL Register – Upper 16-bits

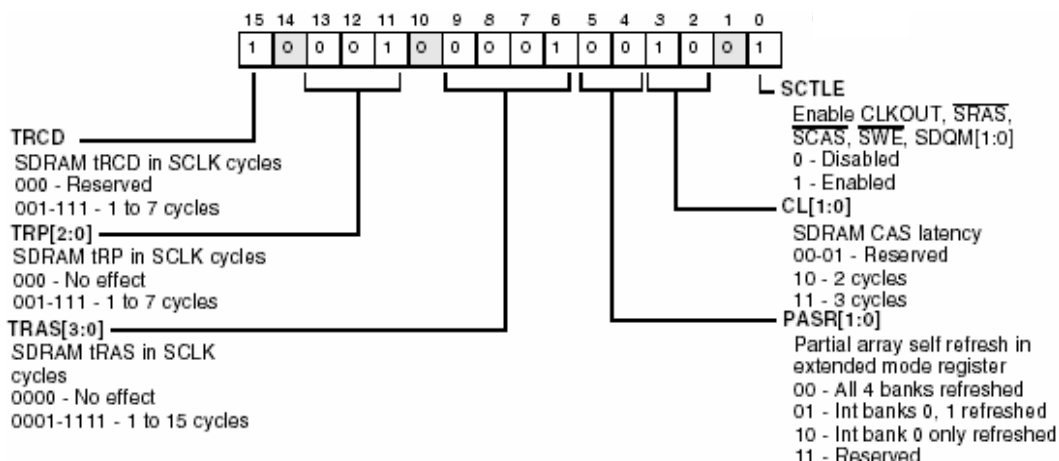


Figure 3. ADSP-BF533 SDRAM EBIU_SDGCTL Register – Lower 16-bits

So how do we correctly set up the SDRAM Global Control register (EBIU_SDGCTL)? Let's have a look at a typical SDRAM datasheet to determine the settings for the different bits:

- **SCTL.** This bit must be set for SDC operation and is enabled by default at reset (**SCTL**).

To use the above bit definition (**SCTL**), the file *defBF533.h* should be included in the source code (see Code 3). This file comes with the VisualDSP++ 16-bit Tools and can be found in the directory:

```
C:\.\AnalogDevices\VisualDSP\Blackfin\include
```

- **CL.** This parameter specifies the delay between a read command and the time data becomes available. It does not apply to write accesses. CAS Latency is generally specified in the datasheet as shown in Table 6.

SPEED	ALLOWABLE OPERATING FREQUENCY (MHz)	
	CAS LATENCY = 2	CAS LATENCY = 3
-7E	≤ 133	≤ 143
-75	≤ 100	≤ 133

Table 6. SDRAM “D” CAS Latency

Assuming the external port runs with a 54MHz system clock (SCLK), the selected CAS LATENCY is 2 (**CL_2**).

Note that, as specified in Table 5, the maximum supported SCLK frequency by the ADSP-BF533 is 133 MHz. The selected frequency for this example, 54 MHz, corresponds to the default value of the ADSP-BF533 EZ-KIT Lite.

Some SDRAM timing specifications (*CL*, *tRAS*, *tRP*, etc) may vary depending on the speed grade of the SDRAM being used.

Settings in this particular example are optimized for a dedicated operating frequency (54 MHz) and speed grade part (-75). Variations in the clock frequency and/or speed grade of the SDRAM device also require modifying the parameter settings.

- **PASR.** When EMREN (Extended Mode Register Enable) is set, the PASR bits (in combination with the TCSR bit) control the value written to the Extended Mode Register. This only applies for mobile low-power SDRAMs (2.5 V). Since SDRAM “D” is standard LVTTTL (3.3 V), these bits can be ignored (**PASR_X**).

- **TRAS.** This parameter determines the RAS to Precharge delay, which is typically given in the datasheet as *tRAS*.

Table 7 illustrates some of the SDRAM timing specifications that can be found in the datasheet. As it can be seen, this SDRAM device (speed grade -75) has $t_{RASmin} = 44$ ns. At 54 MHz, this gives a minimum time of 2.38 cycles. Therefore, t_{RAS} should be set to 3 cycles (**TRAS_3**).

- **TRP.** This parameter determines the Precharge to RAS delay, which is typically given in the datasheet as t_{RP} .

As shown in Table 7, the device with speed grade -75 has $t_{RPmin} = 20$ ns. At 54 MHz, this gives a minimum time of 1.08 cycles. Therefore, t_{RP} should be set to 2 cycles (**TRP_2**).

- **TRCD.** This parameter determines the delay between bank activation and the first read/write from/to SDRAM. It is typically given as t_{RCD} .

From Table 7, the device with speed grade -75 has $t_{RCDmin} = 20$ ns. At 54 MHz, this gives a minimum time of 1.08 cycles. Therefore, t_{RCD} should be set to 2 cycles (**TRCD_2**).

- **TWR.** This parameter determines the delay between a write and a Precharge command. It is typically given as t_{WR} .

As shown in Table 7, the device with speed grade -75 has $t_{WRmin} = 1\text{CLK} + 7.5$ ns = 26 ns. At 54 MHz, this gives a minimum time of 1.4 cycles. Therefore, t_{WR} should be set to 2 cycles (**TRW_2**).

AC CHARACTERISTICS		-7E		-75		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS
ACTIVE to PRECHARGE command	t_{RAS}	37	120,000	44	120,000	ns
ACTIVE to ACTIVE command period	t_{RC}	60		66		ns
ACTIVE to READ or WRITE delay	t_{RCD}	15		20		ns
Refresh period (8,192 rows)	t_{REF}		64		64	ms
AUTO REFRESH period	t_{RFC}	66		66		ns
PRECHARGE command period	t_{RP}	15		20		ns
ACTIVE bank a to ACTIVE bank b command	t_{RRD}	14		15		ns
Transition time	t_T	0.3	1.2	0.3	1.2	ns
WRITE recovery time	t_{WR}	1 CLK+		1 CLK+		ns
		7ns		7.5ns		
		14		15		ns
Exit SELF REFRESH to ACTIVE command	t_{XSR}	67		75		ns

Table 7. Relevant SDRAM “D” Timing Specifications



The value of t_{XSR} is equal to $t_{RAS} + t_{RP}$. This is fixed by the controller. Thus, the user *must* make sure that the specification for t_{XSR} is met when selecting the values for t_{RAS} and t_{RP} .

If $t_{RAS} + t_{RP}$ does not meet the

specifications for t_{XSR} , t_{RAS} or t_{RP} should be increased by 1. Typically, increasing t_{RAS} gives better performance, since it is used less often by the controller.

- **PUPSD.** The Power-up Start Delay bit optionally delays the power-up start sequence

for 15 SCLK cycles. This is useful for multiprocessing systems sharing an external SDRAM.

Since this example is based on the ADSP-BF533 EZ-KIT Lite (single processor system), the setting for this bit does not apply (**PUPSD**).

- **PSM.** This bit determines the SDRAM power-up sequence. From the *Initialization* section in the datasheet:

“[...] Once the 100 μs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied.

[...] Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for Mode Register programming.”

This means that the device minimum requirements after power up are:

PRE + 2×Autorefresh + MRS

When clearing this bit (=0) the controller issues the following sequence of commands:

PRE + 8×Autorefresh + MRS

This meets the power up timing specifications of the selected SDRAM device. Therefore, this bit should be cleared (**PSM**).

- **PSSE.** The Power-up Sequence Start enable bit must be set to 1 to enable the SDRAM power-up sequence (**PSSE**).



A read or write access must be done to enable SDRAM address space in order to have the external bus granted to the SDC so that the SDRAM power-up sequence may occur.

- **SRFS.** When setting the Self-Refresh bit (=1), the SDC completes any active transfers and then puts the SDRAM into self-refresh mode. The next access to SDRAM will take the device out of self-refresh mode, performing the transfer to or from SDRAM.

This mode is used to reduce the application’s power consumption to a minimum when the SDRAM is not being accessed for an extended period of time. This does not apply for this example, therefore this bit should be cleared (**SRFS**).

- **EBUFE.** In systems where several SDRAM devices are used in parallel, and external buffers are needed, this bit should be enabled (=1).

This is valid if the nominal capacitive pin loading is exceeded (50 pF/pin) In this particular example (ADSP-BF533 EZ-KIT Lite), there is only one SDRAM where no buffering of the signals is needed (SDRAM pin capacitance 5 pF+10 pF (PCB) ≈ 15 pF). Therefore, this bit should be cleared (**EBUFE**).

- **FBBRW.** The Fast Back-to-Back Read to Write bit enables SDRAM read followed by write to occur on consecutive cycles. In many systems, this is not possible because the turnoff time of the SDRAM data pins is too long. When this bit is 0, a clock cycle is inserted between read accesses followed by write accesses.

For this example, an extra cycle is added between read and write transactions, therefore this bit should be cleared (**FBBRW**).

- **EMREN.** This bit should only be set when interfacing to mobile low-power SDRAM (2.5 V) devices. Otherwise, this bit should remain cleared.

From the SDRAM “D” datasheet *Features* list:

Single +3.3 V ±0.3 V power supply

Therefore, since this is a standard LVTTL (3.3 V) SDRAM device, this bit should be cleared. (**EMREN**)

- **TCSR.** When EMREN (Extended Mode Register Enable) is set, the TCSR bit (in combination with the PASR bits) controls the value written to the Extended Mode Register.

This only applies for mobile low-power SDRAMs (2.5 V). Since SDRAM “D” is standard LVTTL (3.3 V), this bit can be ignored (**TCSR**).


- **CDDBG.** The Control Disable During Bus Grant bit is used to enable or disable the SDRAM control signals when the external memory interface is granted to an external controller.

If this bit is set (=1), the control signals are three-stated when bus grant is active.

Otherwise, these signals continue to be driven during grant.

In this example, the control signals are not shared with any external controller, therefore this bit should be cleared (**CDDBG**).

A programming example of the EBIU_SDGCTL SDRAM control register is shown at the end of this section (Code 3).

 ALL reserved bits in this register must always be written with zeros.

EBIU_SDBCTL

The SDRAM Memory Bank Control Register includes external bank specific programmable parameters of the SDRAM. This register is 16-bit wide and uses the access timing parameters defined in the EBIU_SDGCTL register.

The bit descriptions for EBIU_SDBCTL are shown in Figure 4.

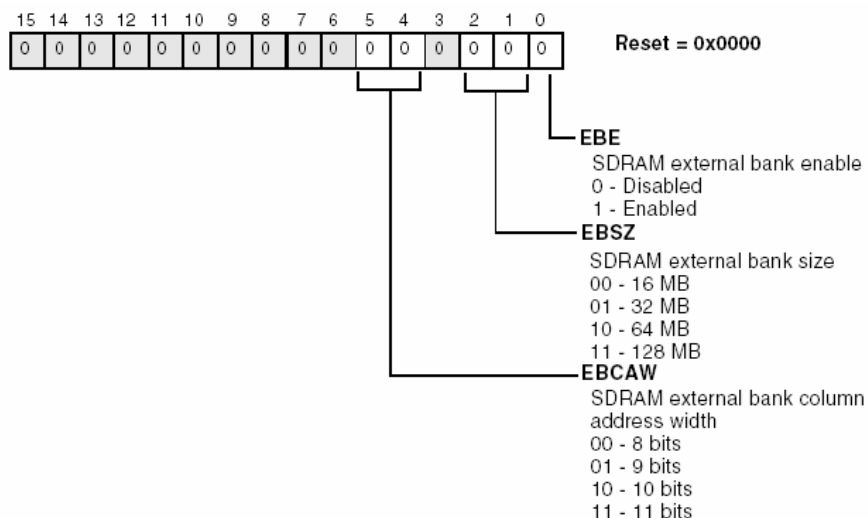


Figure 4. ADSP-BF533 SDRAM Bank Control Register (EBIU_SDBCTL)

- **EBE.** This bit is used to enable or disable the external SDRAM bank. This bit must be enabled when accessing the external

SDRAM bank. If disabled, any access to SDRAM address space generates an internal

error. Therefore, this bit should be set to 1 (**EBE**).


- **EBSZ**. This bit determines the SDRAM External Bank Size according to the density and I/O configuration of the SDRAM device used.

In this example, the selected SDRAM (device “D” -Table 8) is: 16 M x 16. Therefore:

$$EBSZ = 16 M \times 16 = 256 Mbit = 32 Mbyte$$

Thus, the SDRAM External Bank Size should be set to 32 Mbyte (**EBSZ_32**).

For more details on the supported *EBSZ* encodings refer to the *SDRAM Configurations Supported* section of the *SDRAM Controller* in the *External Bus Interface Unit* chapter of the *ADSP-BF533 Blackfin Processor Hardware Reference*.

 Although the smallest supported SDRAM external bank size is 16Mbytes, smaller devices can also be interfaced to the ADSP-BF533.

In this case, the external bank size in SDBCTL should be configured to 16 Mbyte (**EBSZ_16**), but the user’s code should not access any SDRAM address outside the physical memory size of the SDRAM being used. Exceeding this range will result in looping back to the first SDRAM memory location corrupting existing data.

- **EBCAW**. These bits determine the SDRAM external bank column address width. As previously explained (Table 5) page sizes of 512 bytes, 1 Kbyte, 2 Kbytes and 4 Kbytes are supported.

	64 Meg x 4	32 Meg x 8	16 Meg x 16
Configuration	16 Meg x 4 x 4 banks	8 Meg x 8 x 4 banks	4 Meg x 16 x 4 banks
Refresh Count	8K	8K	8K
Row Addressing	8K (A0-A12)	8K (A0-A12)	8K (A0-A12)
Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column Addressing	2K (A0-A9, A11)	1K (A0-A9)	512 (A0-A8)

Table 8. SDRAM “D” Specifications

In order to be able to calculate the page size, the following formula is used:

$$16\text{-bit SDRAM banks: page size} = 2^{(CAW+1)}$$

where *CAW* is the column address width of the SDRAM, plus 1 because the SDRAM bank is 16 bits wide.

As shown in Table 8, the column address width for device “D” is 512 bits (A0-A8). Therefore, $EBCAW = 9$ bits (**EBCAW_9**).

Thus:

$$Page\ size = 2^{(9+1)} = 1024 = 1\ Kbyte$$

A programming example of the EBIU_SDBCTL SDRAM control register is shown at the end of this section (Code 3).

EBIU_SDRRC

The SDRAM Refresh Rate Control Register (EBIU_SDRRC) provides a flexible mechanism for specifying the Auto-Refresh timing.

Since the clock supplied to the SDRAM can vary, the SDC provides a programmable refresh counter which has a period based on the value programmed into the RDIV field of this register that coordinates the supplied clock rate with the SDRAM device’s required refresh rate.

The bit descriptions for EBIU_SDRRC are shown in Figure 5.

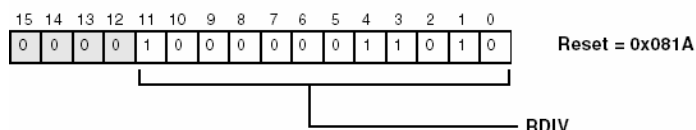


Figure 5. ADSP-BF533 EBIU_SDRRC Register

- **RDIV.** The value to be written to this register can be calculated using the following formula:

$$RDIV = ((f_{SCLK} \times t_{REF}) / NRA) - (t_{RAS} + t_{RP})$$

Where: f_{SCLK} = SDRAM clock frequency
 t_{REF} = SDRAM refresh period
 NRA = number of row addresses
 t_{RAS} = tRAS in clock cycles
 t_{RP} = tRP in clock cycles

For this example, the SCLK frequency is 54 MHz. The refresh count and number of rows are provided in Table 8 as 8K cycle period and 8K rows. The refresh period is also generally listed under the SDRAM features list as:

64 ms, 8,192-cycle refresh

tRAS and tRP are defined in EBIU_SDGCTL as 3 and 2 cycles respectively. With this in mind, the value for RDIV is calculated as follows:

$$RDIV = ((54 \text{ MHz} \times 64 \text{ ms}) / 8192) - (3+2) = 416.87 \approx 416 = 0x1A0 \text{ clock cycles}$$

Therefore, RDIV must be programmed to 0x1A0 (hex).

A programming example of the EBIU_SDRRC SDRAM control register is shown at the end of this section (Code 3).

EBIU_SDSTAT

In addition to the previously mentioned SDRAM control registers, an SDRAM Status Register (EBIU_SDSTAT) provides information on the state of the SDRAM controller, which can be used to determine when it is safe to alter the SDRAM controller parameters or simply as a debug aid.

The bit descriptions for EBIU_SDSTAT are shown in Figure 6.

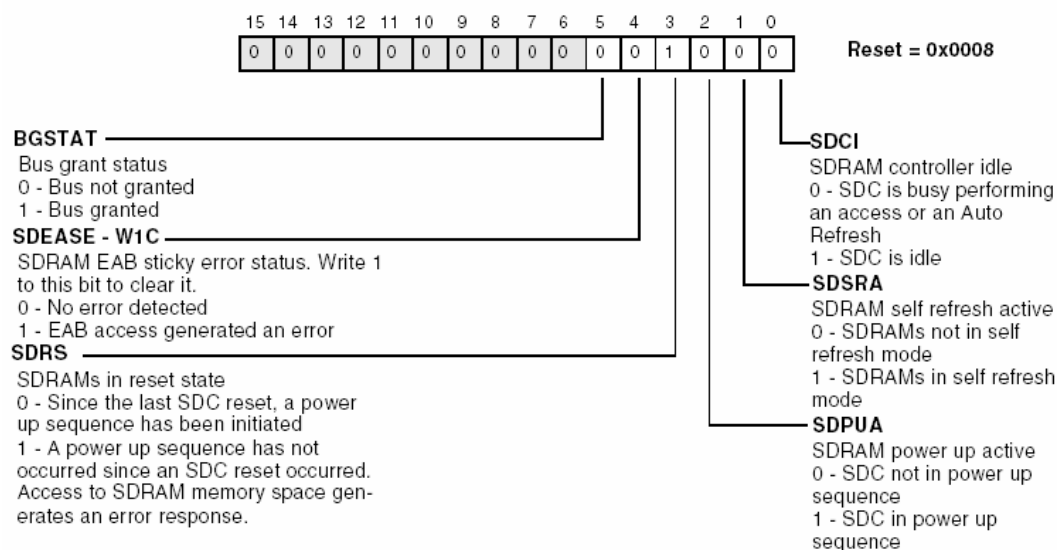


Figure 6. ADSP-BF533 SDRAM Status Register (EBIU_SDSTAT)

For more details on the SDRAM control registers, refer to the *SDRAM Controller* in the *External Bus Interface Unit* chapter of the *ADSP-BF533 Blackfin Processor Hardware Reference*.

With the settings for the EBIU_SDGCTL, EBIU_SDBCTL and EBIU_SDRRC registers previously discussed, the example code for the ADSP-BF533 EZ-KIT Lite would look as follows:

```
#include <defbf532.h>

//SDRAM Refresh Rate Control Register
P0.L = lo(EBIU_SDRRC); P0.H = hi(EBIU_SDRRC);
R0 = 0x01A0 (z);
w[P0] = R0;

//SDRAM Memory Bank Control Register
P0.L = lo(EBIU_SDBCTL); P0.H = hi(EBIU_SDBCTL);
R0 = EBE | EBSZ_32 | EBCAW_9 (z);
w[P0] = R0;

//SDRAM Memory Global Control Register
P0.L = lo(EBIU_SDGCTL); P0.H = hi(EBIU_SDGCTL);
R0 = 0x0; [P0] = R0;
R0.L = SCTL | CL_2 | TRAS_3 | TRP_2;
R0.H = TRCD_2 | TWR_2 | PSSE;
[P0] = R0;
```

Code 3. SDRAM Control Registers Settings using header file defBF532.h

As it can be seen in Code 3, any of the SDRAM control register bits that should be cleared (i.e. PSM, PUPSD, etc.) are simply ignored and not included in the bit settings above (note that the registers are zeroed before initialization).

In the case where these bit definitions were not used, the SDRAM control registers should be programmed as follows:

```
//SDRAM Refresh Rate Control Register
P0.L = lo(EBIU_SDRRC);
P0.H = hi(EBIU_SDRRC);
R0 = 0x01A0 (z);
w[P0] = R0;

//SDRAM Memory Bank Control Register
P0.L = lo(EBIU_SDBCTL);
P0.H = hi(EBIU_SDBCTL);
R0.L = 0x0013; // 0000 0000 00 01 0 01 1
// | -RESERVED- | | | | - SDRAM External Bank Enabled
// | | | | -- Ext.Bank Size = 32Mbyte
// | | | | ----- RESERVED
// | | | | ----- Ext.Bank CAW = 9 bits

R0.H = 0x0000;
[P0] = R0;

//SDRAM Memory Global Control Register
P0.L = lo(EBIU_SDGCTL);
P0.H = hi(EBIU_SDGCTL);
R0.L = 0x10C9; // 0 0 000 0 0000 00 10 0 1
// | | | | | | | | - SDRAM Control Enabled
// | | | | | | | | --- RESERVED
// | | | | | | | | ----- CAS LATENCY = 2
// | | | | | | | | ----- PASR = IRRELEVANT
// | | | | | | | | ----- TRAS = 3 cycles
// | | | | | | | | ----- RESERVED
// | | | | | | | | ----- TRP = 2 cycles
// | | | | | | | | ----- RESERVED
// | | | | | | | | ----- TRCD[1] = 2 cycles

R0.H = 0x0091; // 0 0 0 0 0 0 0 0 1 0 0 10 0 01
```


Refresh rate	600, 900 or 1200	1100, 2200, 1850, 3700
Burst Length	full page	full page
CL (CAS Latency)	1-3 cycles	1-3 cycles
Programmable Init Sequence	yes	yes
Extended MRS	-	yes

Table 9. TigerSHARC Processors with On-Chip SDRAM Controller

SDRAM Features	ADSP-BF535	ADSP-BF533/2/1
Operating Voltage	3.3V	3.3V and 2.5V
Max. Clock Frequency	133 MHz	133 MHz
Max. Memory Size	128 M x 32 (512 Mbytes)	64 M x 16 (128 Mbytes)
Supported Address Map	64, 128, 256, 512 Mbits	64, 128, 256, 512 Mbits
SDRAM Page Size (Byte)	512, 1024, 2048	512, 1024, 2048 or 4096
SDRAM I/O Data Capability	x16, x32	x16
Number of SDRAM Banks	4	4
Refresh rate	Programmable (SDRRC)	Programmable (SDRRC)
Burst Length	1	1
CL (CAS Latency)	2-3 cycles	2-3 cycles
Programmable Init Sequence	yes	yes
Extended MRS	-	yes

Table 10. Blackfin Processors with On-Chip SDRAM Controller

SDRAM Features	ADSP-21065L	ADSP-21161N
Operating Voltage	3.3 V	3.3 V
Max. Clock Frequency	66 MHz	100 MHz
Max. Memory Size	16 M x 32 (64 Mbytes)	64 M x 32 (256 Mbytes)
Supported Address Map	16, 64, 128 Mbits	16, 64, 128, 256 Mbits
SDRAM Page Size	256, 512, 1024	256, 512, 1024, 2048
SDRAM I/O Data Capability	x32	x32, x48 ²
Number of SDRAM Banks	2, 4	2, 4
Refresh rate	Programmable (SDRDIV)	Programmable (SDRDIV)
Burst Length	full page	1

² When link ports are not used.

CL (CAS Latency)	1-3 cycles	1-3 cycles
Programmable Init Sequence	yes	yes
Extended MRS	-	-

Table 11. SHARC DSPs with On-Chip SDRAM Controller

References

- [1] *ADSP-TS201 TigerSHARC Processor Hardware Reference*. First Edition, August 2003. Analog Devices, Inc.
- [2] *ADSP-TS201S TigerSHARC Embedded Processor Preliminary Datasheet*. Rev. PrG, Analog Devices, Inc.
- [3] *ADSP-BF531/ADSP-BF532/ADSP-BF533 Blackfin Embedded Processor Preliminary Datasheet*. Rev. PrB, Analog Devices, Inc.
- [4] *ADSP-BF533 Blackfin Processor Hardware Reference*. Preliminary Revision, March 2003. Analog Devices, Inc.
- [5] *128 Mb:x32 SDRAM Datasheet (MT48LC4M32B2)*. Revision January 2002, Micron Technology, Inc.
- [6] *256 Mb:x16 SDRAM Datasheet (MT48LC16M16B2)*. Revision F January 2003, Micron Technology, Inc.

Document History

Version	Description
Rev 2 – August 13, 2004 by Maikel Kokaly-Bannourah	Added tXSR information to the “Setting up SDRAM Controller” section of the Blackfin Processor chapter
Rev 1 – October 27, 2003 by Maikel Kokaly-Bannourah	Initial Release