



Static Voltage Scaling for ADSP-2148x SHARC® Processors

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Introduction

Typically, for Analog Devices DSPs and processors, minimum and maximum core operating voltage specifications provided in the datasheet (V_{DD_INT}) are fixed voltage values.

These traditional fixed datasheet voltage specifications need to be strictly adhered to, in order to ensure correct and reliable operation of the processor under all operating conditions including temperature and frequency.

There is an alternate voltage specification technique known as Static Voltage Scaling (SVS) that can provide significant performance benefits including higher frequency operation without a major increase in power consumption. That said, Static Voltage Scaling is only available on parts specifically designed for SVS operation. This includes certain ADSP-2148x SHARC® processor variants. For more details on supported devices and corresponding power consumption figures, please refer to the *ADSP-2148x SHARC processor datasheet*^[1].

This EE-note details the requirements to implement a SVS power supply system for ADSP-2148x devices specifically designed to support this feature, enabling core clock speeds of up to 450 MHz.

Implementing SVS on ADSP-2148x processors is enabled by:

1. The optimum V_{DD_INT} voltage for each device is factory programmed into a non-volatile processor register. This unique

voltage value can be read by software at first execution of code to set the external voltage regulator to the appropriate V_{DD_INT} voltage level for each system/device.

2. For reliable operation, the voltage regulator supplying V_{DD_INT} to the processor must be programmable to the exact voltage level required by the device. The recommended design is detailed in the [Programmable Regulator Implementation](#) section.

Note that most existing switching regulator designs that use a resistor divider feedback mechanism to set V_{DD_INT} can be converted to the required programmable regulator by utilizing a programmable resistor (Digipot) device as described next.

SVS Implementation

ADSP-2148x processors that support SVS include a 256-bit SVS_DAT register that contains the unique binary bit pattern corresponding to the value of V_{DD_INT} for each device.

As shown in [Figure 1](#), only a portion of the SVS_DAT register is used for storing the V_{DD_INT} specific information. The rest of this register is reserved.

Firstly, bit positions $SVS_DAT[191-128]$ and $SVS_DAT[255-192]$ are mirror duplicates of each other. This redundancy is implemented to ensure programmed data integrity and error correction.

The 256-bit serial register SVS_DAT can be treated as a sequence of 8 32-bit registers SVS_DAT_n (n=0, 1, 2, 3, 4, 5, 6 and 7). The register contents must be read using a specific sequence, as described in the accompanying example code.

As indicated in Figure 1, SVS_DAT₄ and SVS_DAT₅ (and duplicated SVS_DAT₆ and

SVS_DAT₇ respectively) contain the VDD_INT bits of interest. The register pair SVS_DAT₅:₄ correspond to SVS_DAT[191-128] and the register pair SVS_DAT₇:₆ correspond to SVS_DAT[255-192].

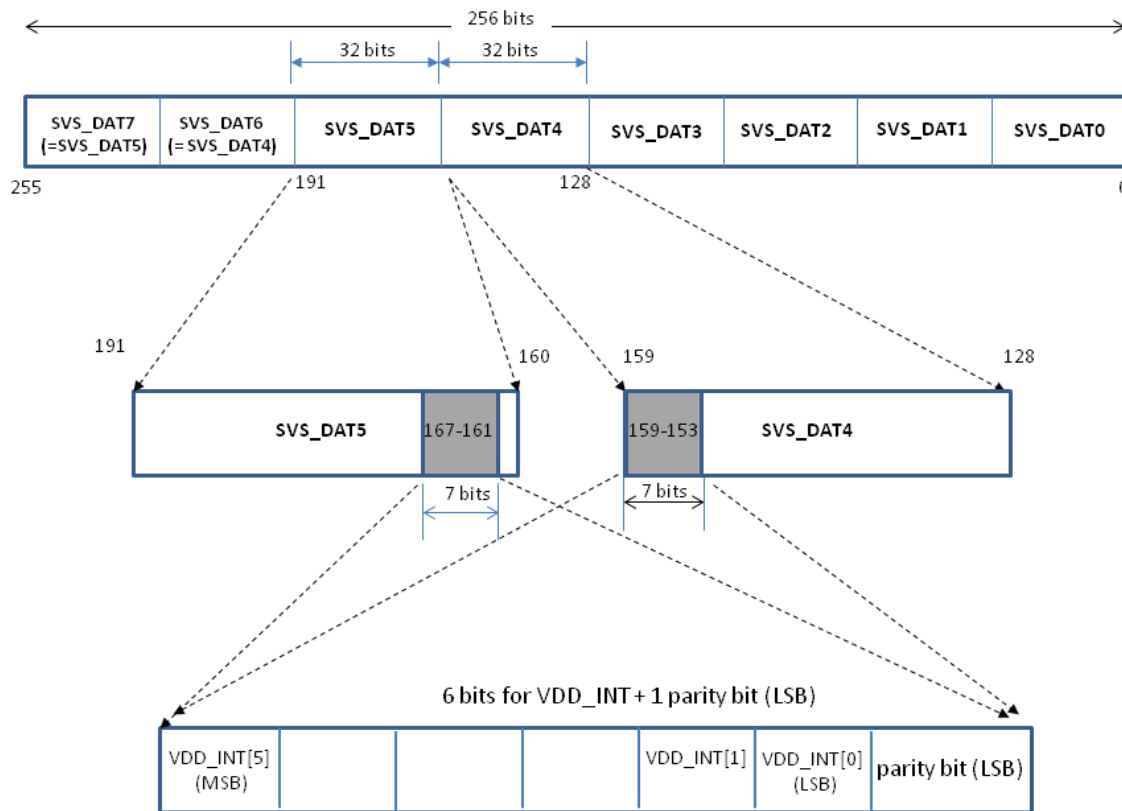


Figure 1. Positioning of VDD_INT information within SVS_DAT register

Built-in Redundancy for SVS_DAT bits

Two levels of redundancy/error checking are implemented in the process of storing the VDD_INT information within the SVS_DAT register. This is done to ensure that in the unlikely, but rare possibility that a bit within the VDD_INT field might be corrupted, it can be corrected for the vast majority of parts.

The first stage of error checking is to ensure that SVS_DAT₅:₄ contents are identical to the

SVS_DAT₇:₆ contents, and that VDD_INT contained in SVS_DAT₄ is identical to the copy in SVS_DAT₅, as well as SVS_DAT₆ and SVS_DAT₇.

The second stage of error checking is a parity check of each the VDD_INT value.

The software example code contained in the associated .ZIP file reads the contents of the four registers SVS_DAT₇:₄, performs the redundancy checks and implements a correction algorithm if any mismatches are detected.

Translating VDD_INT bit pattern values into nominal VDD_INT value

The VDD_INT values can range in value from a minimum of 0.65 Volts to a maximum value of 1.4375 Volts in step sizes of 0.0125 Volts. The following table (Table 1) shows the linear relationship between the voltage and corresponding binary value mapping.

VDD_INT value (Volts)	Bit Pattern (binary value)
0.6500	000000
0.6625	000001
0.6750	000010
....
....
1.4375 V	111111

Table 1. Translation of Bit pattern to corresponding VDD_INT value

Programmable Regulator Implementation

In order to implement an ADSP-2148x specific SVS, the system must be designed with a programmable VDD_INT voltage regulator. In addition, the system initialization code must incorporate the code provided in the associated .ZIP file (adapted to specific system needs, if any) in order to set the programmable voltage regulator to the required VDD_INT value.

Hardware

The attached ADSP-21489 schematics and reference design database contain the details for the required modifications in order to implement Static Voltage Scaling.

Figure 2 shows the power supply circuitry for a conventional fixed voltage regulator power supply. Note that Figure 2 includes both a 5V to 3.3V step-down regulator as well as a 1.1V switching regulator.

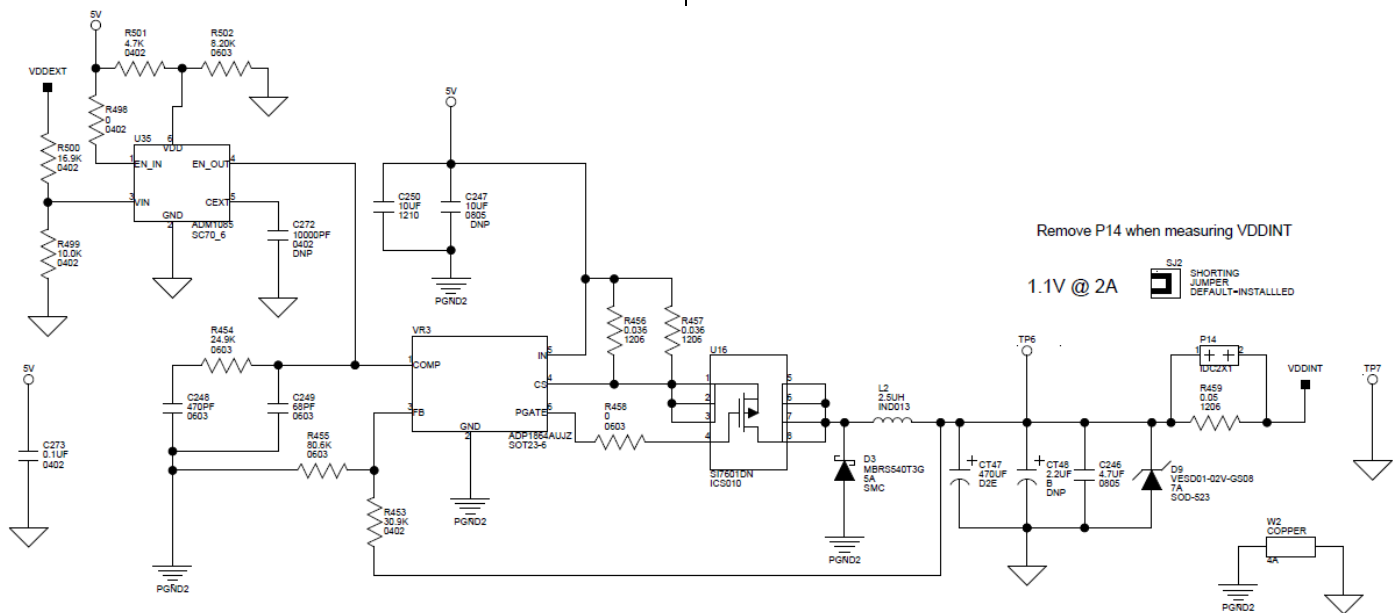


Figure 2 Power Supply portion of traditional EZ-Kit schematic that does not implement SVS

Figure 3 shows the required implementation for an SVS compliant programmable power supply. This reference implementation includes a AD5258BRMZ10 (PN:AD80/009Z-0)^[2] digipot and its associated resistor-divider circuitry, providing the feedback voltage to the ADP2114^[3] switching regulator that supplies VDD_INT.



For proper ADSP-2148x Static Voltage Scaling implementation, it's strongly recommended to use a $\pm 1\%$ accuracy voltage regulator, as per the attached reference design.

That said, customers may design their own programmable voltage regulator circuitry, as long as the required specifications are met. Additional guard-banding to the SVS_DAT value might be required, if an alternate regulator design is implemented. Please contact Analog Devices, Technical Support for specific programmable regulator design guidance including the use of an ADI digipot in the feedback path of other regulators.

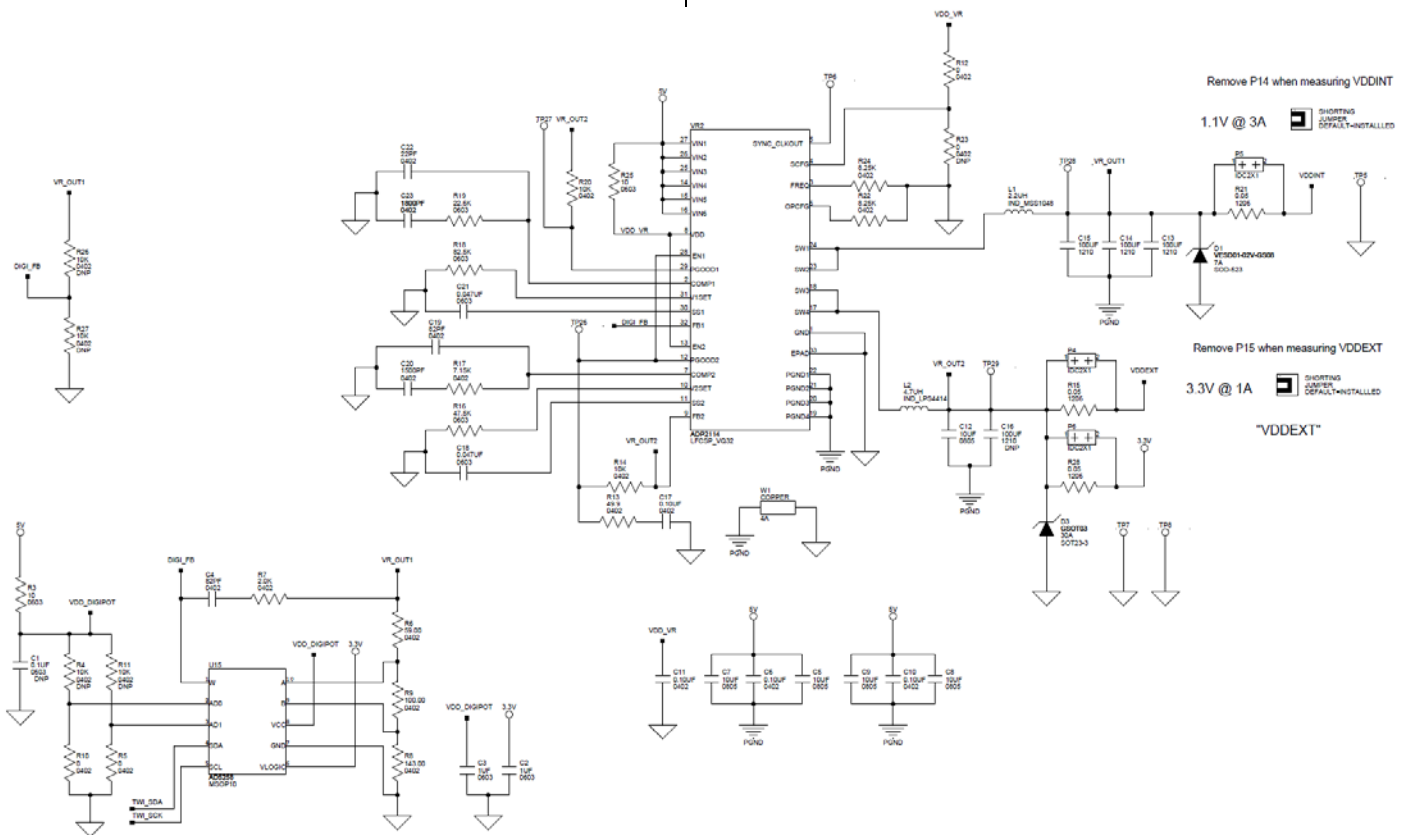


Figure 3. Required Power Supply portion of adjustable regulator for SVS VDD_INT operation

Software

The example code provided in the associated .ZIP file shows the steps involved in accessing and reading the contents of the SVS_DAT register of the device into the eight SVS_DATn 32-bit registers, the algorithm used for testing the checksums and arriving at the unique VDD_INT

for the part, as well as how to program the digipot step via the Two Wire Interface (TWI).

The flow-chart for the implemented algorithm to extract and calculate the VDD_INT bit information from the SVS_DAT register is shown in Figure 4.

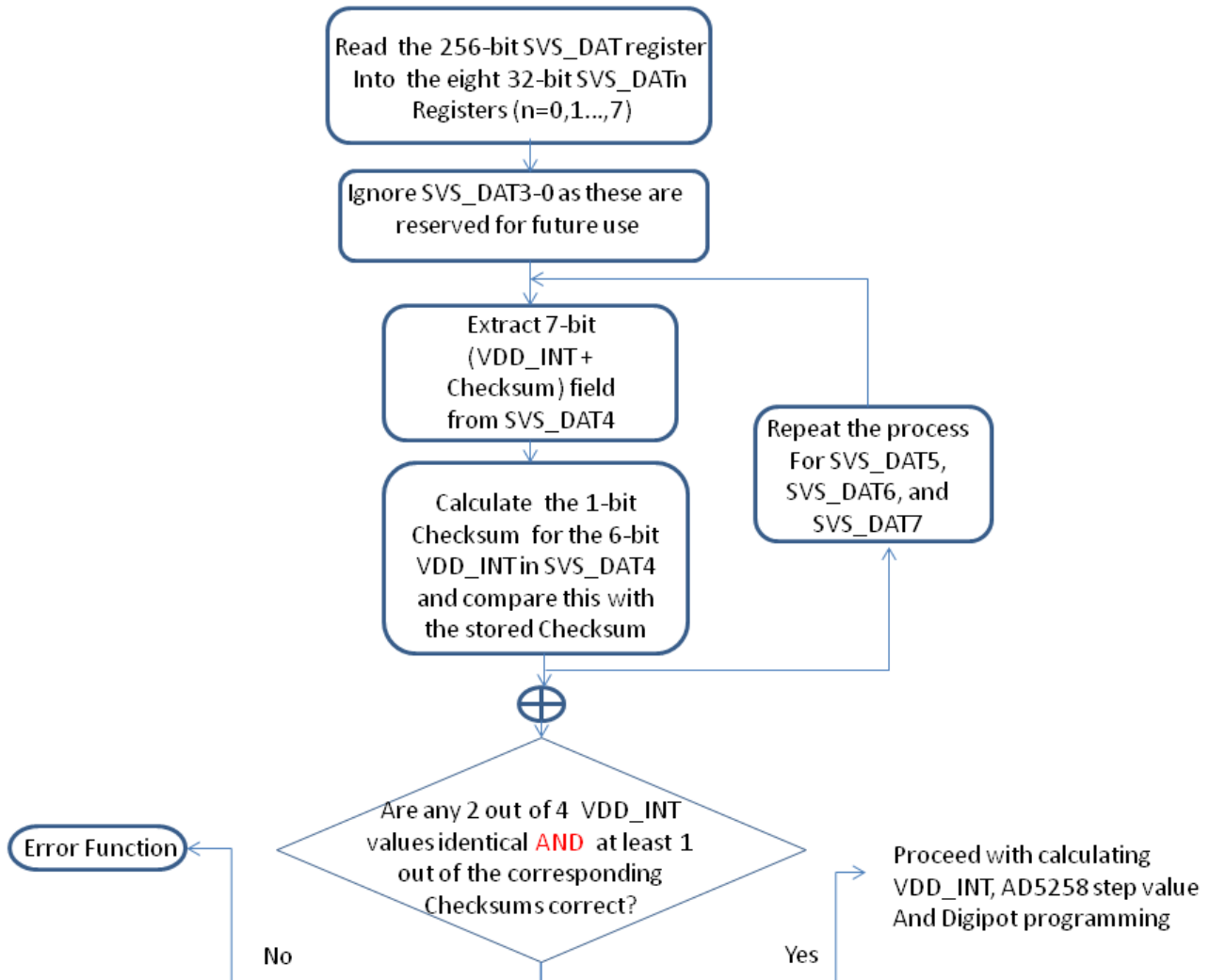


Figure 4. Algorithm for extracting and error-checking of SVS_DAT bits

The step value for programming the digipot, so that it can provide the appropriate V_{DD_INT} voltage to the ADP2114^[3] voltage regulator, is determined by Equation 1:

$$X = \frac{(180.72 - (143.0 * V_{DD_INT}))}{(1.55 * V_{DD_INT})}$$

Equation 1. Digipot step value calculation

where X is the digipot step value and, which is an integer number that can range from 0 to 64.



Equation 1 is only valid for the digipot and resistor-divider network provided in the required SVS reference design. Specifically, Equation 1 is true for the 64-bit AD5258BRMZ10^[2] with the following resistor values: $R_6=59\ \Omega$, $R_8=143\ \Omega$ and $R_9=100\ \Omega$.

For a different digipot or different resistors values, please refer to the corresponding device datasheet.

Also, note that in the provided example code, the step value that is programmed into the digipot is guardbanded by two step values less than what is determined by Equation 1. This results in a higher guardbanded voltage applied to the part.

For example, if the equation results in a step value of 11, the value programmed into the digipot is 9. This is regulator and board design specific in order to guarantee correct voltage at the processor under all possible operating and load transient conditions.

Alternatively, a look-up table containing the nominal V_{DD_INT} voltage and corresponding digipot step value can be used to arrive at the value that needs to be programmed into the digipot.

Incorporating SVS Init-code into System-level Application Code

Figure 5 shows the initialization code necessary to set the programmable regulator SVS V_{DD_INT} value. Note that the non-volatile memory contained within the AD5258BRMZ10^[2] digipot retains the step value programmed the first time. This is a benefit of using the digipot to control the switching regulator that results in a faster start-up time.

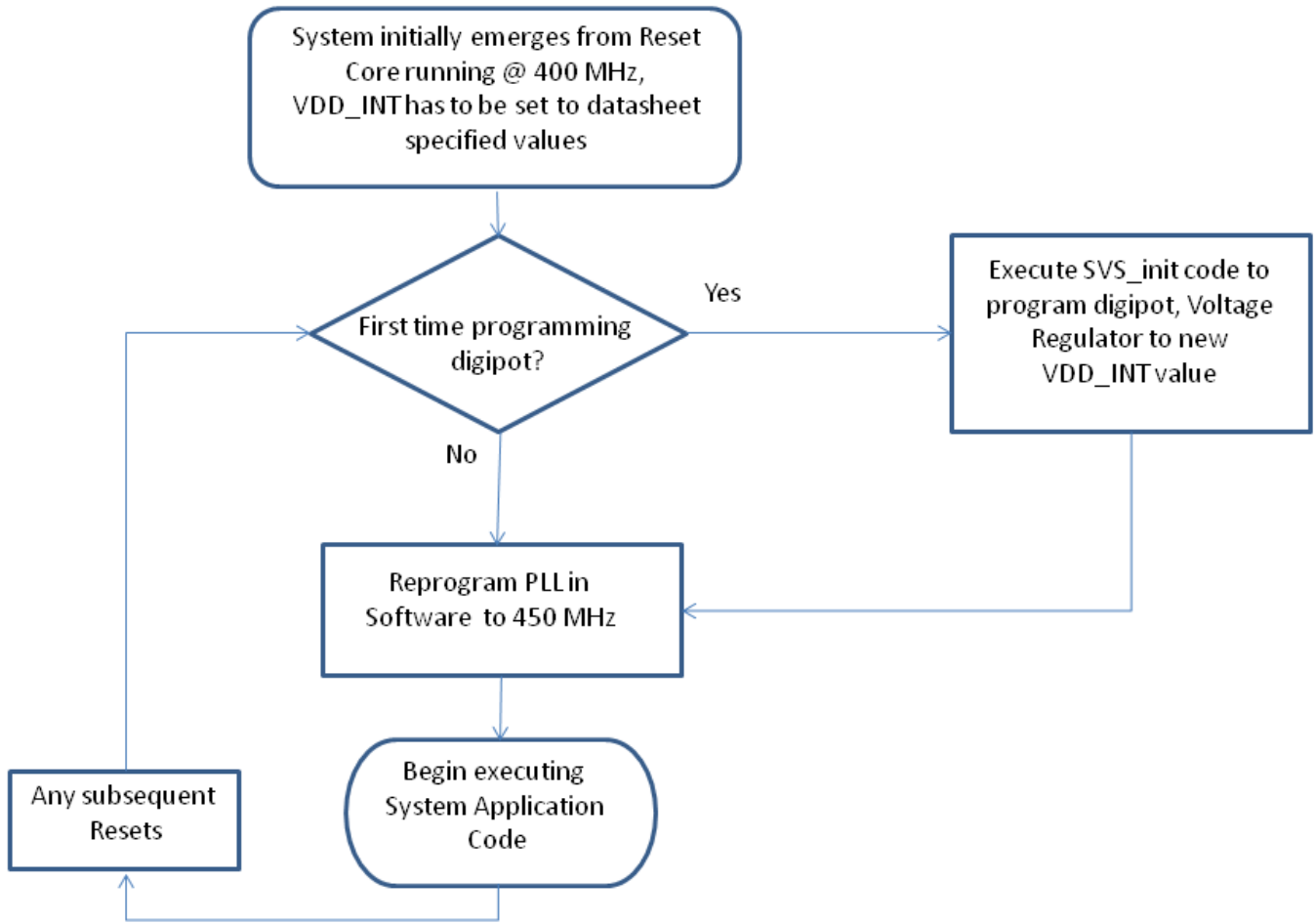


Figure 5 Incorporation of SVS code into System-level Application Code

Observed Load Transient Response

Figure 6 shows the V_{DD_INT} voltage transient response between full-load and no-load V_{DD_INT} measured at a test-point close to the processor. The test-code being executed by the DSP in the example shown alternates between the processor

executing a peak power consumption test vector, and executing NOP (no-operation) instructions. The purpose of this exercise is to measure the voltage transient response of the regulator between full-load and no-load conditions. As shown in Figure 6, the swing between the programmed V_{DD_INT} value and the peak offset is less than 2% even in the worst-case.

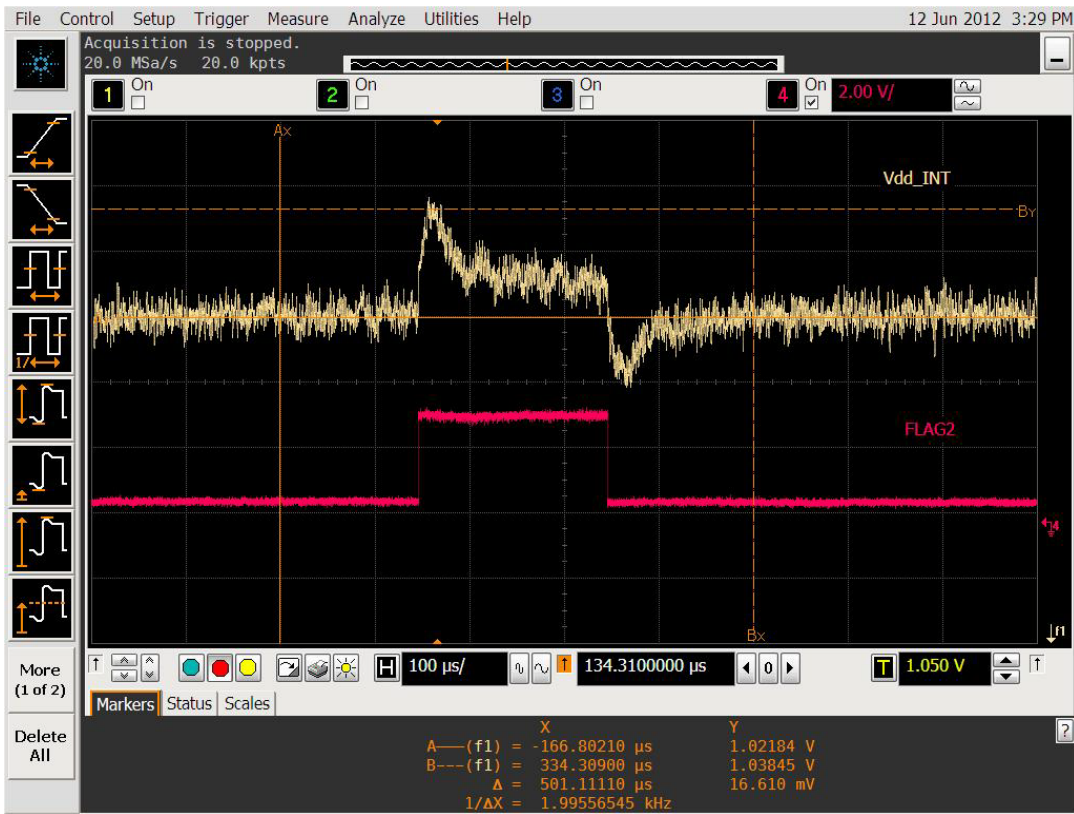


Figure 6 VDD_INT rise-and-drop between full-load, no-load, full-load for the ADP2114 regulator design

References

- [1] *ADSP-21483/21486/21487/21488/21489 SHARC Processor Data Sheet*. Rev B, March 2013. Analog Devices, Inc.
- [2] *AD5258 Nonvolatile, I2C®-Compatible 64-Position, Digital Potentiometer Data Sheet*. Rev C, May 2010. Analog Devices, Inc. (**NOTE: when ordering, reference specific ADI PN AD80/009Z-0**)
- [3] *ADP2114: Configurable, Dual 2 A/Single 4 A, Synchronous Step-Down DC-to-DC Regulator Data Sheet*. Rev 0, July 2009. Analog Devices, Inc.

Document History

Revision	Description
<i>Rev 1 – March 22, 2013 by Ramdas C. and Chirag P.</i>	Initial Release