Engineer-to-Engineer Note   EE-430

Migrating from ADSP-2156x to ADSP-SC59x Processors

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Introduction

This application note provides guidelines for transitioning from the ADSP-2156x processor to the ADSP-2159x/SC591/592/594 processor. It also discusses compatibility between the two processor families.

The ADSP-SC59x/2159x processor is a multi-core, high performance SoC with up to two SHARC+® DSPs and a Cortex-A5 Arm® core. The processor reaches speeds of up to 1 GHz. With a rich set of industry-leading system peripherals, multiple high performance on-chip accelerators, and large on-chip memory, the ADSP-SC59x/2159x processor is a natural choice to upgrade systems based on the ADSP-2156x processor. The Cortex-A5 core along with network interfaces such as GigE, 10/100 EMAC, CANFD, and the USBC controller make the SC59x/2159x processor an ideal choice for connected applications.

ⓘ   The term *ADSP-SC59x* processor includes the ADSP-SC591, ADSP-SC592, and ADSP-SC594 processors.

Pin Compatibility

The ADSP-SC59x/2159x processor provides an upgrade path to designs using ADSP-2156x processors. The ADSP-SC59x/2159x processor is available in two packages: Low Peripheral Count (LPC) and High Peripheral Count (HPC). Both packages are 17x17 mm, 400 ball BGA packages similar to the ADSP-2156x processor package. However, the HPC package has additional peripherals and general purpose I/O pins when compared with the ADSP-2156x processor. The additional peripherals impact the pin functional mapping because some pins are mapped to GPIOs and the new peripherals.

The ADSP-SC59x/2159x LPC package has the same number of GPIOs and external peripherals as the ADSP-2156x processor. It is pin compatible with ADSP-2156x BGA package (ADSP-21566, ADSP-21567, and ADSP-21569) except for newly added power pins for PLL power domain. With the exact footprint and pin compatibility, the ADSP-SC59x/2159x LPC package can replace the ADSP-2156x BGA in existing platforms.

Table 1 shows a comparison of the pins for the ADSP-SC59x/2159x LPC, HPC, and ADSP-2156x BGA packages.

For detailed information about the differences in the processor families, see the processor-specific data sheet[1] and hardware reference manual[2].

Pin Type	Number of Pins		
	ADSP-SC59x/2159x HPC	ADSP-SC59x/2159x LPC	ADSP-2156x BGA
VDD_INT	39	62	66
VDD_PLL	4	4	0
VDD_EXT	11	26	26
VDD_DMC	11	25	25
VDD_REF	3	19	19
VDD_ANA	1	1	1
DMC_VREF	2	2	2
Ground Pins	68	121	121
DAI Pins	40	40	40
GPIO pins	135	40	40

Table 1*: Pin Comparison*

In addition to pin compatibility, pin multiplexing is the same between ADSP-SC59x/2159x LPC and ADSP-2156x BGA packages. Any peripheral can be selected on the pin-mux between the two processors without concern for pin compatibility.

ADSP-SC59x/2159x Feature Enhancements

Dual SHARC+ DSPs running at up to 1 GHz provide double the MIPS, comparatively. Each core is accompanied by one FIR and four IIR accelerators (two FIRs and eight IIRs total), each running at up to 1 GHz. The accelerators can be used to offload many filtering operations from the SHARC+ cores. In addition to increased instances of accelerators, both IIR and FIR accelerators have been enhanced to provide improved performance.

In the IIR accelerator, the Wait for Trigger (TWAIT) functionality is now available in legacy mode and ACM mode. This functionality permits the use of the Channel Auto Iterate (CAI) feature with the possibility of synchronization between multiple IIR accelerators. The CAI feature with TWAIT can be used to skip coefficient loading between processing iterations with a pause.

In the FIR accelerator, the maximum burst transfer size has increased to 16. This feature increases DMA efficiency. Coefficient and data loading in parallel after TCB load is supported, and thereby minimizes load times. A prefetch buffer has been added to both the channels to reduce the access latency of the first data arrival in consecutive burst frames.

The ADSP-SC59x/2159x processor has the following peripheral enhancements. Some enhancements are available only in HPC package:

- CANFD provides high speed CAN network connectivity. The CANFD module has a flexible mailbox architecture that minimizes the processing requirement. It has bit rate switching support that allows data rates up to 8 Mbps for CAN transfers in the data phase. CANFD has a powerful filtering mechanism that supports message reception with an inbuilt FIFO. It supports low power modes along with pretended networking support with wakeup from selectively filtered messages. Available in HPC only.

- EMAC 10/100/1000 with AVB support. Available in HPC only.

- USB controller (with external PHY) support for high speed, full speed, and low speed with ITG modes. 8-bit ULPI PHY interface for connectivity with off-chip PHY. Available in HPC only.

- PDM controller support for direct interface to PDM microphones. The module converts digital PDM microphone data to I^2S/TDM format. The data can be routed internally to the SPORT/ASRC module or externally using the DAI pins. The controller supports four channels of PDM audio inputs from digital microphones with a 24-bit resolution output sampling rate of 4 kHz to 192 kHz.

- DAI Routing Unit (DRU) provides cross connectivity between two DAIs. This module overcomes the limitation of the ability to route only a few signals across DAIs. With the DRU module, all connections across DAIs (by interconnecting two DAI units through DRU) are possible.

- Global enabling of PCGs to synchronize the enabling of multiple PCGs

- Dedicated OSPI controller for flash accesses in single, dual, quad, and octal modes. In addition to standard operation in the ADSP-2156x processor, the OSPI module on the ADSP-SC59x/2159x processor supports a PHY mode of operation that includes DQS for accurate sampling of data at high clock rates. In PHY mode with DQS, the OSPI module can operate at up to 125 MHz in DTR mode, effectively providing a throughput of 250 Mbps. The ADSP-2156x processor supports 125 Mbps.

- Link port support for 2-bit SDR, 4-bit SDR/DDR, and legacy 8-bit SDR modes of operation

- Increased number of instances of SPI (4), UART (4), MDMA (8), PCG (8), Half-SPORTs (16) and GP timers (16). Available in HPC only.

- EPPI for connectivity to high speed CODECs and video encoders/decoders as well as LCD displays. Available in HPC only.

- Updated secure boot architecture speeds up the authentication process in the ADSP-SC59x/2159x processor. The architecture uses the pre-calculated SHA hash digest in the secure header to start authentication process early in the booting process without having to wait for the full image to be loaded. This enhancement save time for secure boot.

Power and Thermal Characteristics

When transitioning from the ADSP-2156x processor to the ADSP-SC59x/2159x processor, consider changes with respect to power and thermal design. Multiple cores and the large set of peripherals consume significantly higher power in the ADSP-SC59x/2159x processor. As a natural consequence of higher power, thermal design becomes equally important in system design.

Power

The power domains in the ADSP-SC59x/2159x processor are the same as the ADSP-2156x processor except for the addition of VDD_PLL. When designing the power supply for these processors, consider the maximum possible power consumption on each power rail and the power sequencing requirements during power-up and power-down operations.

> A power estimation application note will be provided to estimate the power consumption of ADSP-SC59x/2159x processor. Based on estimates, the power consumption on VDD_INT rail will be significantly higher. So, when transitioning from the ADSP-2156x processor to the ADSP-SC59x/2159x processor, upgrading the power supply(regulator) sourcing VDD_INT domain is the major change involved in the board design.

The power sequencing requirement for the SC59x/2159x processor is like the ADSP-2156x processor requirement. The power supply that provides the different power domains of the chip must ensure a certain relationship is maintained between the power domains while powering up and powering down the processor. At all times (including during power-up/power-down sequencing), the VDD_REF, VDD_ANA, and VDD_EXT supplies must stay within the VDELTA_EXT_REF specification given in the data sheet[1]. SYS_XTAL0 oscillations (SYS_CLKIN0) start when power is applied to the VDD_REF pins. All other power supplies can come up at any time before SYS_HWRST is deasserted. The rising edge of SYS_HWRST must occur after all voltage supplies and SYS_CLKIN0 oscillations are valid. Figure 1 shows the power up sequencing required between VDD_REF, VDD_ANA, and VDD_EXT power supplies.
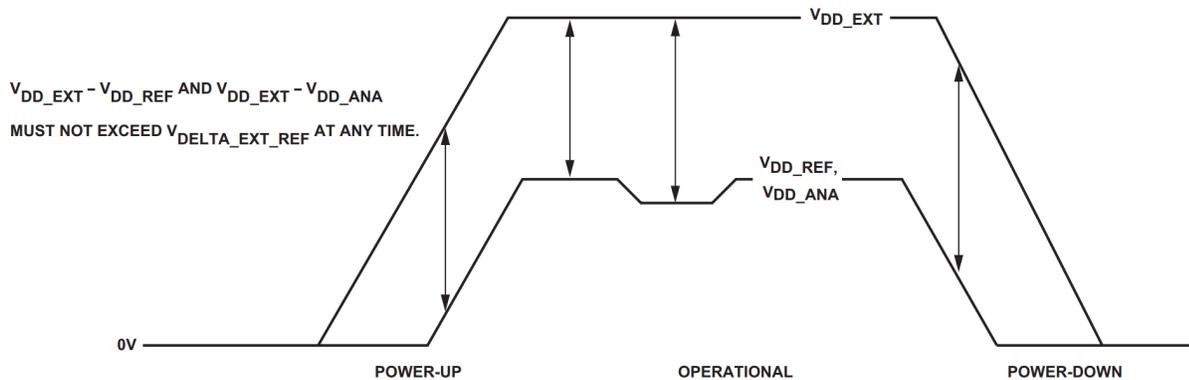

Figure 1: Power-up/Power-down Sequence

VDD_PLL Supply Recommendation

Refer to Table 1. For the ADSP-SC59x/2159x LPC package, the only change from the ADSP-2156x BGA is the four VDD_PLL balls (K06, L06, L07, M07) in place of VDD_INT balls. The voltage specification for VDD_PLL is the same as for VDD_INT in terms of voltage, which is 1V. However, acceptable ripple tolerance on VDD_PLL balls is less when compared to VDD_INT balls. Refer to the product data sheet for ripple tolerance requirements[1]. VDD_PLL should be connected to a low noise source voltage, separate from VDD_INT. Since the specification for VDD_PLL is the same as VDD_INT, to minimize cost, the supply can be derived from VDD_INT supply on the board using a low pass inductor base filter as shown in Figure 2:
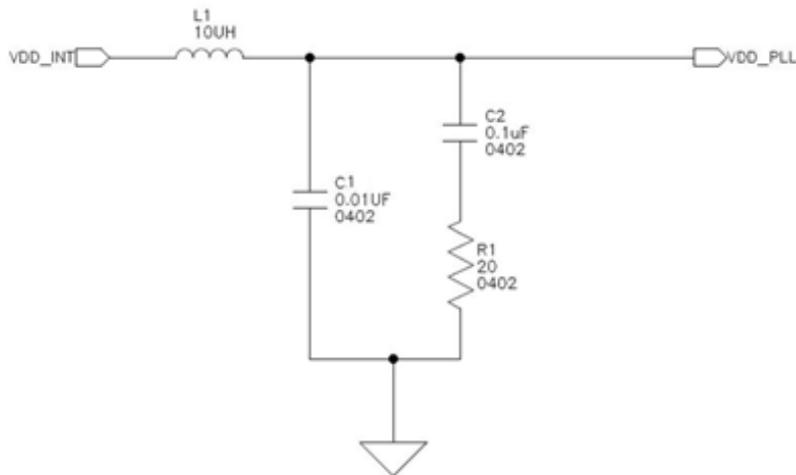
Figure 2: VDD_PLL Reference Circuit

Note the following filter circuit design recommendations:

1. Connect the filter at the entry point of the power plane for VDD_INT to VDD_PLL pins on the PCB.
2. L1 can be either an inductor or a ferrite bead.
3. Consider the self-resonant frequency of L1 to ensure that the inductor acts as a filter at the frequencies of interest.
4. R1 is used for critical damping. It should be adjusted to filter out noise peaks between 100 kHz and 1 MHz.
5. Choose a low-ESR capacitor (C1) to improve the noise response around 100 MHz.
6. Actual filter response will vary based on the components selected.

> Select any components that meet the ripple tolerance given in the processor data sheet[1].

Thermals

All ICs generate heat when power is applied. Therefore, to maintain the device's junction temperature below the maximum allowed, effective heat flow from the IC through the package to the ambient is essential. Dissipating heat from the IC through the package and to the ambient environment is crucial for optimal device and system performance.

Although the device densities and functionalities have increased, and, the associated device power consumption, the maximum allowable device junction temperatures have not changed. In the ADSP-SC59x/2159x processor, the overall power consumption is much higher than in the ADSP-2156x processor. However, the junction temperature (Tj) is the same (125 °C). Therefore, the thermal design of the system around the ADSP-SC59x/2159x processor must ensure that the junction temperature does not exceed 125 °C under any conditions.

While designing the thermal management around the ADSP-SC59x/2159x processor, consider the way Analog Devices provides the thermal characteristics for this processor. In the ADSP-2156x processor, the data sheet provides JESD51 package thermal characteristics in terms of Theta-JA (thermal resistance from junction to ambient, measured as °C/W.) and Psi-JT (thermal resistance from junction to case). The thermal characteristics can be used to estimate the processor die temperature based on ambient temperature, processor package temperature, and the amount of power dissipated inside the processor.

As processor power dissipation increases, JESD51 thermal characteristics are less effective in properly estimating the junction temperature. A better approach is to rely on thermal modes of the IC for correctly estimating the processor temperature. When thermal models are combined with empirical data, the user can have high confidence that the results accurately reflect real-world applications. The package elements are represented as resistors connected to the board in a resistor network. As in the ADSP-2156x processor, the ADSP-SC59x/2159x thermal models are provided in the form of compact thermal models. These models are provided in ECXML format. ECXML is a neutral file format intended to facilitate the provision of thermal models from suppliers to end users. These models are available and can be downloaded from the Analog Devices website.

The ADSP-SC59x/2159x models can be imported into tools like Ansys Icepak. The thermal models contain the ADSP-SC59x/2159x package 3D model and all of the thermal parameters for each element in the 3D model. The models and the rest of the system thermal information can be used to model the whole system (processor on the board along with heat sink and other components). Based on the use case, estimated power numbers (obtained from the power estimation application note) can be input into the thermal model followed by thermal simulation to understand the thermal behavior of the system. Note that the power setting in this model is nominally set at 1.0 W. This setting is a placeholder for the actual power; it needs to be changed before any simulation. It can be changed after importing the EXCML file into tool (for example, Icepak) by changing the power (for example, Die1 Source).

Clocking

Clocking in ADSP-SC59x/2159x processor is driven by two CGU unit as in the ADSP-2156x processor. However, the clocking scheme is more elaborate because there are many diverse peripherals (especially in HPC package) which have specific clocking needs. This complexity is due to an increased number of output clocks from the clock distribution unit (CDU) going to different target peripherals.

Figure 3 shows how the CDU combines the different clocks from two CGUs to source blocks such as GigE, CANFD, SPDIF, Link port, etc.

The ADSP-SC59x/2159x LPC package has one CLKIN input like the ADSP-2156x processor. The HPC package supports a second SYS_CLKIN source to provide two different input clocks to two CGU units. This design provides more flexibility in meeting the clocking requirements of different peripherals by having different CLKIN frequencies to derive the orthogonal set of clocks from each CGU.
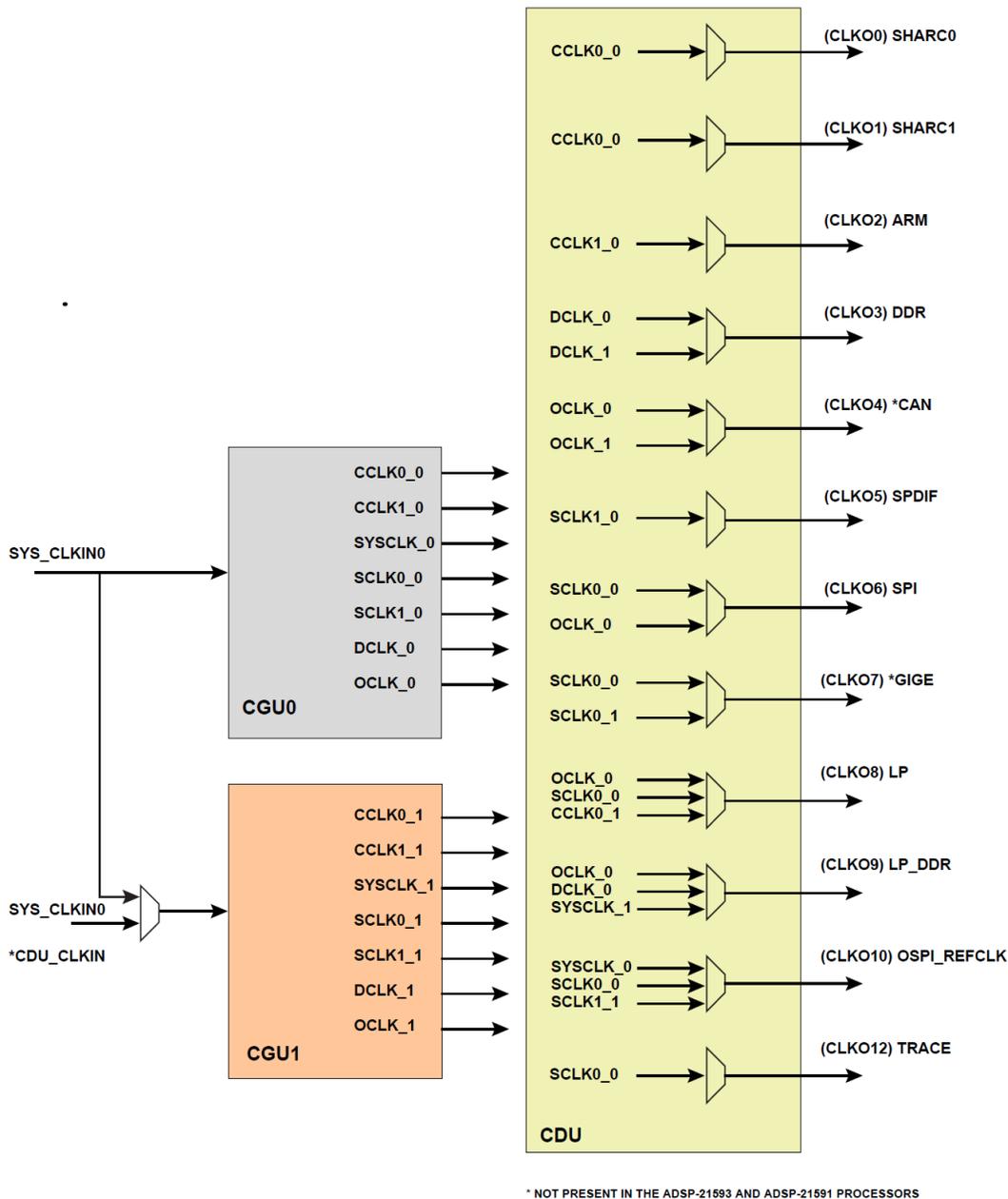
Figure 3: Clocking Scheme

Software Compatibility

Since the ADSP-SC59x/2159x processor shares many peripherals and infrastructure with the ADSP-2156x processor, the existing software written for the ADSP-2156x processor can be reused with minimal changes. System services and device driver (SSLDD) libraries provided with CCES® have been updated to support both the SHARC and Arm cores on ADSP-SC59x/2159x processor.

When porting software, consider the following changes that affect the operation of code in the ADSP-SC59x/2159x processor.

1. Changes in the system MMRs addresses of peripherals

Although most of the peripherals are the same between the ADSP-2156x and ADSP-SC59x/2159x processors, the system addresses of some of the peripheral registers may be different. If the software is using the ADI tools (CrossCore®) generated header files, these changes in MMR addresses are handled by the header files.

2. Interrupt and trigger IDs have changed.

Changes to interrupt and trigger IDs are handled in the ADI-provided header files. However, in the interrupt controller (SEC), the system event aggregator (SEA) is new. The SEA multiplexes the peripheral interrupts onto a single SEC ID channel, thereby allowing the SEC to handle a number of interrupts beyond ID255. The ADSP-SC59x/2159x processor has 325 peripheral interrupts in total (which is beyond what SEC can natively support (255)). Therefore, to accommodate multiple interrupts from a peripheral that are assigned a single SEC ID, the interrupts are differentiated with a unique SEA ID. This new functionality requires a change in how interrupts are handled by the application.

3. Pin multiplexing

When transitioning from the ADSP-2156x BGA to the ADSP-SC59x/2159x LPC, there is no change required in pin multiplexing; the two processors have the same pins as well as pin mux. The ADSP-SC59x/2159x HPC has more ports (up to PORT I) than the three ports in the ADSP-2156x BGA. Pin multiplexing until PORT C is the same as in the ADSP-2156x BGA. But, some peripherals which occur on PORTA, PORTB or PORTC may also occur on higher ports to allow a more diverse use of peripherals. In this case, there may be a need to update the pin mux in software accordingly.

4. Workaround for anomalies

The ADSP-SC59x/2159x processor has corrected some anomalies that existed in the ADSP-2156x processor. These anomalies may affect the workaround implemented in software. Therefore, refer to latest product anomaly sheet[3] to take care of changes that may apply.

References

[1]   *ADSP-21591/21593/21594/ADSP-SC591/SC592/SC594 Data Sheet* Rev PrD, May 2021. Analog Devices, Inc.

[2]   *ADSP-2159x/ADSP-SC591/592/594 SHARC+ Processor Hardware Reference.* Rev 0.2, May 2021. Analog Devices, Inc.

[3]   *ADSP-21591/21593/21594/ADSP-SC591/SC592/SC594 Silicon Anomaly List.* Rev B, May 2021. Analog Devices, Inc.

Document History

Revision	Description
Rev 1 – June 2021 *by Nabeel Shah*	Initial Release