

ADSP-2185L Anomaly List for Revisions 0.0-1.1

The list below represents the known anomalies and workarounds for the ADSP-2185L. The silicon revision of a particular device can be found on the chip, as shown below:

ADSP-2185L	Part Number
-xxx	Speed Grade/Package
xyzzzzzz-1.1	Lot number and silicon revision
Dwwyy	Date code

The table below shows which ADSP-2185Ls have each anomaly. The left hand side of the table lists the type of anomaly and the numbers on the top of the table refer to the particular revision of the silicon. Any box that has an 'x' contained in it has that anomaly. For a complete description of the anomaly, please refer to the subsequent pages.

	0.0	1.0	1.1
1. Type 3 instruction decode error		x	
2. SPORT1 Memory Mapped Register and Corrupted Memory		x	
3. +10%/-5% Power Supply Tolerances		x	x
4. BDMA Write Glitch	x		
5. Pull-down Resistor on <u>IACK</u>		x	

Anomaly #1

When executing a type 3 instruction under the following conditions, the DMOVLAY and PMOVLAY registers can be corrupted.

Conditions:

1. Type 3 instruction; Read/Write Data Memory (Immediate Address).
2. Memory read.
3. To a Group 3 register (RGP = b#11).
4. Immediate address[13:0] = b#01:XXXX:01XX:111X.
 - > If bit 0 is a 0, then PMOVLAY is corrupted.
 - > If bit 0 is a 1, then DMOVLAY is corrupted.

Notes:

- The Group 3 registers are the following:

ASTAT
MSTAT
SSTAT
IMASK
ICNTL
CNTR
SB
PX
RXn
TXn
IFC
OWRCNTR

The anomaly lies within the instruction decode circuitry. Therefore the physical location of the instruction in PM memory is irrelevant. When the PMOVLAY or DMOVLAY registers are corrupted, they are overwritten with the same value which is being written to the Group 3 register.

Example:

ASTAT = DM(0x107F) ;

This instruction will corrupt the DMOVLAY register. It will corrupt the DMOVLAY register by writing the register with the contents of DM location 0x107F.

Workaround:

Ensure that no instructions have the opcode assignment as described above. This can be accomplished through breaking up Type 3 instructions into two separate instructions.

Anomaly #2

When writing to the SPORT1 Control Register (located at memory-mapped location 0x3FF2), the most significant bit must be equal to zero (read only flag out bit). If the most significant bit is written a value of 1, the contents of internal PM/DM will be corrupted.

Anomaly #3

The required supply voltage (V_{dd}) tolerance is $3.3v +10\%/-5\%$ on the ADSP-2185L -210 (52 MHz) speed grade. Therefore, $V_{dd}(\min) = 3.135v$ and $V_{dd}(\max) = 3.63v$. On speed grades of -160 (40 MHz) and less, the required supply voltage tolerance is $+10\%/-10\%$.

Anomaly #4

During a wait-stated Byte DMA write cycle, the DSP will drive data lines D15-D8 (all other data lines are not affected) low for approximately 2ns every processor cycle regardless of the number of BDMA software wait states. This will create a glitch on data lines D15-D8 just prior to the correct data being latched on the bus. The size of the glitch depends on the loading of the data bus. This anomaly effectively changes the formula for the "Data setup before WR~ High" (t_{DW}) timing specification. The formula changes from:

$$\begin{aligned} & .5t_{ck}-7+w \text{ ns} \quad \text{to} \\ & .5t_{ck}-7 \text{ ns} \end{aligned}$$

This anomaly only affects data lines D15-D8 when performing wait stated BDMA writes. The address bus and write strobe work properly with any wait state value.

Workaround:

A latch could be used to capture the information on the BDMA data lines during the period that the information being written is stable. Also, because of the brevity of the glitch, the capacitance on the data bus may be enough to hold the data values to a sufficient level.

Anomaly #5

If, when coming out of reset, the PF3 pin is not held low, the IACK signal may tri-state instead of dropping below V_{OL} when IDMA is inactive or is performing an address or data latch.

Workaround:

Use a pulldown resistor on PF3 as described in "Modes of Operation" in the datasheet.
