ADSP-2186L Anomaly List for Revisions 0.0-2.0

The list below represents the known anomalies and workarounds for the ADSP-2186L. The silicon revision of a particular device can be found on the chip, as shown below:

ADSP-2186L	Part Number
-xxx	Speed Grade/Package
xyzzzzzzz-**2.0**	Lot number and **silicon revision**
Dwwyy	Date code

The table below shows which ADSP-2186Ls have each anomaly. The left hand side of the table lists the type of anomaly and the numbers on the top of the table refer to the particular revision of the silicon. Any box that has an 'x' contained in it has that anomaly. For a complete description of the anomaly, please refer to the subsequent pages.

	0.0	1.1	2.0
1. BDMA Write Glitch	x		

Anomaly #1

During a wait-stated Byte DMA write cycle, the DSP will drive data lines D15-D8 (all other data lines are not affected) low for approximately 2ns every processor cycle regardless of the number of BDMA software wait states. This will create a glitch on data lines D15-D8 just prior to the correct data being latched on the bus. The size of the glitch depends on the loading of the data bus. This anomaly effectively changes the formula for the "Data setup before WR~ High" (t_{DW}) timing specification. The formula changes from:

.5tck-7+w ns to
.5tck-7 ns

This anomaly only affects data lines D15-D8 when performing wait stated BDMA writes. The address bus and write strobe work properly with any wait state value.

Workaround:
A latch could be used to capture the information on the BDMA data lines during the period that the information being written is stable. Also, because of the brevity of the glitch, the capacitance on the data bus may be enough to hold the data values to a sufficient level.