Notes on using Analog Devices' DSP, audio, & video components from the Computer Products Division
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ADSP-2181 IDMA Port - Cycle Steal Timing

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This EE-Note will give an explanation of how long an idma access will take under varying conditions.

The variables **IDEL** and **ODEL** refer to the delay associated with driving a value on/off chip. Refer to the appropriate 218x data sheet for actual delay values.

The variable **W** refers to the wait state value for a given external access.

When referring to sport autobuffering internal/external refer to which memory space the data memory access goes to, not to any sport configuration.

1.Starting with /IACK low.

2.After /IS and /WR (or /IRD) are asserted it should take IDEL for the 218x to receive this and ODEL to respond by driving /IACK high.

3.It will then take between .5 and 1.5 TCLK cycles to synchronize and request a cycle steal. The IDMA Port is the highest priority cycle steal so it will receive the next available cycle.

4.The worst case time to complete the current cycle varies as follows:

ACCESS	TCLKS
An internal instruction with/without an internal access	.5
An internal instruction with one external access	.5+W
An internal instruction with two external access	.5+W1+(1+W2)
An external instruction with/without an internal access	.5+W
An external instruction with one external access	.5+W1+(1+W2)
An external instruction with two external access	.5+W1+(1+W2)+(1+W3)
An internal BDMA access	.5
An external BDMA access	.5+W
An internal autobuffer access	.5
An external autobuffer access	.5+W
Bus granted and not hung (See Users Manual--Bus Request)	.5
Bus granted and hung (See Users Manual--Bus Request)	.5+ Time until bus grant deasserted
In idle	.5
In slowidle(n)	.5+n

5.Now it executes the idma access using the stolen cycle of time TCLK.

6.It then takes an additional .5 TCLK + ODEL to drive NIACK high.

Given no external accesses the overall times would be:

Best case time is IDEL + 2.5TCLK + ODEL
Worst case time is IDEL + 3.5TCLK + ODEL

Given one external accesses

Best case time is IDEL + 2.5TCLK + ODEL
Worst case time is IDEL + (3.5+W)TCLK + ODEL

Given two external accesses

Best case time is IDEL + 2.5TCLK + ODEL
Worst case time is IDEL + (4.5+W1+W2)TCLK + ODEL

Given three external accesses

Best case time is IDEL + 2.5TCLK + ODEL
Worst case time is IDEL + (5.5+W1+W2+W3)TCLK + ODEL

Using Bus Request

Best case time is IDEL + 2.5TCLK + ODEL
Worst case time is IDEL + (INFINITE)TCLK + ODEL

Using Slowidle(n)

Best case time is IDEL + 2.5TCLK + ODEL
Worst case time is IDEL + (2.5+n)TCLK + ODEL

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