ANALOG DEVICES

Computer Products Division **12/23/98**

ADSP-2187L Anomaly List for Revisions 0.0-1.1

The list below represents the known anomalies and workarounds for the ADSP-2187L. The silicon revision of a particular device can be found on the chip, as shown below:

ADSP-2187L	Part Number
-xxx	Speed Grade/Package
xyzzzzzzz-**1.1**	Lot number and **silicon revision**
Dwwyy	Date code

The table below shows which ADSP-2187Ls have each anomaly. The left hand side of the table lists the type of anomaly and the numbers on the top of the table refer to the particular revision of the silicon. Any box that has an ‘x’ contained in it has that anomaly. For a complete description of the anomaly, please refer to the subsequent pages.

	0.0	0.1	0.2	1.0	1.1
1. Type 3 instruction decode error				x	
2. BDMA Write Glitch	x	x	x		
3. IACK orientation change				x	x
4. +10%/-5% Power Supply Tolerances	x	x	x	x	
5. IDMA Boot and PMOVLAY anomaly	x	x			
6. Non-operational BDMA Boot	x	x			
7. Loop Counter Glitch	x	x			

Anomaly #1

When executing a type 3 instruction under the following conditions, the DMOVLAY and PMOVLAY registers can be corrupted.

Conditions:

1. Type 3 instruction; Read/Write Data Memory (Immediate Address).
2. Memory read.
3. To a Group 3 register (RGP = b#11).
4. Immediate address[13:0] = b#01:XXXX:01XX:111X.
    > If bit 0 is a 0, then PMOVLAY is corrupted.
    > If bit 0 is a 1, then DMOVLAY is corrupted.

Notes:

- The Group 3 registers are the following:
    ASTAT
    MSTAT
    SSTAT
    IMASK
    ICNTL
    CNTR
    SB
    PX
    RXn
    TXn
    IFC
    OWRCNTR

The anomaly lies within the instruction decode circuitry. Therefore the physical location of the instruction in PM memory is irrelevant. When the PMOVLAY or DMOVLAY registers are corrupted, they are overwritten with the same value which is being written to the Group 3 register.

Example:

```
ASTAT = DM(0x107F) ;
```

This instruction will corrupt the DMOVLAY register. It will corrupt the DMOVLAY register by writing the register with the contents of DM location 0x107F.

Workaround:
Ensure that no instructions have the opcode assignment as described above. This can be accomplished through breaking up Type 3 instructions into two separate instructions.

Anomaly #2

During a wait-stated Byte DMA write cycle, the DSP will drive data lines D15-D8 (all other data lines are not affected) low for approximately 2ns every processor cycle regardless of the number of BDMA software wait states. This will create a glitch on data lines D15-D8 just prior to the correct data being latched on the bus. The size of the glitch depends on the loading of the data bus. This anomaly effectively changes the formula for the "Data setup before WR~ High" (t_{DW}) timing specification. The formula changes from:

.5tck-7+w ns to
.5tck-7 ns

This anomaly only affects data lines D15-D8 when performing wait stated BDMA writes. The address bus and write strobe work properly with any wait state value.

Workaround:
A latch could be used to capture the information on the BDMA data lines during the period that the information being written is stable. Also, because of the brevity of the glitch, the capacitance on the data bus may be enough to hold the data values to a sufficient level.

Anomaly #3

The sense of IACK will remain the same. IACK is active low.

IACK = 0 = OK
IACK = 1 = Busy

The design change modifies the IACK pin from an open drain requiring a pull up resistor to an open source requiring a pull down resistor. This means:

IACK = 0 = OK = Hi Impedance (Floating)
IACK = 1 = Busy = Active Hi

The IACK lines of all the processors can be wire OR'ed and a pull down resistor should be used. A resistor in the range of 10KΩ to 47KΩ is recommended.

```
IACK1 ------|
            |
IACK2 ------|
            |-----------------------
IACK3 ------|                   |
            |                  \
IACK4 ------|                   /  10-47KΩ
                               \
                               |
                                = (GND)
```

With this scheme, all IACK lines will be floating in the acknowledge state. The pull down resistor will pull the floating lines low. When any of the processors become busy, its IACK line will go active high, pulling all the IACK lines hi. Depending upon the resistor value being used 100-500µA will flow through the resistor.

Anomaly #4

The required supply voltage (V_{dd}) tolerance is 3.3v +10%/-5%. Therefore, V_{dd} (min) = 3.135v and V_{dd} (max) = 3.63v.

Anomaly #5

During the IDMA boot process, the processor will begin execution from PM address 0 when location 0x2000 on PM Overlay 4 is written to, as well as when PM location 0x0000 is written to. The processor should only begin execution when PM location 0x0000 is written. The effect of this anomaly is that if location 0x2000 on PM Overlay 4 is written before PM location 0x0000, then the processor will begin execution from un-initialized memory.

Workaround:
1. Ensure that no code or data segments inhabit location 0x2000 on PM overlay 4. An architecture file can be written such that this memory location is not used.
2. Initialize location 0x2000 on PM Overlay 4 after the boot sequence has been completed and the processor has started to execute other code.

Anomaly #6

BDMA boot capability is not functional on the device.

Anomaly #7

Under certain voltage conditions, certain bit patterns are corrupted when written to the counter. The anomaly is seen when the values have several adjacent “1 - 0” sequences. Further characterization is on-going.
