8 MEMORY INTERFACE

Overview

The ADSP-218x family of processors has a modified Harvard architecture in which data memory stores data and program memory stores both instructions and data. A program instruction or opcode can be fetched from internal memory and executed. In the same clock cycle, two data elements can be accessed from internal memory: one from Data Memory and the other from Program Memory.

Program Memory and Data Memory

Each ADSP-218x family processor contains on-chip RAM, which allows a portion of the Program Memory space and a portion of the Data memory space to reside on-chip. External Program Memory and external Data Memory can also be used in a system design. 16 K words total of external Program Memory (24-bits) and 16 K words total of external Data Memory (16-bits) can be addressed as 8 K overlay memory segments.

Byte Memory Space

Each processor has a 4 M addressable byte-wide memory space (Byte Memory space). This space can be used for the following:

- Loading on-chip program memory with code from an external EPROM at reset
- Bulk code or data storage during runtime
- Software overlays when a program's code size exceeds the amount of on-chip memory on the processor

I/O Memory Space

The ADSP-218x processors support I/O Memory space. This space is a 16-bit, 2048 location that allows for the memory mapping of external peripherals or other processors to the ADSP-218x processor. External memory select signals are associated with each of these external memory spaces.

Memory Buses

In each ADSP-218x family processor, memory is connected to the internal functional units by four on-chip buses: the Data Memory Address (DMA) bus, Data Memory Data (DMD) bus, Program Memory Address (PMA) bus and Program Memory Data (PMD) bus. The internal PMA bus and DMA bus are multiplexed into a single address bus that is extended off-chip. Likewise, the internal PMD bus and DMD bus are multiplexed into a single external data bus. The sixteen MSBs of the external data bus are used as the DMD bus: external bus lines D_{23-8} are used for DMD_{15-0}.

External Memory Spaces

There are four separate external memory spaces: Data Memory, Program Memory, Byte Memory, and I/O Memory. To provide external access to these memory spaces, the ADSP-218x processors extend the 14-bit internal address bus and 24-bit data bus off-chip and provide the $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, and $\overline{\text{IOMS}}$ select lines. The $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, and $\overline{\text{IOMS}}$ signals indicate which memory space is being accessed.

Because the Program Memory and Data Memory buses are multiplexed off-chip, if more than one external transfer must be made in the same instruction, an overhead cycle will be required. An overhead cycle is not required if just one off-chip access (with no wait states) occurs in any instruction.

All external memories may have automatic wait state generation associated with them. The number of wait states—each equal to one instruction cycle—is programmable.

Composite Memory Select

The Composite Memory Select (and its $\overline{\text{CMS}}$ select line) lets a single off-chip memory be accessed as multiple memory spaces. The Composite Memory Select register lets you define which memory spaces are selected by the $\overline{\text{CMS}}$ signal. By using this register, you can assign the $\overline{\text{CMS}}$ signal to become active on any combination of Program Memory, Data Memory, Byte Memory, or I/O Memory external memory accesses.

External Overlay Memory

External Program Memory and external Data Memory can be addressed as 8 K overlay memory segments (pages). These overlay segments are mapped to addresses 0x2000-0x3fff for Program Memory overlay regions and 0x0000-0x1fff for Data Memory overlay regions.

Internal Direct Memory Access Port

The Internal Direct Memory Access (IDMA) port is a 16-bit slave port that supports booting from an external host processor. This port also allows the host runtime access to all of the internal memory contents (both internal Program Memory and Data Memory) of the DSP—except for the memory-mapped control registers, which reside at the uppermost 32 locations of internal Data Memory. The DMA feature of this port lets you define the number of memory locations the DSP transfers to or from internal memory in the background while continuing foreground processing.

Memory Modes

The IDMA port is a separate port on the ADSP-2181 and ADSP-2183 processors and a configured port on all other ADSP-218x processors. For all of the ADSP-218x family processors, except for the ADSP-2181 and ADSP-2183, the external address and data pins are multiplexed with the IDMA address/data bus and control signals. The functionality of these multiplexed pins is determined at reset by external Mode pins. The value of these Mode pins determine whether the 100-pin ADSP-218x processors have access to the full 14-bit address bus and 24-bit data bus (Full Memory Mode) or if the processor has IDMA functionality (Host Memory Mode) with a single address bit (`A0`) and a 16-bit data bus (`D[23:8]`).

The pin multiplexing design enables processors to use a smaller number of pins, which results in a smaller package size. This reduced size helps save board “real estate” in board size-critical applications. On the other hand, this reduced size requires a more complex design in order to use both the external address and data busses simultaneously with IDMA port functionality.

Memory Interfaces

In the modified Harvard architecture used by ADSP-218x processors, Program Memory stores both instructions and 24-bit or 16-bit data values; Data Memory stores 16-bit data values only. The amount of on-chip memory differs for each processor. Table 8-1 identifies the amount of on-chip memory contained in each processor.

Table 8-1. ADSP-218x Processor Base On-Chip Memory

Processor	Program Memory	Data Memory
ADSP-2181	16 K by 24-bit words	16 K by 16-bit words
ADSP-2183	16 K by 24-bit words	16 K by 16-bit words
ADSP-2184, ADSP-2184L and ADSP-2184N	4 K by 24-bit words	4 K by 16-bit words
ADSP-2185, ADSP-2185L, ADSP-2185M, and ADSP-2185N	16 K by 24-bit words	16 K by 16-bit words
ADSP-2186, ADSP-2186L, ADSP-2186M, and ADSP-2186N	8 K by 24-bit words	8 K by 16-bit words
ADSP-2187L and ADSP-2187N	32 K by 24-bit words	32 K by 16-bit words
ADSP-2188M and ADSP-2188N	48 K by 24-bit words	56 K by 16-bit words
ADSP-2189M and ADSP-2189N	32 K by 24-bit words	48 K by 16-bit words

Figures 8-1 through 8-6 show the on-chip Program Memory and Data Memory configurations and their address mappings for each of the ADSP-218x family processors.

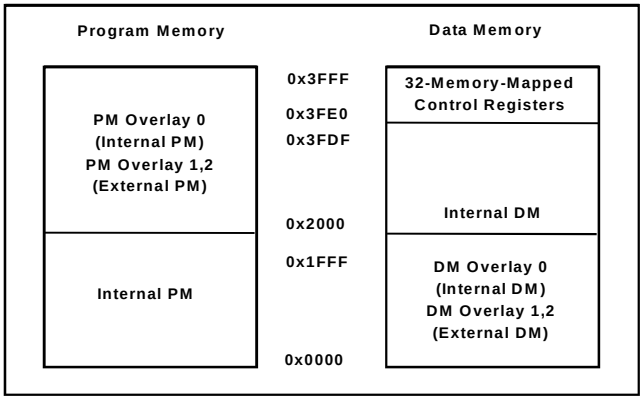

Figure 8-1. ADSP-2181, ADSP-2183, and ADSP-2185 Memory Architecture (MMAP=0 for ADSP-2181 and ADSP-2183, and Mode B=0 for ADSP-2185)

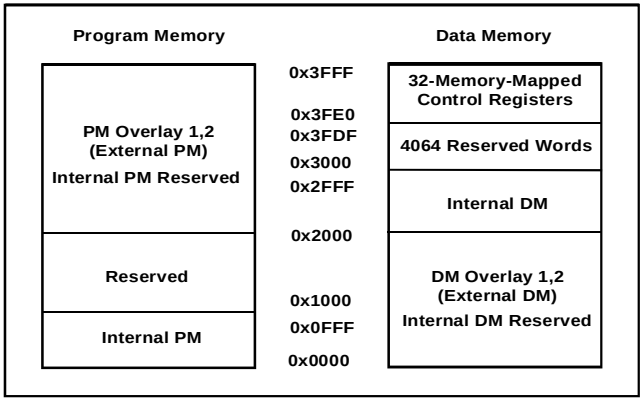

Figure 8-2. ADSP-2184 Memory Architecture (Mode B=0)

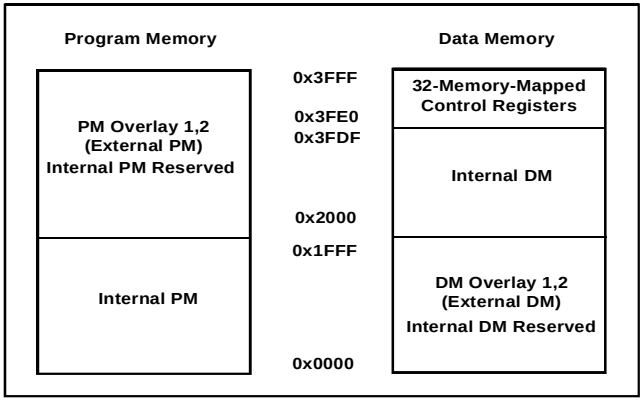

Figure 8-3. ADSP-2186 Memory Architecture (Mode B=0)

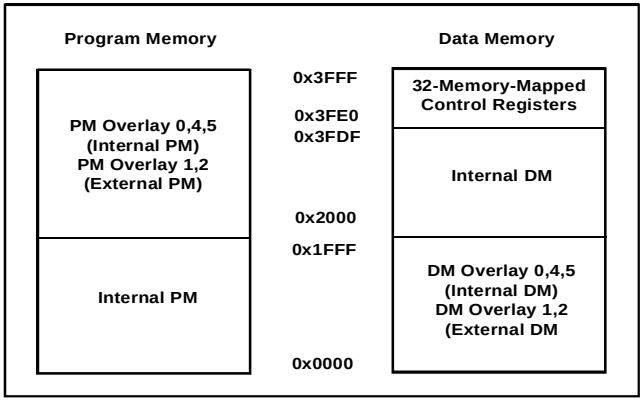

Figure 8-4. ADSP-2187 Memory Architecture (Mode B=0)

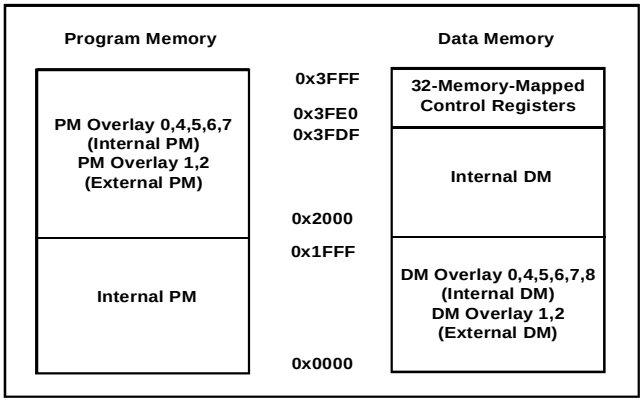

Figure 8-5. ADSP-2188 Memory Architecture (Mode B=0)

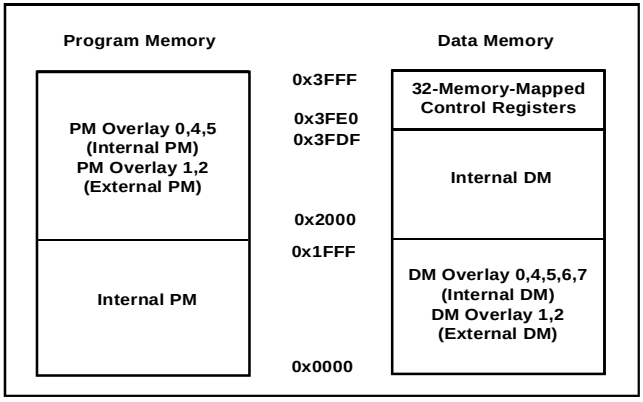

Figure 8-6. ADSP-2189 Memory Architecture (Mode B=0)

These memory maps show how the internal memory is configured for each of the ADSP-218x family processors. Since the ADSP-2184 and ADSP-2186 processors have less than 16 K words of Program Memory and Data Memory, some of their internal memory locations are reserved and should not be used in the Linker Description File (LDF) or accessed at runtime in the executable program. Please note that all external memory locations map to Program Memory and Data Memory overlay pages 1 and 2.

Program Memory Interface

The ADSP-218x family Program Memory is 24-bits wide. Up to two accesses to internal Program Memory can be completed per instruction cycle. Instruction read accesses are done on the first half of the clock cycle, and data reads and writes are done on the second half of the clock cycle.

The Program Memory Address bus is 14 bits in length. This length allows the ADSP-218x processors to directly access 16 K of internal Program Memory. For processors with more than 16 K internal Program Memory, the additional memory regions are accessed or selected as 8 K Program Memory overlay segments, using a Program Memory Overlay register (`PMOVLAY`). This register acts as a program memory page select.

All of the ADSP-218x family processors can also access up to 16 K of external Program Memory. External Program Memory is also selected by using the Program Memory Overlay register. Only one overlay region can be active at a time; this restriction applies to both internal and external overlay regions.

The PWAIT field of the System Control register sets the number of wait states for each access to external Program Memory overlays. The value of the PWAIT bit field of the System Control register defaults to fifteen after reset for all ADSP-218x M and N series processors. Bit 15 of the System Control register for these ADSP-218x M and N series processors defaults to 1, which assigns twice the value of the PWAIT bit field plus one (2N+1) wait states. The PWAIT bit field defaults to seven after reset for all other ADSP-218x processors.

For all ADSP-218x processors, Program Memory Overlay regions 1 and 2 correspond to external Program Memory overlay regions, each 8 K in length. All other overlay regions are internal overlays, except for Overlay region 3, which is reserved. External Program Memory overlays are selected by using the Program Memory Overlay register (PMOVLAY). Only one Program Memory overlay region can be active at a time; this restriction applies to both internal and external Program Memory overlay regions.

Internal Program Memory overlay regions do not apply to the ADSP-2184 and ADSP-2186 processors.

When accessing external Program Memory overlay pages, the PMOVLAY register controls or determines the value of the address pin A13. When the PMOVLAY register equals 1, the value of A13 is zero. When the PMOVLAY register equals two, the value of address pin A13 is 1. Table 8-2 explains the operational behavior of the PMOVLAY register and address pin A13 when using external Program Memory overlay pages.

Table 8-2. PMOVLAY and Program Memory Overlay Addressing

PMOVLAY	Memory	A13	A12:0
0,4,5,6,7	Internal 8 K Region	N/A	N/A
1	External 8 K Overlay 1	0	13 LSBs of address between 0x2000 and 0x3FFF
2	External 8 K Overlay 2	1	13 LSBs of address between 0x2000 and 0x3FFF

The on-chip Program Memory and internal and external Program Memory overlay regions can hold both instructions and data intermixed in any combination. By assigning the memory architecture description in the Linker Description File, a programmer can specify absolute address placement for any code or data module, including code for the interrupt vector table and reset vector. The reset vector is located at Program Memory address 0x0000. In conjunction with the Linker Description File, the ADSP-218x processor linker determines where to place relocatable code and data segments.

All of the Program Memory overlay regions map from address location `PM(0x2000)` to `PM(0x3FFF)`. The value of the Program Memory Overlay register (`PMOVLAY`), determines which overlay region is currently being accessed and whether an internal or an external `PM` overlay region is being accessed by the DSP core.

ADSP-218x processors' program sequencer operates independently from the PMOVLAY register. The program sequencer only operates on the absolute address of the current instruction it is executing. For Program Memory, the overlay regions map to the address range 0x2000 – 0x3fff. Special care must be taken by the programmer to ensure that the proper target address and overlay are accessed when making jumps or calls in the program.

Also, the DAG registers operate independently of the PMOVLAY register. Again, special care must be taken to ensure the proper target Program Memory region is being accessed when performing register indirect jump or call instructions or when performing serial port autobuffering to Program Memory overlay regions.

Data Memory Interface

The Data Memory of the ADSP-218x family processors is 16-bits wide. Similar to the internal Program Memory of these processors, up to two accesses to internal Data Memory can be completed per instruction cycle. Memory read accesses are done on the first half of the clock cycle and memory writes are done on the second half of the clock cycle.

The Data Memory Address bus is 14 bits in length; the ADSP-218x processor can directly access 16 K of internal Data Memory. For processors with more than 16 K of internal Data Memory, the additional memory regions are accessed or selected as 8 K Data Memory overlay segments using a Data Memory Overlay (DMOVLAY) register. This register acts as a Data Memory page select.

For all ADSP-218x processors, Data Memory Overlay regions 1 and 2 correspond to external Data Memory overlay regions, each 8 K in length. All other overlay regions are internal overlays, except for Overlay 3, which is reserved. External Data Memory overlays are selected by using the Data Memory Overlay register (DMOVLAY). Only one Data Memory overlay region can be active at a time; this restriction applies to both internal and external Data Memory overlay regions.

Internal Data Memory overlay regions do not apply to the ADSP-2184 and ADSP-2186 processors.

The DWAIT field of the Wait State Control register sets the number of wait states for each access to external Data Memory overlays. The value of the DWAIT bit field of the System Control register defaults to seven after reset for all ADSP-218x M and N series processors, but the total number of wait states is fifteen for these processors. Bit 15 of the Wait State Control register for these ADSP-218x M and N series processors defaults to 1, which assigns twice the value of the DWAIT bit field plus one (2N+1) wait states. The DWAIT bit field defaults to seven after reset for all other ADSP-218x processors.

The on-chip Data Memory and internal and external Data Memory overlay regions can be used to store data. By assigning the memory architecture description in your Linker Description File, you can specify absolute address placement for any data segment. In conjunction with your Linker Description File, the ADSP-218x linker determines where to place relocatable data segments.

When accessing external Data Memory overlay pages, the DMOVLAY register controls or determines the value of the address pin A13. When the DMOVLAY register equals 1, the value of A13 is 0. When the DMOVLAY register equals 2, the value of address pin A13 is 1. Table 8-3 explains the operational behavior of the DMOVLAY register and address pin A13 when using external Data Memory overlay pages.

Table 8-3. DMOVLAY and Data Memory Overlay Addressing

DMOVLAY	Memory	A13	A12:0
0,4,5,6,7,8	Internal 8 K Region	NA	NA
1	External 8 K Overlay 1	0	13 LSBs of address between 0x0000 and 0x1FFF
2	External 8 K Overlay 2	1	13 LSBs of address between 0x0000 and 0x1FFF

All of the Data Memory overlay regions map from address location DM(0x0000) to DM(0x1FFF). The value of the Data Memory Overlay register (DMOVLAY) determines which overlay region is currently being accessed and whether an internal or an external DM overlay region is being accessed by the DSP core.

Since the DMOVLAY register works independently from the program sequencer and DAGs, special care must be taken by the programmer to ensure that the proper target memory location is accessed. For example, the programmer should take care when switching between Data Memory Overlay regions while serial port autobuffering is active. On a positive note, this switching could allow the programmer to configure the serial port autobuffering mechanism to operate in “ping-pong” fashion when switching between overlay memory regions.

Listing 8-1 provides example instructions that demonstrate how to use the DMOVLAY register.

Listing 8-1. DMOVLAY Register Example

```
DMOVLAY=DM(0x1234); /* type 3 instruction, DMOVLAY is loaded
                       with the contents of address
                       DM(0x1234) */
DMOVLAY=2;          /* type 7 instruction, DMOVLAY is loaded
                       with the value 2 */
DMOVLAY=AX0;        /* DMOVLAY is loaded from AX0 register */
AX0=DMOVLAY;        /* AX0 is loaded from DMOVLAY register */
```

Byte Memory Interface

The ADSP-218x processor's Byte Memory space is 8 bits wide and can address up to 4M bytes of program code or data. The ADSP-218x processor can boot through this interface, as well as performing read and write accesses to an 8-bit memory device via the BDMA port during runtime. The external signal $\overline{\text{BMS}}$ is active during Byte Memory accesses.

Each read or write to Byte Memory consists of data (which is driven on data bus lines D[15:8]) and address information (driven on address lines A[13:0], concatenated with data lines D[23:16]). This gives the BDMA port a total of 22 bits of addressing, which allows you to access up to 4M byte of ROM or RAM. This memory can be read from or written to in four different formats: 24-bit code, 16-bit data, 8-bit data MSB aligned, or 8-bit data LSB aligned. For 8-bit MSB aligned accesses, the LSBs are zero padded during byte memory reads. For 8-bit LSB aligned accesses, the MSBs are zero padded during byte memory reads.

Wait states for Byte Memory accesses are programmable via the BMWAIT bit field of the Programmable Flag and Composite Memory Select Control register. For the ADSP-218x M and N series processors, the default setting for BMWAIT is fifteen after reset. For all other ADSP-218x processors, the default setting is seven after reset.

For more information on the ADSP-218x processor's Byte Memory and BDMA port, please refer to the "BDMA Port" section in Chapter 9, "DMA Ports".

I/O Memory Space

The ADSP-218x family processors have a dedicated 16-bit wide I/O Memory space consisting of 2048 locations. This dedicated memory space allows you to memory map peripherals using this space rather than using external Program Memory and/or external Data Memory addressing and resources to interface with external devices.

There are four programmable wait state regions that are associated with I/O Memory space. The Wait State Control register contains the `IOWAIT0:3` bit fields that control the four I/O Memory wait state regions, consisting of 512 locations each.

For the ADSP-218x M and N series processors, the default setting for `IOWAIT` is 15 after reset. For all other ADSP-218x processors, the default setting is 7 after reset. Figure 8-7 shows the Wait State Control register and the `IOWAIT0:3` fields that control I/O Memory wait state regions for the ADSP-218x M and N series processors. Figure 8-8 shows the same information for all other ADSP-218x processors

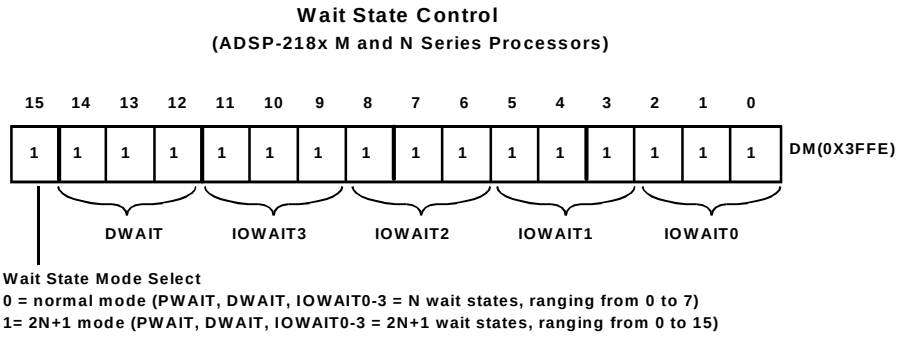

Figure 8-7. Wait State Control Register (ADSP-218x M and N Series)

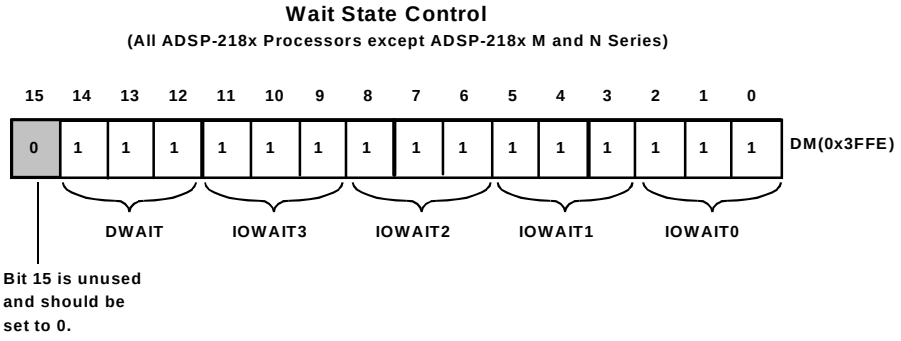

Figure 8-8. Wait State Control Register (All ADSP-218x Processors except M and N Series)

The Wait State Control register is divided into the following fields:

- IOWAIT0—This 3-bit field sets the number of wait states (0-7) for accesses to I/O Memory addresses 0x000-0x1ff.
- IOWAIT1—This 3-bit field sets the number of wait states (0-7) for accesses to I/O Memory addresses 0x200-0x3ff.
- IOWAIT2—This 3-bit field sets the number of wait states (0-7) for accesses to I/O Memory addresses 0x300-0x4ff.
- IOWAIT3—This 3-bit field sets the number of wait states (0-7) for accesses to I/O Memory addresses 0x400-0x5ff.

For the ADSP-218x M and N series processors, bit 15 of the Wait State Control register operates as a Wait State Mode Select bit. When set, this bit configures the external I/O memory accesses to a "2N+1" wait state mode. This 2N+1 wait state mode also applies for external Program Memory and Data Memory accesses via the DWAIT field of the Wait State Control register and the PWAIT field of the System Control register.

The following assembly instructions are examples of how I/O memory locations can be accessed during run time:

```
ax0 = 0x1234;          /* Write a value to ax0 register */
IO(0x1ff) = ax0;       /* I/O Memory write */

ay1 = IO(ASIC_Host); /* Read data value from I/O Memory Mapped
                        ASIC */
```

Since I/O Memory space is a separate, dedicated memory space, the address mapping for I/O Memory space is not included as information in your Linker Description File. The only method of assigning (and accessing) I/O Memory in your system is during runtime in your assembly code. (I/O Memory space is not directly supported by the C Runtime Environment.)

Because of this restriction, in order to guarantee proper system performance, the programmer and system designer must take special care to ensure that the correct address mapping is performed both in hardware and in software.

Composite Memory Select

The ADSP-218x family processors have a programmable memory select signal, Composite Memory Select ($\overline{\text{CMS}}$). This signal lets you generate a memory select for devices mapped to more than one memory space, with the same timing as the other individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, and $\overline{\text{IOMS}}$).

Based on the value of the CMSSEL bit field (bits 11:8) in the Composite Select Control register (see Figure 8-9), the ADSP-218x processor asserts $\overline{\text{CMS}}$ when the corresponding memory select signal(s), $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, and $\overline{\text{IOMS}}$, are asserted. The $\overline{\text{CMS}}$ signal can be enabled to become active for any of these signals individually. By default after reset, the CMSSEL field is initialized to enable the $\overline{\text{CMS}}$ signal to become active for any $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, or $\overline{\text{IOMS}}$ memory access. ($\overline{\text{BMS}}$ is disabled.)

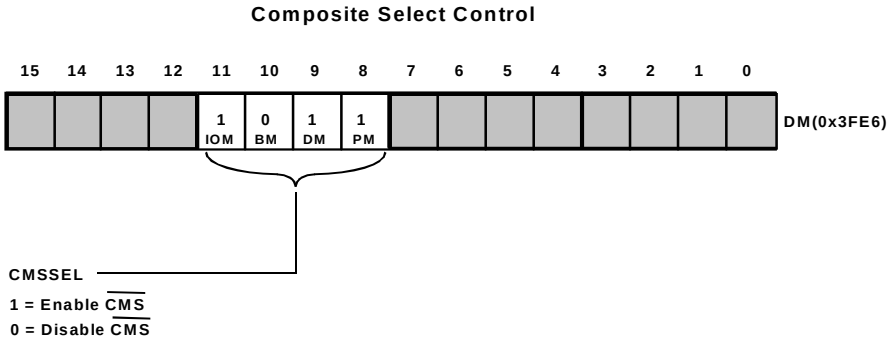

Figure 8-9. CMSSEL Selection for CMS Signal

Figure 8-10 and Figure 8-11 in the next sections provide two examples for using the $\overline{\text{CMS}}$ signal in system designs.

CMS Signal as Chip Select for 32 K x 8-Bit SRAMs

Figure 8-10 provides an example of using the $\overline{\text{CMS}}$ signal as a chip select for three 32 K x 8-bit SRAMs with no glue logic. The purpose of this chip select is to implement two pairs of 8 K external overlay regions: two for Program Memory and two for Data Memory.

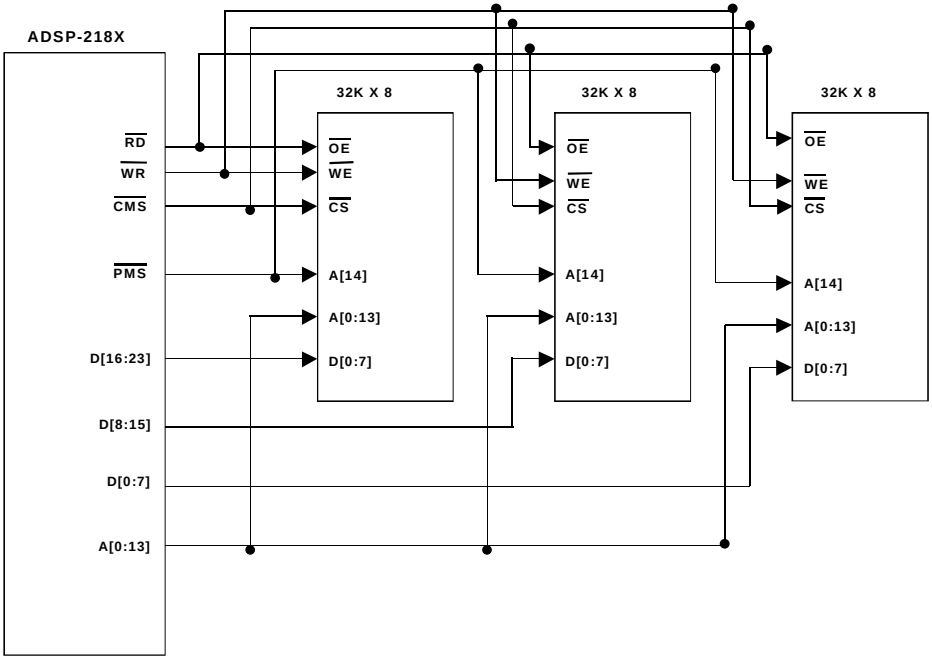

Figure 8-10. Example Using CMS Signal as a Chip Select

In this example, the $\overline{\text{CMS}}$ signal is configured to trigger for both Program Memory and Data Memory accesses (when the $\overline{\text{PMS}}$ or $\overline{\text{DMS}}$ signals are active). The $\overline{\text{PMS}}$ signal is used as the upper order address line (A[14]) to the SRAMs. When the DSP performs Program Memory accesses, the $\overline{\text{PMS}}$ signal becomes active (low), causing the A14 address line of the SRAMs to be driven low. When the DSP performs Data Memory accesses, the $\overline{\text{PMS}}$ signal becomes inactive, causing the A14 address line of the SRAMs to be driven high.

The main advantage of this implementation is that only three 32 K x 8-bit SRAMs are required for this configuration. Normally, five 16 K x 8-bit SRAMs are required to implement two pairs of 8 K overlay regions for Program Memory and Data Memory. This implementation helps to save on board "real estate" where board space is limited.

BMS Disable

For the following ADSP-218x models, there is a disable $\overline{\text{BMS}}$ control bit (bit 3 of the System Control register) that allows the processor core to enable or disable the $\overline{\text{BMS}}$ signal during Byte Memory accesses:

- ADSP-2184, ADSP-2184L and ADSP-2184N
- ADSP-2185L, ADSP-2185M, and ADSP-2185N
- ADSP-2186, ADSP-2186L, ADSP-2186M, and ADSP-2186N
- ADSP-2187L and ADSP-2187N
- ADSP-2188M and ADSP-2188N
- ADSP-2189M and ADSP-2189N

When $\overline{\text{BMS}}$ is disabled, it can be used with the $\overline{\text{CMS}}$ signal to allow the mapping of multiple memory devices to the Byte Memory space. Figure 8-11 provides an example of this use of the $\overline{\text{BMS}}$ and $\overline{\text{CMS}}$ signals.

In this example, the DSP is booted from an EPROM. By default after reset, the $\overline{\text{BMS}}$ signal is enabled for Byte Memory accesses. After the DSP has been booted and initialized during runtime, the system program can disable the $\overline{\text{BMS}}$ signal and also enable the $\overline{\text{CMS}}$ signal to trigger during $\overline{\text{BMS}}$ accesses. This process allows the $\overline{\text{CMS}}$ signal to chip select the FLASH or SRAM memory during runtime while leaving the $\overline{\text{BMS}}$ signal disabled. Leaving the $\overline{\text{BMS}}$ signal disabled prevents any contention between the two devices.

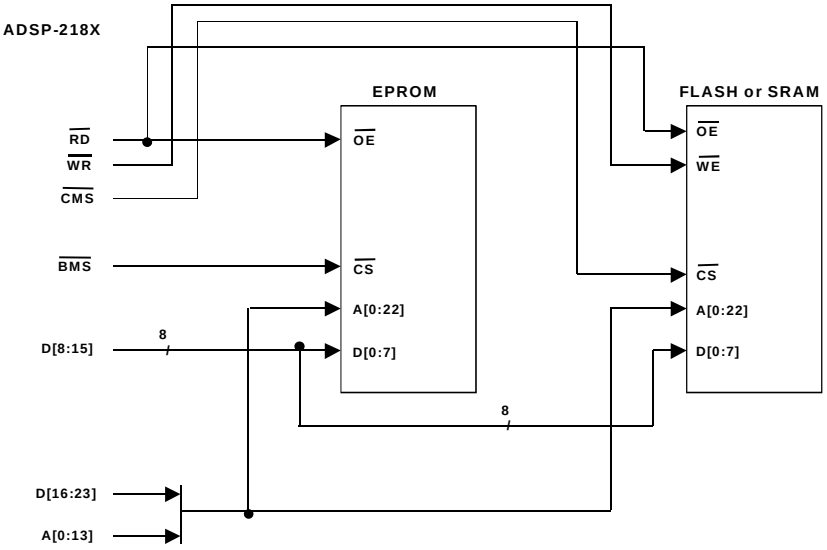

Figure 8-11. Example Using $\overline{\text{CMS}}$ Signal to Chip Select FLASH or SRAM Memory

Memory Interface Modes

All ADSP-218x family processors, except for the ADSP-2181 and ADSP-2183, are available in a 100-lead LQFP package. The ADSP-218x processors in 100-lead LQFP packages can be used in one of two modes; Full Memory Mode or Host Memory Mode. Full Memory Mode allows complete operation of the external 24-bit data and 14-bit address busses with full external overlay memory and I/O capability. Host Memory Mode allows complete IDMA functionality with limited external addressing capabilities. The operating mode is determined by the state of the Mode C pin *only* during the rising edge of the $\overline{\text{RESET}}$ signal. The operating mode cannot be changed while the processor is running.

Full Memory Mode

In Full Memory Mode, the ADSP-218x processors in 100-lead LQFP packages have complete use of the external address and data busses. In this mode, the processors behave in exactly the same manner as the ADSP-2181 and ADSP-2183 processor with the IDMA port removed.

The processors have a 24-bit external data bus, a 14-bit address bus and 5 memory select signals. Byte memory is accessed for data by using the middle eight bits of the data bus. The upper eight bits of the data bus combined with the 14 address pins provide a 22 bit address for Byte Memory space. All of these features behave exactly the same as they do on the ADSP-2181 and ADSP-2183. Hold Off cases (autobuffer cycle stealing, external memory accesses with wait states, and so forth) are simplified because an IDMA transfer never occurs. In this mode, the IDMA port is disabled as if IS was deselected or pulled high on the ADSP-2181 or ADSP-2183 processors.

Host Memory Mode

Host Memory Mode allows complete IDMA port operation with limited external addressing capabilities. It gives full use of the IDMA port as found on the ADSP-2181 and ADSP-2183 processors, but there are limitations on the use of the external memory bus. In Host Memory Mode the lower eight bits of the data bus, D[7:0], become IDMA control pins and IAD bus pins. The upper 13 bits of the address bus A[13:1] become the lower 13 bits of the IDMA address/data bus IAD[12:0]. IDMA transfers occur exactly as they do on the ADSP-2181 and ADSP-2183 processors.

Accessing Peripherals

The external bus in Host Memory Mode still remains available in a limited form. The processors' address pins A[13:1] are changed to IAD[12:0] when the Mode C pin is high. As a result, the chip cannot drive an address externally. However, internally, the chip behaves as if external accesses are occurring. The external bus behaves in the same way as an ADSP-2181 or ADSP-2183 system where address bits A[13:1] and data bits D[7:0] are ignored. The upper 16 bits of the data bus can still be used for external data transfers, but only one address bit is available, A0.

Writes to Data Memory or I/O Memory space activate the appropriate memory select(s), RD or WR, place data on D[23:8], and drive a single address bit on A0. Program Memory reads and writes behave similarly but have the added consideration of the PX register.

For Program Memory reads and writes, only the upper 16 bits will be available externally. When 24-bit data is written to external Program Memory, the upper 16 bits are driven out on data bus pins [23:16]. The PX register still latches the lower eight bits of the program memory word, but these bits are not driven externally. If a 24-bit read of external memory occurs, no external pins control the value of the PX register, and the PX register is written with all 1s.

The missing address bits restrict using the external bus with a conventional memory device, which has separated address and data buses. These external transfers might be usable with shared address/data memory chips, or they can be used for communication with an ASIC. The memory selects will still be active, so each memory space is effectively collapsed into two external addresses, address 0 and 1. Clever use of the $\overline{\text{CMS}}$ pin allows a user to decode 8 external addresses of 16-bit words using A0, IOMS, DMS, PMS and CMS. More addresses can also be provided by using the DSP's Flag Out pins as a memory select for a peripheral. Table 8-4 provides some possible 16-bit peripheral addresses for a total of 8 devices.

Table 8-4. Possible 16-Bit Peripheral Addresses

Memory Select	A0 (0 or 1)
$\overline{\text{PMS}}$	2 address locations
$\overline{\text{DMS}}$	2 address locations
$\overline{\text{IOMS}}$	2 address locations
$\overline{\text{CMS}}$	2 address locations

Byte Memory Accesses

BDMA accesses are still allowed in Host Memory Mode. However, because address pins A[13:1] became the IAD bus, construction of a complete byte address is impossible without the use of external address generators or latches, since only a single address bit (A[0]) is available.

Byte Memory addresses on the ADSP-2181 and ADSP-2183 processors are 22-bit addresses formed from D[23:16] and A[13:0]. In Host Memory Mode D[23:16] and A0 are the only address bits available externally. D[23:16] will be in the DMPAGE register value. A0 will be 1 for odd byte addresses and 0 for even byte addresses.

BDMA and IDMA timing and cycle stealing are the same as on the ADSP-2181 and ADSP-2183 processors. BDMA with limited address bits available still provides a flexible interface to the DSP. Without full address bits, addressing memory will be more difficult. However, host or micro-controller communication is possible because the order of the byte sequence is known.

Memory Interface Pins

Table 8-5 provides a description of Full Memory Mode pins, and Table 8-6 provides a description of Host Memory Mode pins on ADSP-218x processors in 100-lead LQFP packages.

Table 8-5. Full Memory Mode Pins (Mode C=0)

Pin Name	Number of Pins	I/O	Function
A13:0	14	O	Address Output Pins for Program, Data, Byte and I/O spaces
D23:0	24	I/O	Data I/O Pins for Program, Data, Byte and I/O spaces (8 MSBs are also used as Byte Memory addresses) **Note:** For 16-bit accesses, use pins 23:8.

Table 8-6. Host Memory Mode Pins (Mode C=1)

Pin Name	Number of Pins	I/O	Function
IAD15:0	16	I/O	IDMA Port Address/Data bus
A0	1	O	Address Pin for External I/O, Program, Data, or Byte access[1]

Table 8-6. Host Memory Mode Pins (Mode C=1) (Cont'd)

Pin Name	Number of Pins	I/O	Function
D23:8	16	I/O	Data I/O Pins for Program, Data Byte and I/O spaces
$\overline{\text{IWR}}$	1	I	IDMA Write Enable
$\overline{\text{IRD}}$	1	I	IDMA Read Enable
IAL	1	I	IDMA Address Latch Pin
$\overline{\text{IS}}$	1	I	IDMA Select
$\overline{\text{IACK}}$	1	O	IDMA Port Acknowledge Configurable in Mode D; Open Drain

1 In Host Memory Mode, external peripheral addresses can be decoded using the A0, CMS, PMS, DMS, and IOMS signals.