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ADSP-2189M Anomaly List for Revision 0.0-0.4

The list below represents the known anomalies and workarounds for the ADSP-2189M. The silicon revision of a particular device can be found on the chip, as shown below:

ADSP-2189M	Part Number
-xxx	Speed Grade/Package
xyzzzzzzz-**0.0**	Lot number and **silicon revision**
Dwwyy	Date code

The table below shows which ADSP-2189Ms have each anomaly. The left hand side of the table lists the type of anomaly and the numbers on the top of the table refer to the particular revision of the silicon. Any box that has an 'x' contained in it has that anomaly. For a complete description of the anomaly, please refer to the subsequent pages.

	0.0	0.1	0.2	0.3	0.4
1. Additional VDDINT current draw for active inputs	x	x	x	x	x
2. Speed Path with BDMA accesses into internal Overlay Memory	x	x	x	x	x
3. Speed Path with accesses to external Program and external Data Memory	x	x	x	x	x
4. Latency in ASTAT register writes from external memory	x	x	x	x	x
5. Industrial temperature range 85C to -20C	x	x	x	x	x

The latest anomaly sheets are available from the World Wide Web at:

http://www.analog.com/support/anomalies/anomalies.html

Anomaly #1

There is additional current on VDDINT when an active input is held high. Inputs disabled or held low are not affected. The extra current is approximately 170µA per high input. Note that the current is internal V_{DD} supply current and not input leakage current. During the powerdown state this additional current will dominate the measured current on $V_{DD(INT)}$. An example of the total current draw during powerdown is given below:

I_{DD} powerdown max current:		100µA
Pins Held High:	RESET	170µA
	BR	170µA
Total powerdown current:		440µA

This current draw will exist in all processor states (powerdown, idle and active). However,

the total current draw during the active state is typically great enough such that the additional draw on active inputs will be negligible.

Anomaly #2

When performing BDMA accesses with the BDMA Overlay Bits not equal to zero (bits 4-7 of the BDMA Control Register (0x3FE3)), the maximum speed which the part can operate is 72MHz. If the ADSP-2189M is operating at greater than 72MHz, BDMA accesses can be made only to internal memory overlay 0.

Anomaly #3

If the DSP is performing waitstated external memory accesses to Program or Data Memory, the maximum speed which the processor can operate at is 72MHz. External accesses with wait states equal to zero can operate at up to the maximum speed of the processor.

Anomaly #4

If you are executing the instruction:

```
ASTAT=DM(<addr>);
```

from external program memory (PMOVLAY=1 or 2), there will be a one cycle latency after the instruction finishes executing until the value in ASTAT will be valid. This means that your code must wait one cycle after this instruction executes before the ASTAT register can be safely tested or operated on.

Workarounds:

There are two potential workarounds for this anomaly:

1. If possible, place all Data Memory loads of the ASTAT register in internal memory.
2. If Data Memory loads of the ASTAT register must lie in external memory, make the next instruction a NOP.

This anomaly is unaffected by the number of waitstates used to access external program memory.