Using an External Switching Regulators to Supply an Adjustable Internal Voltage to Blackfin Processors.

Contributed by Tony Seliverstov   *Rev 3- January 30, 2007*

Introduction

The BlackFin family of processors include an optional internal programmable PWM voltage controller which is shown on Figure 1. Together with a set of external components (Q1,D1,L1 and C1-C5) they provide an adjustable voltage power supply for internal voltage.
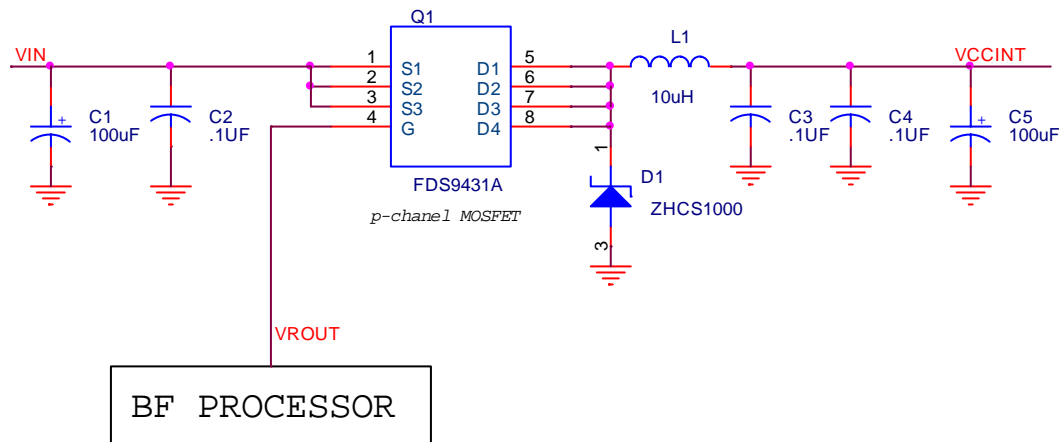
Figure 1.

The structure of the internal voltage regulator is based on a very simple voltage controller. It does not include current limiting functionality and synchronous rectification. It also does not include soft start capability.

This application note describes how an external regulator can be used in conjunction with internal voltage controller to:

- improve dynamic performance;
- improve efficiency;
- improve stability ;
- reduce   PCB area required and
- reduce rating required for components.

   This application note also provides guidelines for designing such regulator and give test results of prototypes .

Connecting BlackFin to External Buck Regulator

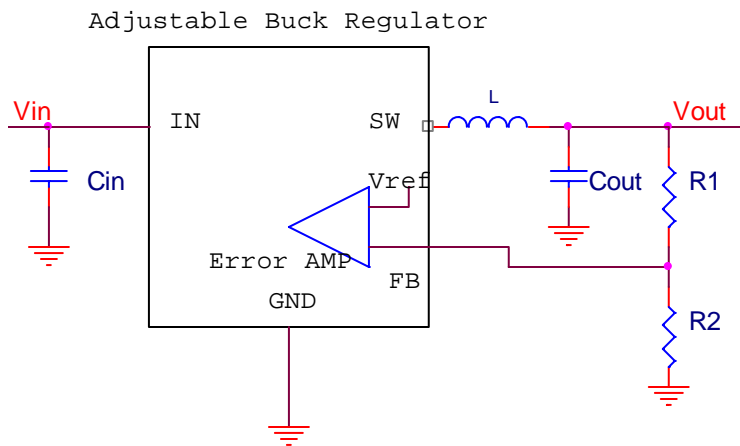Figure 2 shows the configuration of an adjustable Buck converter.

Figure 2

The value of regulator output voltage Vout is determined by voltage divider R1,R2 connected to feedback pin FB according to expression (1):

$$Vout = Vref (1 + R1/ R2) \qquad (1)$$

, where Vref is a value of regulator internal voltage reference.

The configuration of the voltage divider R1 and R2 may be modified as shown on Figure 3, with an additional resistor R3 and an additional voltage source Vcntrl.
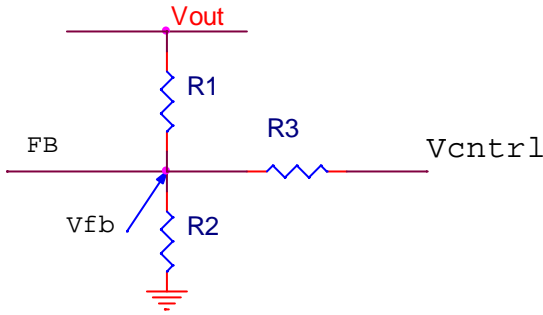

Figure 3

The fact that the Buck converter is a closed loop feedback system allows us to make the assumption that the voltage on FB Vfb is equal to the internal voltage reference Vref, That is,   Vfb = Vref.   The value of output voltage Vout may then be calculated as :

$$Vout = Vref (1 + R1/R2 + R1/R3) - Vcntrl (R1/R3) \qquad (2)$$

As seen from equation(2), the output voltage Vout is a function of   Buck regulator internal voltage reference (Vref) , external additional voltage   Vcntrl, and the ratios of resistors R1,R2,R3, which are connected to feedback pin FB of regulator. If the VRout pin of BlackFin will be connected through a low-pass filter to resistor R3, it will form an internal voltage regulator using BlackFin voltage controller as part of an additional feedback loop.

The voltage on the VRout pin of BlackFin is a PWM voltage with a duty cycle D. After passing this through low-pass filter the generated DC voltage (Vcntrl) can be expressed as:

$$Vcntrl = D \times Vin \qquad\qquad\qquad (3)$$

, where Vin is the value of DC supply voltage on I/O pins of BlackFin processor. Let's see how to choose values of all the parameters and components to provide reliable regulator operation.

The values of some of the components and parameters are "known" before we start the design :

a) Vout ---- Vout-min= 0.8V, Vout-max = 1.2 V, defaulted value on power up is 1.2 V ;

b) Vin-nom ---- 3.3 Volts , specified range is Vin-min= 2.7 Volts to Vin–max=3.6 Volts ;

c) Vref ----- 0.6- 1.2 Volts determined by specification of regulator manufacturer;

d) R1 and R2 value are usually specified by Buck regulator manufacturer;

e) D should be in range 0.2 – 0.7 to provide a specific dynamic range margin for the BlackFin controller. Using equation (3), we determine the range of Vcntrl as

Vcntrl-min = Dmin x Vin-min = 0.54 V to

Vcntrl-max = Dmax x Vin-max =2.52 V .

We then find the values of R3 and parameters of low-pass filter. Because of a large variation in the values of R1 and R2 that are recommended by different regulators manufacturers, we should use the ratios R1/R2, R1/R3 and R1/R2.

Let's assume that R2=R3 , this means that R1/R2= R1/R3 . Expression (2) for the maximum core voltage Vout-max may be rewritten as :

Vout-max = Vref (1 + 2R1/R2) – Vcntrl-min x R1/R2   (4)

Solving expression (4) for Vref=0.8V:

1.2 = 0.8 (1+ 2R1/R2) - 0.54 x R1/R2 which gives R1/R2 = 0.4 for Vref=0.8V.

   Using the same process, optimal values of ratio R1/R2 for different Vref may be found:

  for Vref= 0.6V optimal R1/R2=0.9, for Vref=1.0V - R1/R2 = 0.43 .

Table 1 presents numerical values of expression (2) for Vref=0.8V and R1/R2=0.4

TABLE 1

Vout , V	1.2	1.1	1.0	0.9	0.8
Vcntrl , V	0.60	0.85	1.10	1.32	1.80
D for Vin =2.7 V	0.22	0.31	0.41	0.50	0.67
D for Vin=3.3 V	0.18	0.26	0.33	0.40	0.54
D for Vin= 3.6 V	0.17	0.24	0.30	0.37	0.50

   As shown in Table 1, all calculated parameters are in the range of what was considered in the original preliminary design assumptions.

   The VROUT PWM signal should also be low-pass filtered before it can be used as Vcntrl. The best way of implementing low-pass filter function is by splitting resistor R3 in two resistors R3a and R3b and putting a filtering capacitor C3 to GND as shown in Figure 4:
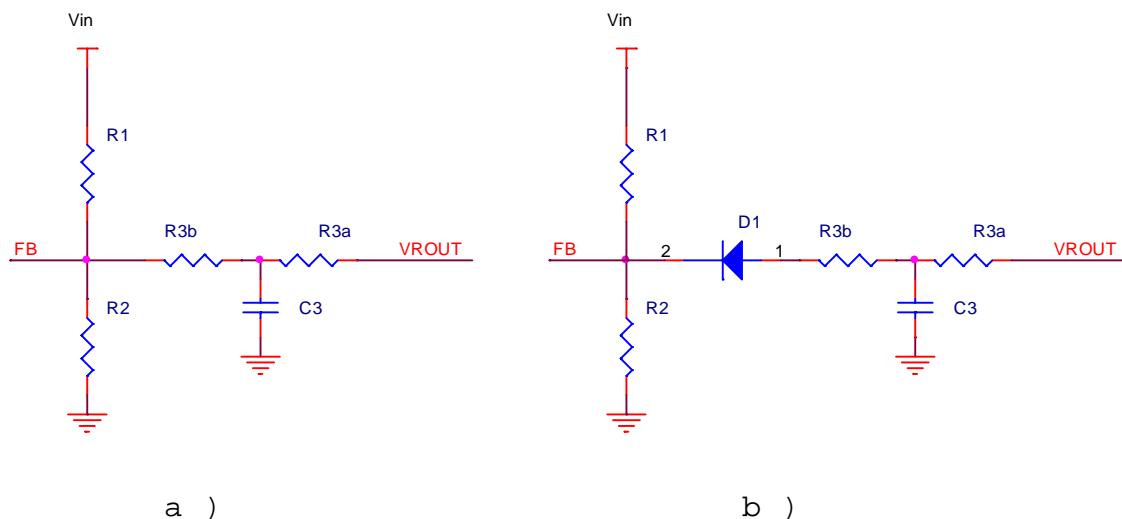
a)   b)

Figure 4

The value of capacitor C3 may be chosen from expression for cut-off frequency
of the low-pass filter:

$$f_c = \frac{1}{2\pi R_3 C_3}$$

The cut-off frequency fc should be chosen to be around 100kHz to provide effective
filtering of the 1MHz PWM VROUT signal (and not to reduce bandwidth of external
regulator) . Diode D1 shown in Figure 4b serves as decoupling component for the
impeadance of the VROUT pin in order to prevent additional biasing of regulator
feedback input . The diode forward voltage Vdf should be low enough not to
substantially increase the value of the needed Vcntrl signal. A Panasonic schottky barrier
diode MA27D29 has a value of forward voltage of Vdf=0.25 V ,which is low enough to
be used in this application. For other diodes, the calculation of ratio R1/R2 should be
made by adding value of Vdf to the value of Vcntl-min.

Practical implementation and test results.

The layout of the PCB and lead-lag compensation of the error amplifier of the external voltage regulator are the most critical aspects of a practical implementation of core power supplies using this method, because additional feedback loop of BlackFin voltage controller may cause instability of that power supply.

In the PCB layout process, designers should follow the recommendations of the manufacturer of the chosen regulator. In most of the voltage regulator specifications, the recommended PCB layout is given and designers should make their PCB layout as close as possible to that recommended layout.

Configuration and values of error amplifier compensation components are given by the manufacturer of a chosen voltage regulator. Usually that provides stable operation of the regulator. If the regulator is unstable with recommended values of compensation components, try to make compensation more "stiff", by decreasing value of compensation resistor and proportionally increasing value of compensation capacitor.

BlackFin processor internal voltage regulator was successfully implemented with several external regulators:

a) Linear Technology LTC3406 on single core BlackFin processors ADSP-BF533 and BF537.

   The LTC 3406 doesn't need any external compensation.

b) Linear Technology LTC3411 on dual core BlackFin processor ADSP-BF561.

   Compensation: Rc=1.3kOhms, Cc=10 000 pF .

c) ADI ADP3051 on single core BlackFin processor ADSP-BF537 on PoSt537 application board.

   Compensation : Rc=6.2 kOhms, Cc=3 900 pF.

   The schematic of "core" voltage power supply using ADSP3051 regulator implemented on PoSt 537 board is shown in Figure 5:

Figure 5

NAND-gate U7, resistors R194,R219 , capacitors C91,C92 and diode D9 form
the circuitry responsible for the "hibernate-wake up" function of "core" voltage
supply. Pin 7 of voltage regulator U7 "/SHDN" in normal operation should be in
the "high" logical state and for "hibernate" mode of operation should be in the
"low" logical state.

     The operation of that circuit is based on two assumptions:
a) in normal mode operation the VROUT signal is always a PWM signal;
b) in hibernate mode of operation the VROUT is in "high" logical state.

The timing diagram of "normal/ hibernate" mode of operation is presented on
Figure 6.

Figure 6

Results of measuring efficiency of PoSt37 board "core" voltage regulator presented in Table 2.

Table 2

CONDITIONS Load, Preset Voltage	Vin, Volts	Vcore, Volts	Iin, mA	Icore, mA	Pin mW	Pcore mW	Efficiency %
Low, 1.20 V	3.3	1.255	23.2	54.2	76.56	68.02	88.8
Low, 1.00 V	3.3	1.049	16.0	41.1	52.8	43.11	81.6
Low, 0.90 V	3.3	0.94	12.8	35.8	42.24	33.65	79.7
Low, 0.85 V	3.3	0.89	11.7	32.6	38.61	34.47	89.3
Middle, 1.20 V	3.3	1.26	43.7	103.2	144.2	130.0	90.2
Middle, 1.00 V	3.3	1.055	29.0	78.9	95.7	83.24	87.0
Middle, 0.9 V	3.3	0.943	22.9	68.5	75.57	64.59	85.4
Middle, 0.85 V	3.3	0.897	22.4	65.5	73.92	58.75	79.5
High, 1.20 V	3.3	1.278	76.3	181.7	251.8	232.2	92.2
High, 1.00 V	3.3	1.067	51.4	142.5	169.6	152.05	89.6
High, 0.90 V	3.3	0.951	41.7	124.0	125.1	118.0	95.1
High, 0.85 V	3.3	0.901	36.3	115.3	119.8	103.9	86.7

Figure 7 represents transition from hibernation mode to full on operation:

Ch1- Vcore, 200 mV/Div, upper trace on Figure 7;

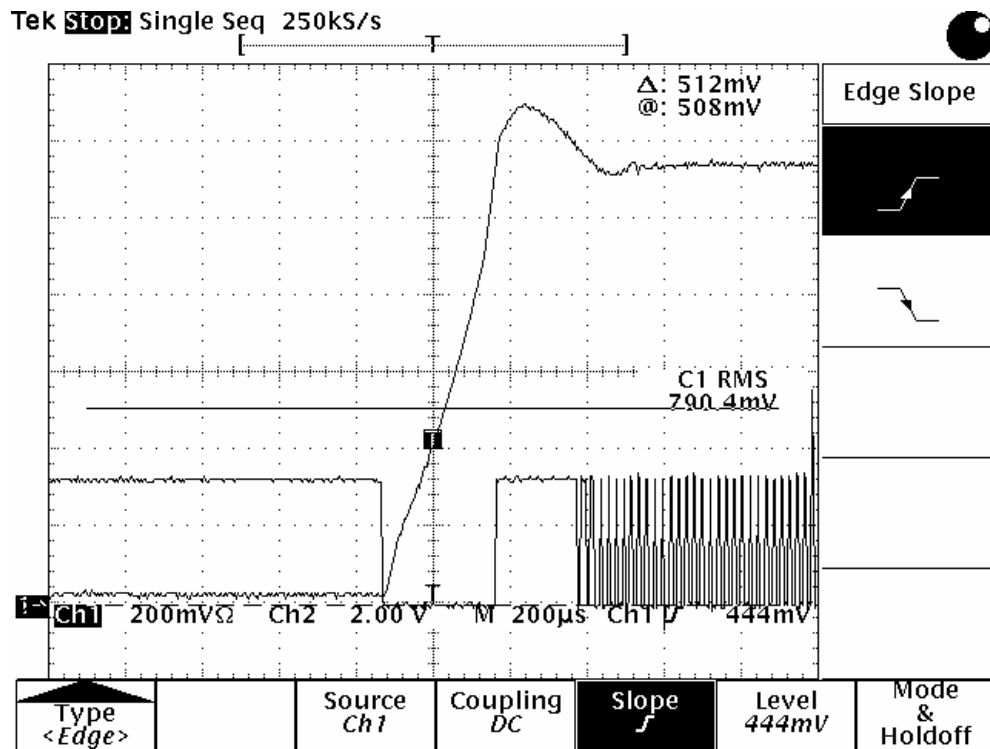Ch 2- VCORE, 2.0 V/Div, lower trace on Figure 7.

Figure 7