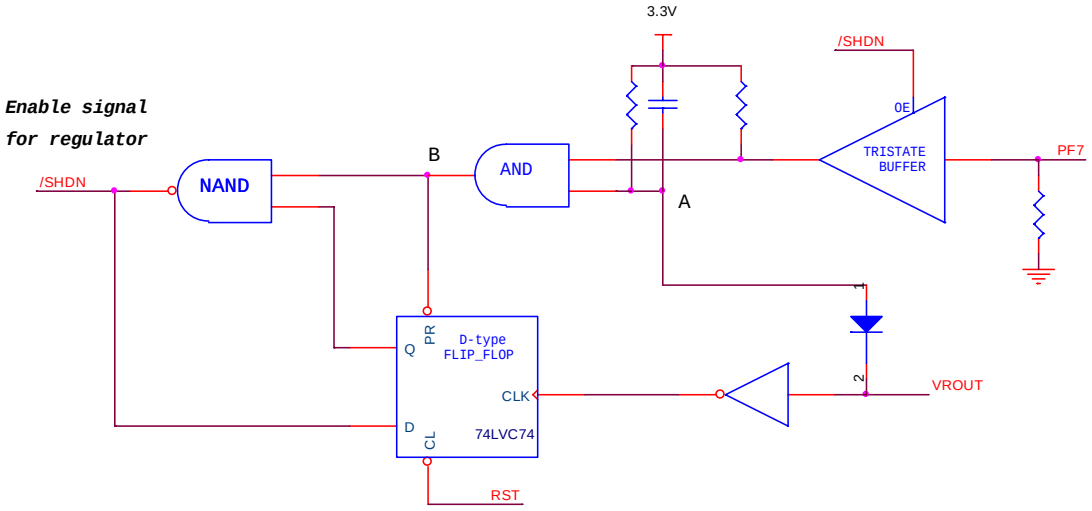
EXTERNAL CIRCUITRY FOR "HIBERNATE_ WAKE UP" FUNCTION ON BLACK FIN PROCESSOR WITH A FIXED VOLTAGE EXTERNAL VOLTAGE REGULATOR .

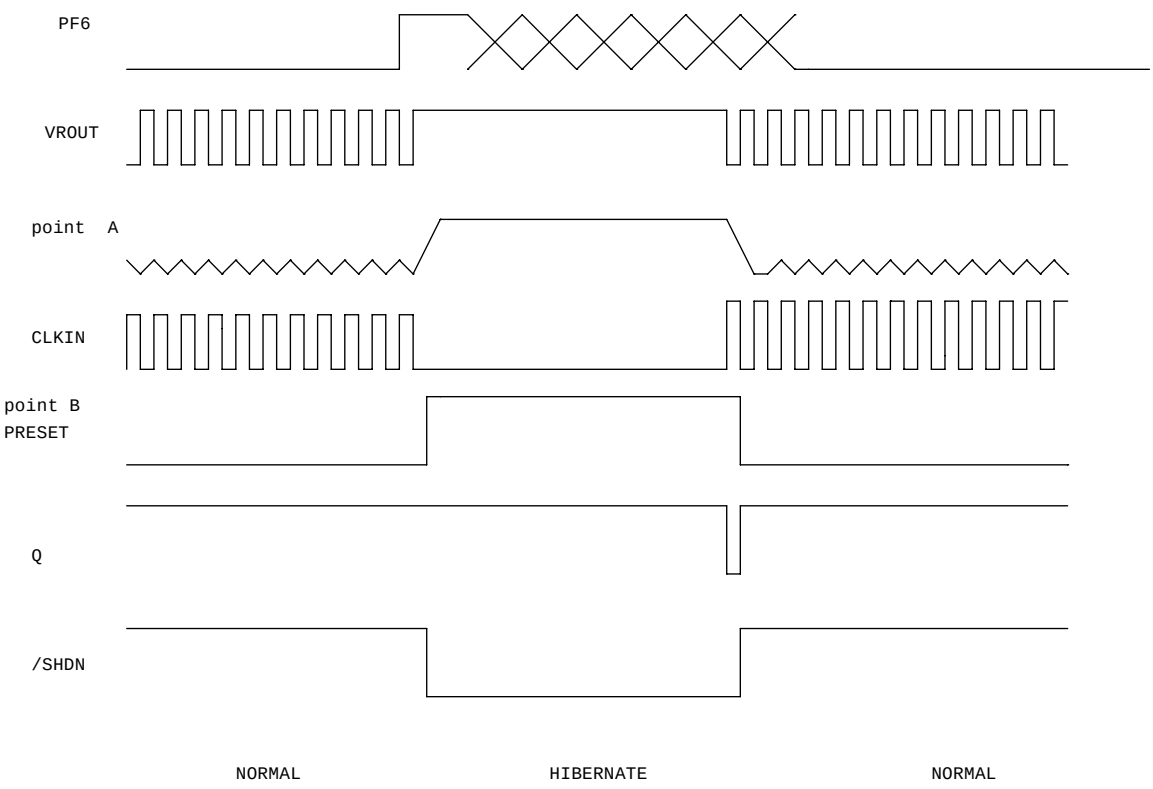
Initial assumptions for implementing hibernate/wake up circuitry are:

1) General purporse I/O signal starts the process of switching from normal operation to hibernation;
2) In "normal" mode of operation the VROUT signal is iither "low" or in any duty cycle PWM mode;
3) VROUT signal in "hibernate" state is switches to "high" logic level;
4) VROUT signal in the moment of transition from "hibernation" state to normal have at least one transition "high" to "low" logic level.

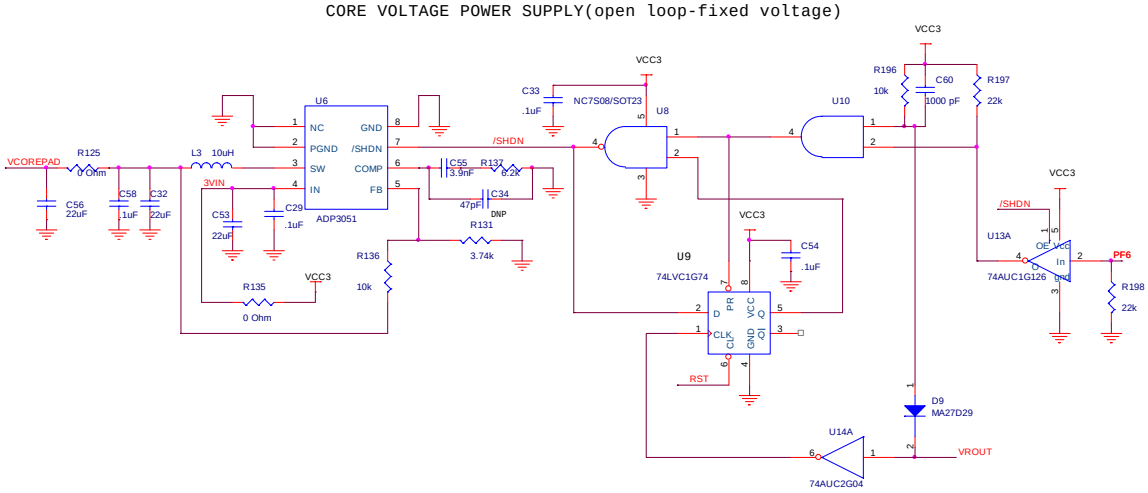
"HIBRRNATE/ WAKE UP" logic for open loop fixed voltage external regulator



HIBERNATE / WAKE-UP TIMING DIAGRAMM

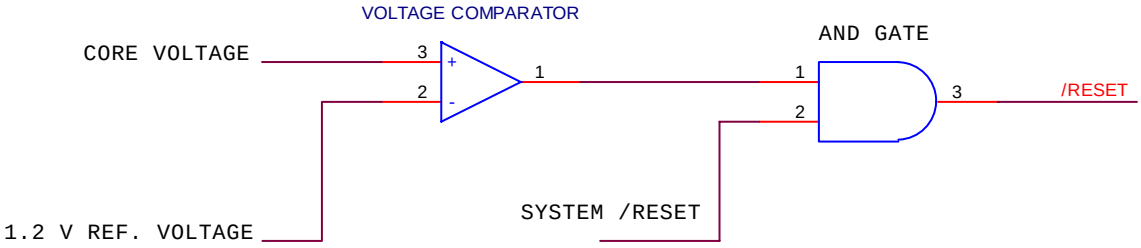


Practical implementation on PoST537 board:



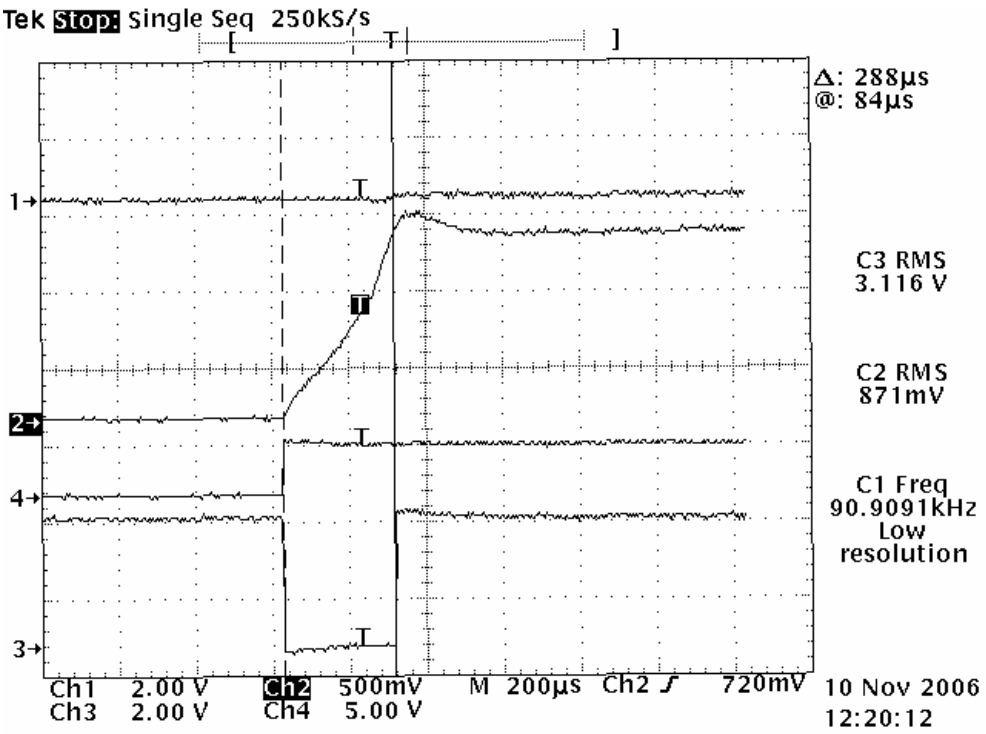
The voltage level on VCCCOREPAD should be set below the voltage of the internal voltage controller setting. If You use the defaulted setting Vrefint=1.2V, the“core” voltage should be set to level lower than 1.2V, i.e. 1.1 volts.

After a wake-up event, the “core” voltage starts to built up. The time when it reaches a nominal value may be different for different regulators and for different values of total output capacitance. That means that a circuitry “power OK” needs to be implemented . That circuit should include a voltage comparator and a two inputs AND gate as shown in the schematic below:



During the time when the “core” voltage is less than the defaulted value of 1.2 Volts, the processor will be kept in a “reset” state.

An oscillogram plot of a practical circuit tested with the PoSt 537 board is shown below:



This plot shows the process of wake-up from hibernation.

Where : Ch1 – PF7;
Ch 2- Vcore ;
Ch 3 - /RESET;
Ch 4 - /SHDN.