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Switching Regulator Design Considerations for ADSP-BF533 Blackfin® Processors

Contributed by Bob Libert, Brian Erisman, and Joe Beauchemin

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Introduction

The Blackfin® embedded processor's on-chip voltage regulator is a switching buck regulator that requires external components to function properly. This application note describes how buck converters work and provides guidelines for choosing the external components for the control circuit to work with ADSP-BF531 / ADSP-BF532 / ADSP-BF533 Blackfin processors. Since the design of the internal voltage regulator is similar to other Blackfin processors, this note applies to the ADSP-BF534 / ADSP-BF536 / ADSP-BF537 and the ADSP-BF561 processors as well.

Internal Voltage Regulator

The internal voltage regulator on Blackfin processors is a buck converter that reduces the input voltage, which can range from 2.25 V to 3.6 V, to the voltage applied to the core, which is programmable from 0.8 V to 1.2 V.

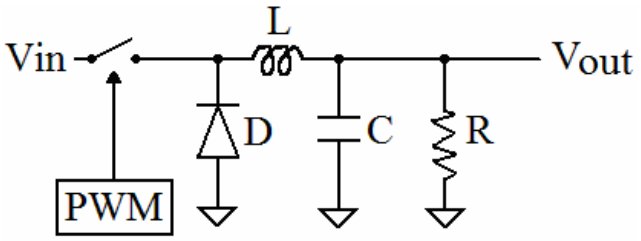

Figure 1. Basic Buck Converter

A buck converter consists of a switch, an inductor, a diode, a capacitor, and a pulse-width modulator (PWM), as shown in Figure 1.

The PWM controller is internal to Blackfin processors, and the rest of the components are external.

A control loop senses the regulator voltage and sets the duty ratio (D) of the PWM to generate the programmed voltage, where D is approximately:

$$D = \frac{Vout + V_d}{Vin + V_d}$$

As can be seen in this equation, the forward voltage of the diode (V_d) contributes to both terms. Variations in the diode's forward voltage and input and output voltages cause D to range from approximately 30% to 63%.

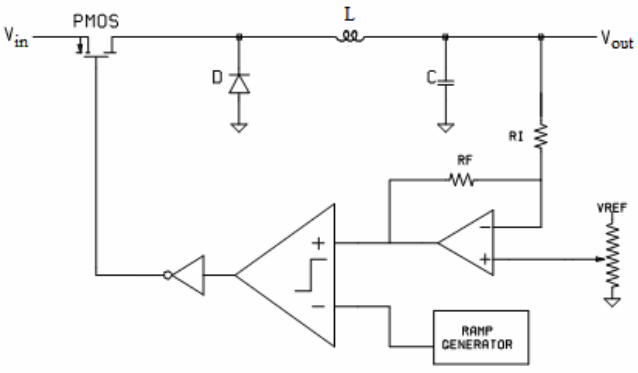

Figure 2. Internal Voltage Regulator Circuit

The internal voltage regulator circuit (Figure 2) consists of a voltage reference, an error amplifier, a ramp generator, a comparator, and a driver.

There are two states for the switch, closed (T_{on}) and open (T_{off}), where D is defined as:

$$D = \frac{T_{on}}{T_{on} + T_{off}}$$

During T_{on}, the switch connects the supply voltage (V_{in}) to the inductor (L), causing the current in the inductor to ramp up.

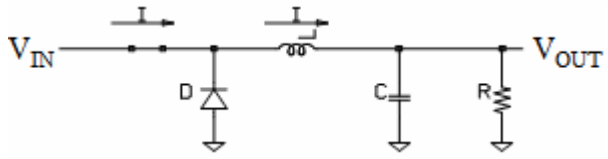

Figure 3. Switch Behavior During T_{on}

During T_{off}, the switch is off and the diode turns on, which results in a negative voltage across the inductor. This, in turn, causes the current to decrease.

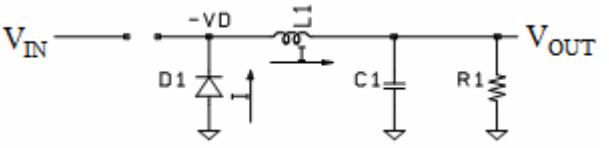

Figure 4. Switch Behavior During T_{off}

The average current is load current (I_{load}). The waveforms for the inductor current ($I_{inductor}$) and the voltage at the input to the inductor (V_{in}) should resemble Figure 5.

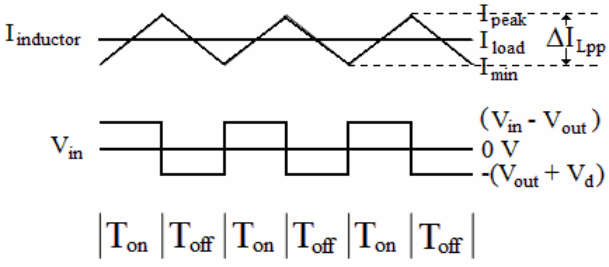

Figure 5. Inductor Wave Forms

Another parameter introduced in Figure 5 is the inductor ripple current (ΔI_{Lpp}). This is the peak-to-peak measurement of current values that can be expected to flow through the inductor.

The real circuit will also contain a number of parasitic elements associated with the external components. The PMOS FET has two parasitic elements which reduce its efficiency. The first is $R_{DS(on)}$, the resistance between the drain and the source. The power lost between the drain and the source (P_{RDS}) is the power dissipated within the channel of the FET itself, which is present only during the T_{on} period, and is simply:

$$P_{RDS} = I_{load}^2 * R_{DS(on)} * D$$

The second parameter affecting the FET's efficiency is its gate charge (Q_G). The loss due to Q_G (P_{QG}) occurs during both switching periods, when the gate driver charges and discharges the gate (V_{gs}). The value of P_{QG} depends on the switching frequency (f_{SW}) and the turn on (T_r) and turn off (T_f) times of the gate, and is defined as:

$$P_{QG} = f_{SW} * ((V_{in}/2)*(I_{load}*(T_r+T_f)) + (Q_G*V_{gs}))$$

The inductor has a DC resistance (R_L). The loss due to R_L (P_{RL}) is defined as:

$$P_{RL} = I_{load}^2 * R_L$$

The largest contributor to overall loss is within the diode. The diode limits its efficiency (P_D) because it has a forward voltage (V_d) that is on during the T_{off} time and is dependent on I_{load}. The efficiency degradation caused by the diode is implicit in the equation:

$$P_D = I_{load} * V_d * (1 - D)$$

The output filter capacitor has a parasitic inductance (L_{ESL}) and resistance (R_{ESR}). Parasitic inductance has no first-order effect on efficiency, but degrades the filter performance by increasing the output ripple and raising the burden on other load bypass capacitors. Parasitic resistance

degrades efficiency and directly translates inductor ripple current into what is usually the dominant component of output ripple voltage. The power loss due to R_{ESR} is given by:

$$P_{ESR} = (\Delta I_{Lpp}{}^{2} * R_{ESR}) / 12$$

Analyzing the loss models for the two switch-states yields two simple observations. Figure 6 shows the equivalent circuit diagram with the switch on, which eliminates the diode.

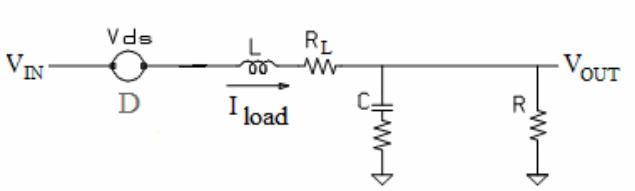

Figure 6. On-State Loss Model

Figure 6 shows that the switch's on-state loss is in series with the input source V_{in}, therefore, an equivalent voltage loss term, V_{ds}, can be subtracted from the input voltage in the D equation:

$$D = \frac{V_{out} + V_d}{V_{in} - V_{ds} + V_d}$$

Similarly, Figure 7 depicts the equivalent circuit diagram with the switch open:

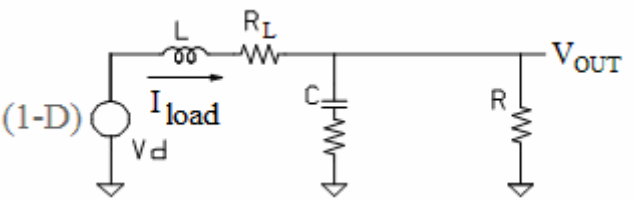

Figure 7. Off-State Loss Model

Here, the observation can be made that the output inductance loss is in series with the output, so an equivalent voltage loss term can be added to the output, and is simply the inductor's equivalent resistance (R_L) multiplied by the load current (I_{load}). Thus, the D equation becomes:

$$D = \frac{(V_{out} + (I_{load} * R_L) + V_d)}{(V_{in} - V_{ds} + V_d)}$$

Buck converters usually work in what is called the continuous mode. In the continuous mode of operation, the current through the inductor rises during the T_{on} state and falls during the T_{off} state, and the switching frequency (f_{SW}) spans the two states:

$$f_{SW} = 1 / (T_{on} + T_{off})$$

The voltage regulator runs in continuous mode during normal Blackfin processor operation (i.e., in Full On mode and Active mode).

The other mode of operation, discontinuous mode, is the mode in which there is a period of time after T_{off} when there is no current flowing in the inductor. This occurs when the Blackfin processor is in a low-power state with a low voltage on the core supply. Usually, this is a mode to be avoided because it changes the loop characteristics. Figure 8 shows the impact on inductor current for the two modes of operation:

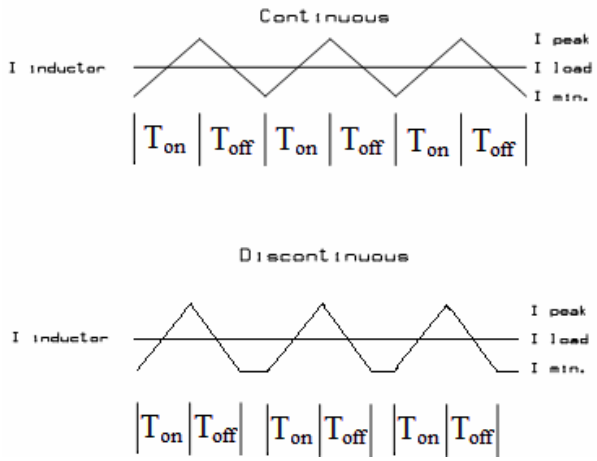

Figure 8. Continuous I_L vs Discontinuous I_L

In the discontinuous plot above, the space between T_{off} and the subsequent T_{on} is referred to as "dead time".

External Component Selection

The four external components of the regulator and the bypass capacitor on the input supply voltage need to be chosen to fit the operation of the Blackfin processor's internal switching regulator. Tradeoffs can be made with respect to cost or efficiency. Each component has parasitic elements. Reducing these parasitics usually improves efficiency, but may add cost.

Power Transistor (FET)

The gate drive inside the Blackfin processor's internal regulator was designed to provide a maximum drive current of 200 mA. A small internal current-limiting resistor, parasitics from bond wires, and package leads limit the actual charge time and reduce the efficiency. The FET to be chosen should have a gate charge (Q_G) of less than 20 nC.

The other critical parameter of the FET is its $R_{DS(on)}$. In general, lower is better; however, since the supply voltage (V_{gs}) can vary from 2.25 V to 3.6 V, be sure to examine the $R_{DS(on)}$ vs. V_{gs} curve in the FET data sheet. Check the $R_{DS(on)}$ component for the minimum V_{gs}.

The breakdown voltage (BVD_{SS}) should not be a problem, since most FETs have breakdowns greater than 12 V. Since the maximum V_{in} is 3.63 V, the expected diode voltage should result in a total voltage of around 4 V. Being ultra-conservative, the specified BVD_{SS} should exceed roughly twice this value. The power dissipation on the switch should be specified to be greater than 0.5 W.

In summary, the FET should meet these minimum requirements:

$R_{DS(on)}$ @V_{gs} = 2.5V or less	< 0.2Ω
Gate charge	< 20nC
Power dissipation	> 0.5W
BVD_{SS}	> 10V

Inductor

Given a pre-selected switching frequency and fixed PWM control, the inductor controls the amount of current ripple, the response of the control loop, and whether the regulator runs in continuous mode or discontinuous mode. The minimum value for the inductor (L_{min}) can be calculated from the following equation:

$$L_{min} > \frac{(V_{in} - V_{out}) * D}{(\Delta I_{Lpp} * f_{SW})}$$

Recall that the ΔI_{Lpp} term is the peak-to-peak magnitude of the ripple current in the inductor, which, under steady-state conditions, is the current that flows into the output capacitor. Under steady-state conditions, the duty ratio (D) is adjusted by the feedback loop in such a way that the magnitude of ramp-up and ramp-down currents in the inductor will be equal (Figure 8). However, note that a minimum load current is necessary to keep the regulator in continuous mode. This current is known as the *critical current*, and is represented as $I_{critical}$. Figure 9 depicts how $I_{critical}$ relates to ΔI_{Lpp}:

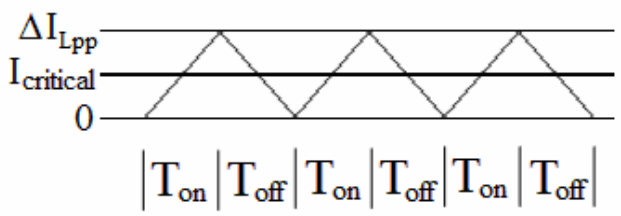

Figure 9. Inductor Current

For minimal inductance values, ΔI_{Lpp} is assumed to be ***twice*** $I_{critical}$.

Because of the wide range of operating conditions, the choice of inductor involves some compromise. The calculated values for all load conditions range from 0.9 µH to 68 µH. One value will not allow continuous operation or fast response to transients. A 10 µH inductor was chosen to cover most of the operating range at the 1 MHz default clock frequency.

Choosing the inductor value alone is not sufficient, as there are other parameters that should also be considered when selecting the inductor for the regulator circuit.

Minimize the DC resistance in the inductor (R_L) to about 0.1-0.25 Ω (typical). The inductor's resistance (R_L) and load impedance (R) also affect the DC gain.

The RMS current rating (I_{rms}) must be able to handle the maximum current expected from the Blackfin processor. Refer to the application note *Estimating Power for ADSP-BF533 Blackfin Processors (EE-229)* [1] for details regarding how to compute this value.

The saturation current (I_{sat}) must be greater than the I_{rms} plus ½ ΔI_{Lpp} plus a safety margin. Some I_{sat} maximum specifications state that the maximum is when the inductance is reduced by 10%.

Finally, the inductor should be specified for 1 MHz to support all three programmable switching frequencies.

Capacitors

Two capacitors must be specified, each with its own requirements.

The first capacitor is the power supply bypass capacitor. Because of the switching transients that may adversely affect the power supply, a low ESR (R_{ESR}), >68 µF electrolytic capacitor and a 0.01 µF (or 0.1 µF) ceramic capacitor must be connected as close as possible to the source of the switching FET.

The filter capacitor should have R_{ESR} in the range of 20 to 40 mΩ, because the R_{ESR} adds zero to the loop response, which cancels one of the LC poles. This restriction is true by virtue of voltage mode control use:

$$\frac{V_{out}}{V_{sw}} = \frac{(s * R_{ESR} * C + 1)}{(s^2 * L * C * (1 + \frac{R_{ESR}}{R})) + (s * (\frac{L}{R} + R_{ESR} + 1))}$$

The R_{ESR} also contributes to the ripple:

$$\Delta V_{out} = \Delta I_{Lpp} * R_{ESR}$$

One equation for the minimum value (C_{min}) of the filter capacitor is:

$$C_{min} = \frac{\Delta I_{Lpp}}{(f_{SW} * \Delta V_{out})}$$

However, since the value of the capacitor also affects the loop response, a minimal value may cause excess ripple and/or oscillations. To meet the loop response criteria and provide good transient response, the inductor value should be near its minimum and the capacitor/inductor pole should be set to about 10 kHz. The zero from the R_{ESR} and capacitor should be about three to five times the pole frequency.

Diode

A Schottky diode is recommended to reduce the loss associated with the forward diode voltage (V_d), although any switching diode can be used with a reduction in efficiency. The diode should also be able to handle the maximum load current.

Design Example

The following is a sample design that can be used as a reference. The sample has the following parameters:

V_{in} = 3.3V

V_{out} = 1.2V (default)

f_{SW} = 1MHz (default)

I_{load} = 300mA

ΔI_{Lpp} = 30% of I_{load} (ripple current)

ΔV_{out} <10mV (ripple voltage)

R_L = 0.046Ω

$R_{DS(on)}$ = 0.18Ω

Q_G = 8.5nC

$T_r = T_f = 35ns$

$V_d = 375mV$

$R_{ESR} = \sim 60m\Omega$

Some of the above specifications are taken from data sheets of specifically chosen components. For this design example, the following components are being used:

Inductor – Miller PM3316 15µH [2]

FET – Fairchild FDS9431A [3]

Diode – Zetex ZHCS1000 [4]

Capacitor – Tantalum 100µF

From this particular design example's sample characteristics and the specifications given by the chosen components, the theories discussed in this note can be applied to obtain values for minimum inductance (L_{min}) and minimum capacitance (C_{min}). From there, the pole frequency (F_{pole}), the capacitor and R_{ESR} zero frequency (F_{zero}), and efficiency (η) can be calculated as well.

In addition to the parameters detailed above, the duty ratio and ripple current must first be obtained before using the given equations for the inductor and capacitor.

Before solving for D, V_{ds} must first be obtained:

$V_{ds} = I_{load} * R_{DS(on)}$

$V_{ds} = 300mA * 0.18\Omega$

$V_{ds} = 54mV$

This V_{ds} value is then substituted into the D equation:

$$D = \frac{(V_{out} + (I_{load} * R_L) + V_d)}{(V_{in} - V_{ds} + V_d)}$$

$$D = \frac{(1.2V + (300mA * 0.046\Omega) + 375mV)}{(3.3V - 54mV + 375mV)}$$

$D = 0.44$

Note that this D value falls within the expected range of 30% to 63%.

The second unknown in the L_{min} equation is the ripple current:

$\Delta I_{Lpp} = 30\% * I_{load}$

$\Delta I_{Lpp} = 0.3 * 300mA = 90mA$

This value can be substituted into the L_{min} equation along with D:

$$L_{min} > \frac{(V_{in} - V_{out}) * D}{(\Delta I_{Lpp} * f_{SW})}$$

$$L_{min} > \frac{(3.3V - 1.2V) * 0.44}{(90mA * 1MHz)}$$

$L_{min} > 10.27\mu H$

A 15 µH inductor satisfies the above L_{min} requirement. If a 15 µH inductor is chosen, the ripple current then becomes:

$$\Delta I_{Lpp} = \frac{(V_{in} - V_{out}) * D}{(L * f_{SW})}$$

$$\Delta I_{Lpp} = \frac{(3.3V - 1.2V) * 0.44}{(15\mu H * 1MHz)}$$

$\Delta I_{Lpp} = 62mA$

Now the minimum capacitance can be computed. Knowing that the 10 mV specification is a maximum voltage ripple number, the C_{min} equation can be used:

$$C_{min} = \frac{\Delta I_{Lpp}}{(f_{SW} * \Delta V_{out})}$$

$$C_{min} = \frac{62mA}{(1\ MHz * 10mV)}$$

$C_{min} = 6.2\mu F$

The transient response depends on the output impedance of the filter (Z), which is:

$$Z = \sqrt{\frac{L}{C}}$$

$$Z = \sqrt{\frac{15\mu H}{6.2\mu F}}$$

$Z = 1.56\Omega$

To reduce the output impedance and improve the transient response, the cap is increased to 100 µF. Z then becomes 0.39 Ω.

Next, the pole (F_{pole}) can be calculated:

$$F_{pole} = \frac{1}{2\pi\sqrt{LC}}$$

$$F_{pole} = \frac{1}{2\pi\sqrt{15\ \mu H * 100\ \mu F}}$$

F_{pole} = 4109 Hz = ~5kHz

And the zero (F_{zero}) becomes:

$$F_{zero} = \frac{1}{(2\pi * R_{ESR} * C)}$$

$$F_{zero} = \frac{1}{(2\pi * 60m\Omega * 100\mu F)}$$

F_{zero} = 26.5kHz

These F_{pole} and F_{zero} values are within the desired limit for stability.

To address efficiency, the total power loss in the circuit must be accounted for and subtracted from the total power output (P_{out}) at the load:

$P_{out} = V_{out} * I_{load}$

P_{out} = 1.2V * 300mA

P_{out} = 360mW

The losses in the circuit, as described previously, are P_{RDS}, P_{QG}, P_{RL}, P_D, and P_{ESR}.

Computing P_{RDS}:

$P_{RDS} = I_{load}^2 * R_{DS(on)} * D$

$P_{RDS} = 300mA^2 * 0.18\Omega * 0.44$

P_{RDS} = 7.1mW

Computing P_{QG}:

$P_{QG} = f_{SW} * ((I_{load} * (T_r + T_f)) + (Q_G * V_{gs}))$

P_{QG} = 1MHz*((300mA*(35ns+35ns))+(8.5nC*3.3V))

P_{QG} = 49mW

Computing P_{RL}:

$P_{RL} = I_{load}^2 * R_L$

$P_{RL} = 300mA^2 * 0.046\Omega$

P_{RL} = 4.1mW

Computing P_D:

$P_D = I_{load} * V_d * T_{off}$

P_D = 300mA*375mV*(1-0.44)

P_D = 63mW

Computing P_{ESR}:

$P_{ESR} = (\Delta I_{Lpp}^2 * R_{ESR}) / 12$

$P_{ESR} = (62mA^2 * 60m\Omega) / 12$

P_{ESR} = 0.02mW

The final loss comes from the power required to drive the PWM switcher itself (PL_{PWM}), which is 0.5 mW. Taking all these losses into consideration, the total power loss (PL_{TOT}) can be described by the following:

$PL_{TOT} = P_{RDS} + P_{QG} + P_{RL} + P_D + P_{ESR} + PL_{PWM}$

PL_{TOT}= (7.1 + 49 + 4.1 + 63 + 0.02 + 0.5)mW

PL_{TOT}= 124mW

After calculating the total power loss, the efficiency (η) of the circuit can be calculated:

$\eta = P_{out} / (P_{out} + PL_{TOT})$

η = 360mW / (360mW + 124mW)

η = 74.4%

The efficiency will be lower at low load currents because the 49 mW switching loss is independent of load.

Board Layout Considerations

The board layout must minimize the connection between the `VROUT[1:0]` pins and the gate pin of the FET. The trace resistance and inductance must be low enough to handle 1 MHz switching speeds and 200 mA of switching current. The traces to and from the FET's source and the V_{DDEXT} supply pin on the Blackfin processor should, if possible, be Kelvined to their power supply to avoid transient effects on other devices connected to the same supply. The connection paths to the FET's drain, the diode, inductor, and capacitors should be as short as possible and able to handle the load current.

The same is true for the ground connections, since they will carry the same load currents as the supply during the T_{off} time (the load current through the diode) and the gate switching current during T_{on}.

Lastly, locate the electrolytic capacitors at the FET source and the output side of the inductor. Add ceramic 0.1 or 0.01 µF capacitors in parallel to reduce the high frequency impedance.

References

[1] *Estimating Power for ADSP-BF533 Blackfin® Processors (EE-229).* Rev 1, February 2004. Analog Devices, Inc.

[2] *PM3316-100M Inductor Data Sheet.* J.W. Miller Magnetics.

[3] *FDS9431A P-Channel 2.5V Specified MOSFET Data Sheet*. September 1999. Fairchild Semiconductor.

[4] *ZHCS1000 Schottky Rectifier Diode Data Sheet.* Zetex Semiconductors.

Document History

Revision	Description
Rev 1 – February 2, 2005 *by Bob Libert, Brian Erisman, and Joe Beauchemin*	Initial Release