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Interfacing the ADSP-BF535 Blackfin® Processor to Single-CHIP CIF Digital Camera "OV6630" over the External Memory Bus

Contributed by Thorsten Lorenzen *April 17, 2003*

1 Introduction

The purpose of this note is to describe how to hook up video devices like a CIF (Common Interface Format) Single–Chip Digital Camera to the external bus of the ADSP-BF535 Blackfin® Processor. Because of its architecture and video processing capabilities, Blackfin Processors will interface with video devices. The ADSP-BF535 as the first part of the Blackfin family is not equipped with a standard interface that glueless interact with video devices. This note is dedicated to show how the Asynchronous Interface can be used to receive video in CIF sizes.

2 Output Format of the OV6630

The OV6630 is a CMOS Image sensor provided as a single chip video/imaging camera device designed to provide a high level functionality in a single, small-footprint package. For more details about the functionality it is referred to the internet address below. In order to explain the way been accessed by the ADSP-BF535 Processor see the schematic of the required output pins in figure 2.1. The datasheet for the OV6630 can be found at www.ovt.com

As it can be seen in figure 2.1 the pins Y[7:0] and UV[7:0] are required to transfer data. The PCLK represents the clock aligned to the data. Each raising edge of the PCLK will indicate valid data on the bus. These pins are necessary and must be linked to the ADSP-BF535 for data transfers. Additionally, some pins are required for device control and configuration purposes. The pin HREF asserted (polarity can be chosen) indicates active video pixels (image data).

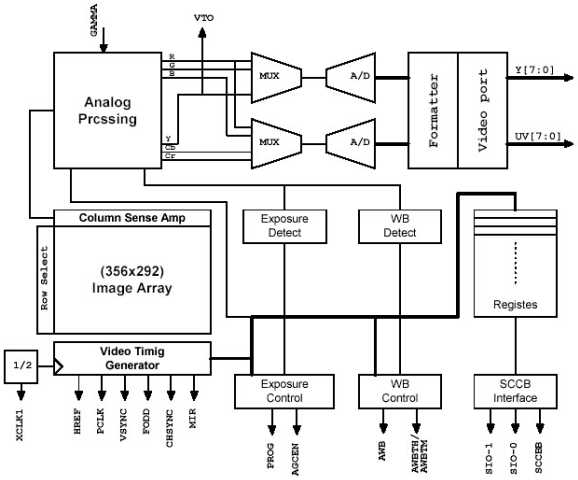

Figure 2.1

Because of the programmable sensor size as it is discussed below HREF provides a way to distinguish between active video pixels and blank data. The blank data of the modified senor field will also be transferred and is represented by hex “10” on Y[7:0] and hex “80” UV[7:0]. Figure 2.2 shows a transfer of one pixel, blanking and HREF indicating an active pixel. Due to the configuration the sensor is set to output over a 16 -bit bus in this note. One pixel exists of one byte of luminance and one byte of

chrominance information that can be transferred the same time.

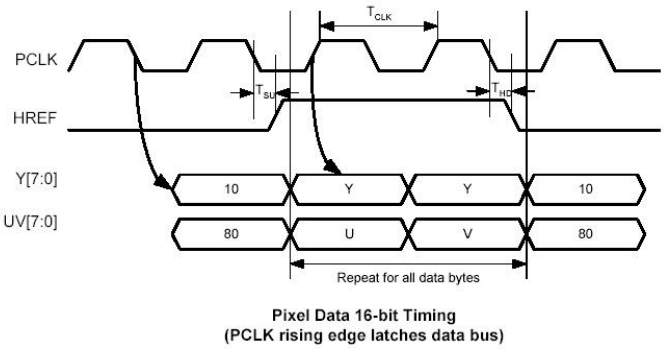

Figure 2.2

The windowing feature of the OV6630 image sensors allows user-definable window sizing as required by the application. Window size setting (in pixels) ranges from 2 x 2 to 356 x 292, and can be positioned anywhere inside the 356 x 292 boundary.

Note that modifying window size and/or position does not change frame or data rate. The OV6630 imager alters the assertion of the HREF signal to be consistent with the programmed horizontal and vertical region. The default output window is 352 x 288. Figure 2.3 shows it graphically.

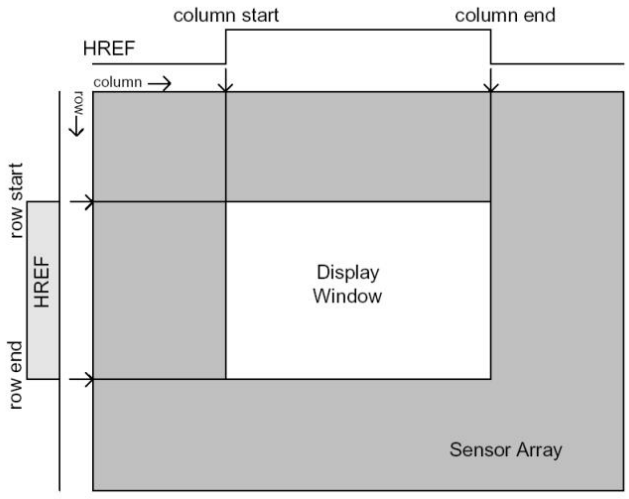

Figure 2.3

In order to detect the first line of each frame the signal VSYNC asserts before. Figure 2.4 shows the VSYNC pin on channel 1 and the HREF pin on channel 4. It can be seen if the sensor is set to transfer e.g. 200 lines the HREF will be asserted 200 times also. Each start of frame will be indicated by VSYNC around 2 ms before HREF asserts.

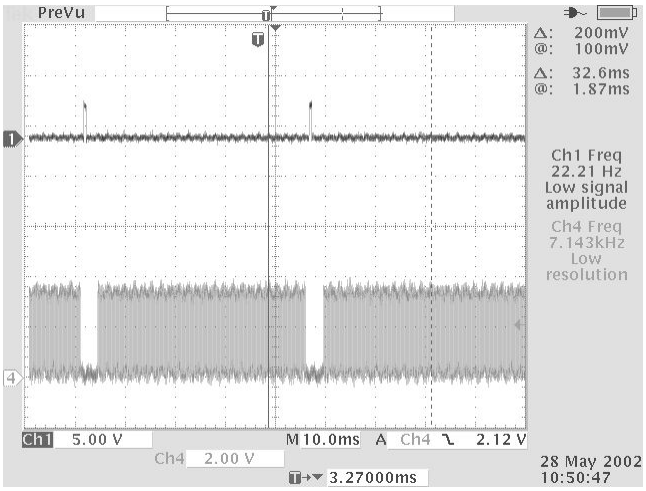

Figure 2.4

The video output port of the OV6630 image sensor provides a number of output format / standard options to suit many different application requirements. These formats are user programmable through Omnivision's SCCB two wire control interface.

The OV6630 imager supports both ITU-601 and ITU-656 output formats in different configurations.

In this note the sensor is set to provide differential video signals (YUV) 4:2:2, 16-bit wide and clocked at 8.867MHz (PCLK).

3 Asynchronize Interface of the ADSP-BF535 Blackfin Processor

The Processors asynchronous interface is used to receive the video data. 32-bit data can be fetched in a manner it is shown in figure 3.1.

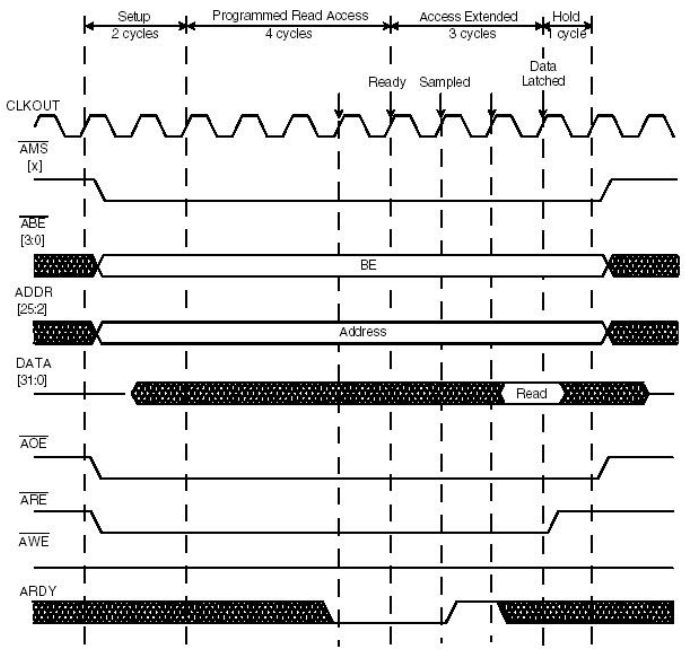

Figure 3.1

As mentioned in the ADSP-BF535 Blackfin Hardware Reference Manual after a read cycle is initiated the Async Memory Select line (/AMS) , Async Ouput Enable line (/AOE) and the Async Read Enable line (/ARE) become asserted. After a multicycle "Read Access" delay (Configured by the Async Interface Bank Control Register), the /ARE pin normally de-assert to complete the read operation. But if the interface is configured to extend the access, the /ARE pin remains low until the ARDY pin has been sampled high. The data will be fetched one cycle after this happened.

Due to the architecture of the ADSP-BF535, a DMA-controlled data download is somewhat non-intuitive. Each data transfer is split into bursts of eight read access. After the burst, a gap appears because of internal bus activity. Figure 3.2 illustrates this.

As shown in the figure, the first DMA is set up to read 32 data words (shown as Channel 2, the /ARE signal). The large gap before the next DMA is required for loading the next DMA descriptor.

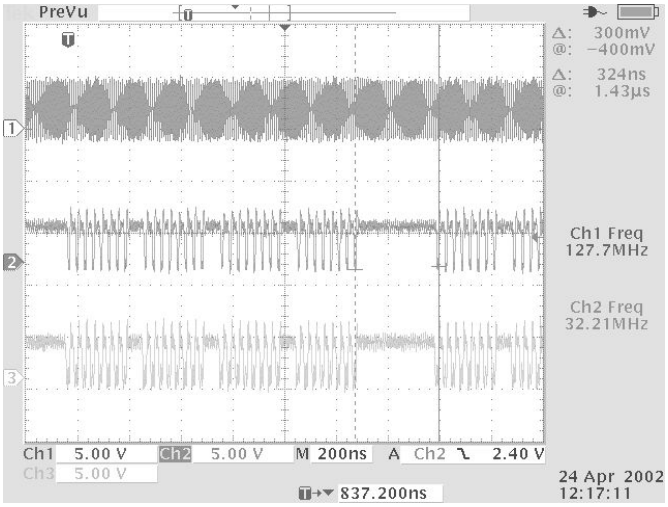

Figure 3.2

Note also that each DMA transfer is split into bursts of eight accesses (in this configuration, four bursts per DMA execution). Understanding this behavior is crucial for developing a proper DMA interface. Figure 3.3 zooms into one of these burst patterns to analyze how many cycles are taken for each access.

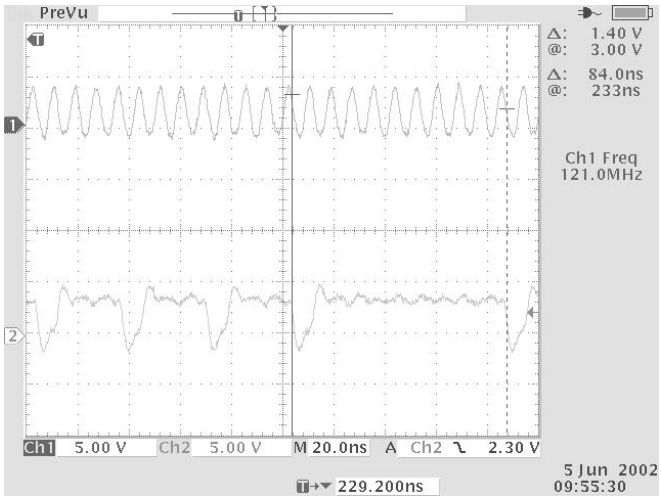

Figure 3.3

The peripheral clock "SCLK" is displayed in channel 1 and channel 2 shows the /ARE pin. After eight read strobes are done nine extra cycles are taken to place the data into internal memory.

4 Interface the ADSP-BF535 Processor into the OV6630

The ADSP-BF535 is configured to make full use of its 32-bit external memory interface, in order to gain maximum throughput. Two 16-bit words from the camera will be packed into one 32-bit word before being read by the Blackfin Processor.

To interface to the single-chip camera, LVT16374 latches are used. These parts are able to fetch the data received from the video device and latch it until the Asynchronous Interface has been read.

The 8.867 MHz PCLK of the OV6630 clocks a 74HC74 configured as a /2 divider. The 4.43 MHz output then clocks an LVT16374 to fetch the data transmitted by Y[7:0] and UV[7:0] at the rising edge. The data will be held in the LVT16374 until the next rising edge of the CLOCK “CK” appears.

When /OE asserts, the Processor reads the data latched by the LVT16374.

The ARDY pin is used to synchronize the video data with the ADSP-BF535. As long as the ARDY pin is low, the access is held off? This way, the camera is able to control the asynchronous memory interface.

By routing a GPIO pin to the PWDN pin of the OV6630, the sensor can be turned off without the lose of configurations done during setup time by the SCCB bus.

By routing a GPIO pin to the PWDN pin of the OV6630, the sensor can be turned off without the lose of configurations done during setup time by the SCCB bus.

5 Data Structure and Improvements

As mentioned in section 2, the camera sends active data plus blanking data sequentially. Blanking data does fill the internal memory but doesn’t contain any useful information.

The ADSP-BF535 provides 256kBytes of internal L2 Memory. One frame of CIF video contains 352 X 288 pixels. Each pixel can be represented in two bytes under the 4:2:2 digital component video representation. This equates to 202,752 bytes per frame. As shown in Figure 5.2, storing the blanking data as well would obviously cause the memory to overflow.

The use of the AND gate shown in Figure 4.1 stops the data transfer to avoid storing blanking data to the internal memory. The AND gate is controlled by the HREF signal of the camera. HREF remains high during active video transfers. The memory will be filled just with active video data.

To detect the first line of each frame, the VSYNC signal can be used as mentioned in section 2. VSYNC is connected to a programmable flag and generates an interrupt before the start of a frame. This interrupt will enable the DMA transfer.
Figure 5.1 shows how the timing requirements of the camera and the Processor are met.

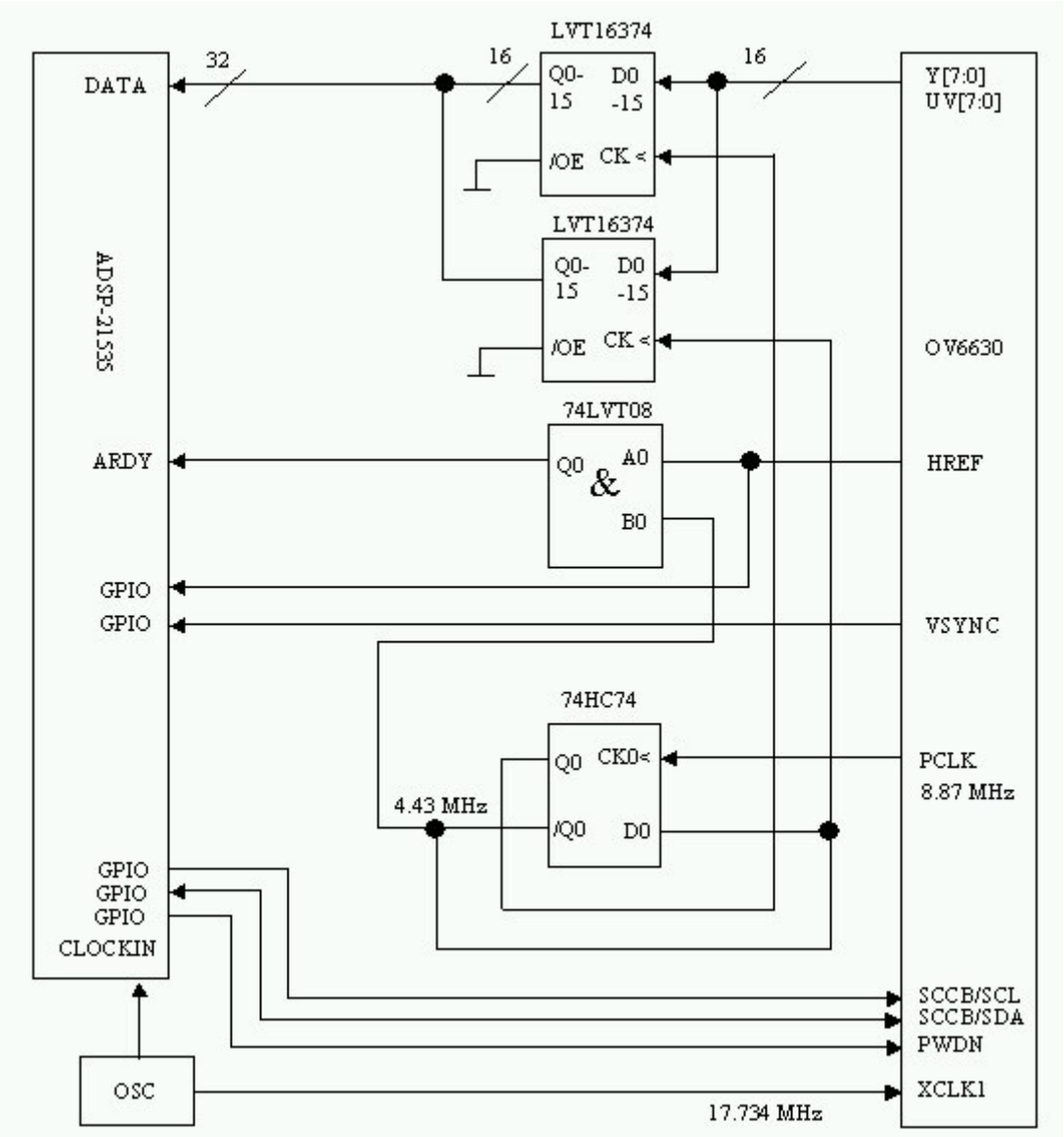
LVT16374
DATA
32
16
Q0-15
D0-15
/OE
CK
16
Y[7:0]
UV[7:0]
LVT16374
ADSP-21535
OV6630
74LVT08
ARDY
Q0
A0
&
B0
HREF
GPIO
GPIO
VSYNC
74HC74
Q0
CK0
PCLK
8.87 MHz
4.43 MHz
/Q0
D0
GPIO
GPIO
GPIO
CLOCKIN
SCCB/SCL
SCCB/SDA
PWDN
OSC
XCLK1
17.734 MHz

Figure 4.1

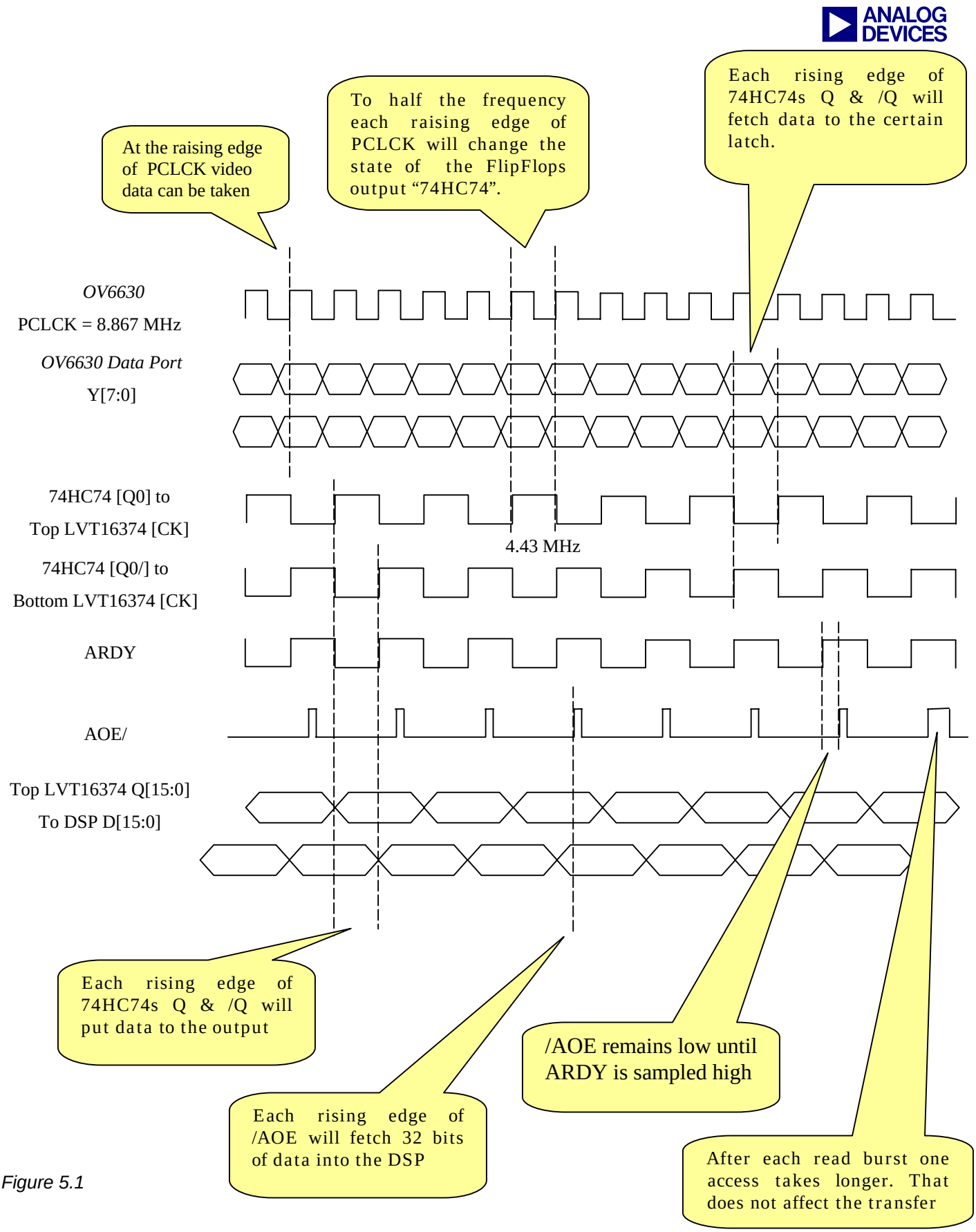
At the raising edge of PCLCK video data can be taken
To half the frequency each raising edge of PCLCK will change the state of the FlipFlops output “74HC74”.
Each rising edge of 74HC74s Q & /Q will fetch data to the certain latch.
OV6630
PCLCK = 8.867 MHz
OV6630 Data Port
Y[7:0]
74HC74 [Q0] to
Top LVT16374 [CK]
4.43 MHz
74HC74 [Q0/] to
Bottom LVT16374 [CK]
ARDY
AOE/
Top LVT16374 Q[15:0]
To DSP D[15:0]
Each rising edge of 74HC74s Q & /Q will put data to the output
/AOE remains low until ARDY is sampled high
Each rising edge of /AOE will fetch 32 bits of data into the DSP
After each read burst one access takes longer. That does not affect the transfer

Figure 5.1

BLACKFIN Memory [Hex32]

	DESTINATION1										
[F00002BC]	69ED77ED	6DE96FEC	7BE874E8	83E985EA	7FEF80EA	7BEE80EC	79EC8DEF	75EC8FEC	71EA78EC	73EE65EC	71EA66EE	75EF6CEC
[F00002EC]	71EE7BEE	7BED7FED	74EC7DEA	54EB81EC	55EF7FED	67EE71F0	70ED6DED	7BE97AEB	7BEC87EC	71F077ED	77F07BF0	7BEE81F0
[F000031C]	7DEA85ED	7CEA83EB	6FF085EB	61F07FF0	6DF07BF0	7CEC7CEE	80EE79EF	71EF78EF	71EE6DEE	73EF6CEE	65F07BEF	62EE8BF0
[F000034C]	60EA8BED	6FEE7FEE	77EE7DF0	74EB7CEC	69EE83EC	6DED86F0	65EC84EC	67EE7FEE	6CEB7DEA	6FF085EF	71ED7FEF	77EF7DF0
[F000037C]	7CEA7EED	73EC6FEA	65EB65ED	6CED61EC	7CEB6BF0	7DE967E7	7BED6BF0	73EA7BEB	73EC81EB	6FEC83ED	67EB78EC	6FEE69ED
[F00003AC]	79EE65EF	7BEC6FEE	73EE7BED	5BEE7CEF	53EF70EE	58EC65EE	63EB69EA	7AED7BEC	7CF07DEF	71F077F0	84ED6FED	83EE6CED
[F00003DC]	73F069EF	6BED78EE	71F083EE	77EB8BEF	80EB89EC	84EC83EC	7BEE7EED	63F078F0	53F070EE	67EE79EE	7BEC7DEF	75F080EE
[F000040C]	68EF84F0	5FED7FED	67ED80EE	6BEE87EF	67E983EC	77EC7BEC	83ED6CEC	7BEE63ED	75EB70ED	83E875EC	88EC72E8	74EE6DEC
[F000043C]	69EE76EE	77ED7EED	7CEC86F0	7EEE8CED	69F081EE	56F079F0	51EE7BF0	53EC79EE	59ED6EEB	61F073F0	62EE7BF0	80EE7EED
[F000046C]	7FEE75EE	62F073EF	60EE7EF0	75EC80EC	7FEE70EF	7DED68EE	77ED69EE	73EC63EC	77F05FED	7FEE63F0	85EE65ED	83F06CEF
[F000049C]	88F071F0	86F06FF0	87EF73F0	8AEF75EE	8BEF7BF0	93F07DF0	85F07FF0	87F07CF0	8FF077F0	8CED75ED	8BF073F0	93EF76F0
[F00004CC]	9DF073EE	801078F0	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010
[F00004FC]	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010
[F000052C]	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010
[F000055C]	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010
[F000058C]	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010
[F00005BC]	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010
[F00005EC]	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010
[F000061C]	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010
[F000064C]	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010
[F000067C]	73E98010	75EE75EB	7BEA77F0	7DED6FEA	71EC6BEF	76ED6DED	84ED70EA	82ED74ED	7BEC78EF	80EC83EB	73EC8AED	61EA86EB
[F00006AC]	69EA7FEC	6BEC79E8	71EC7FF0	81EC83ED	80E979E9	8BEB75EA	74EB7DEB	61EE83EC	75ED7FF0	87EC76EC	83EE6FEC	71EC75EE
[F00006DC]	57EF73ED	56ED7FF0	6EEE7BEE	74EE6CEE	64EF6EEE	65EE80F0	6BEE86EF	6BEC84EC	5DEC7DEC	71ED7FEF	87EE8BED	83ED89EE
[F000070C]	6BEF76ED	63ED75F0	6EEE74ED	6FEE79EE	71EF7CEF	75ED83EF	7AED85EF	81EF7FEB	8BEC75EF	91E774E7	8AEB87EA	76F088EB
[F000073C]	63EC81EE	67ED8DEF	78EC8BEE	84EC7FEC	7EEE6BEB	7FEE69F0	75EF69EE	76EE76F0	77EE73ED	73EE6CED	69EF77F0	67EE7DEF
[F000076C]	6CEC77ED	7BEE75EE	81EB7BEC	77EE78EE	6FEE6CEE	6EF06DEF	75F079F0	7FED7BEE	84F07AEF	81F07BF0	75EE7BEE	61EE78EF
[F000079C]	56EC79ED	60EF79EE	67F077F0	6EEE6FEE	64EC73ED	53EF7FED	5CF08BF0	64EC8BF0	74F076ED	67EE73F0	67F075EE	70EF7BF0
[F00007CC]	74EA83EB	6EEE86EE	73EE81ED	76EC87F0	7EEE88EE	85ED7DEE	6FEE7BEE	5BED78EE	5BEC69EC	73EE67F0	7BEC66EC	85EB72ED
[F00007FC]	93EC70EB	8CE970EA	6DEA79E8	5FEC7DED	6DEC7FEC	74ED77EC	70EC6FED	7AEC6FEC	7BEE75ED	6FF074F0	52ED71F0	57F06BEE
[F000082C]	63EC67EE	63E86AEA	6BEB75E9	6BEF7BEE	6EEB7CEF	7CEA74EB	76ED6DEC	66EE71EE	6EEE84F0	80F08CEE	85EC89EE	7DEA7FEA
[F000085C]	7BEC7BEE	6BED75EB	5BF073EE	5DF06FF0	77EC76F0	85EE89EE	79EE8FEC	63EE8FF0	62EE85ED	68EC80EC	63ED87ED	65EB84EE
[F000088C]	6FEA75EA	74EC6CED	7AEE6CEE	74EC71EE	7BE875EC	7DEA70E9	77EE70EB	61EC7FEE	69ED84EC	6FEC85EF	67ED83ED	65F081EF
[F00008BC]	65EE80F0	64EE7FEE	69EE7BF0	6BED6DEC	63EE71EE	61EC83ED	69EB86EB	5DEF78ED	5FF074F0	63EE78F0	6FED80EE	73EE76EE
[F00008EC]	73EB6FEC	84EE6DED	8BED64EE	83EF5DED	78EB66EE	75ED66EA	6DF064F0	77EE70EF	83F079F0	84EE76EE	86F077F0	89F073F0
[F000091C]	85F06EF0	84F075F0	87F07FF0	80EF73F0	7EEE67EE	7CF064F0	7DEE6BF0	9CF077EF	801081F0	80108010	80108010	80108010
[F000094C]	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010
[F000097C]	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010
[F00009AC]	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010
[F00009DC]	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010
[F0000A0C]	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010
[F0000A3C]	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010
[F0000A6C]	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010
[F0000A9C]	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010	80108010
[F0000ACC]	80108010	80108010	80108010	80108010	80108010	80108010	80108010	6BEA8010	71EE83F0	73EE80EF	7FEC85EB	7BEA8EED
[F0000AFC]	77EC86EA	87EB8CEE	89EC88EA	84EE83ED	7CEC87EE	75EB82EA	65EC7FEB	5DEC85EC	63ED8BEC	7CEC87F0	8DEA84EC	89EA78E9
[F0000B2C]	7CEC7DEC	6FEC83EC	6DEE7FEC	6DEE7BEE	81ED80EC	7DED95EE	64ED8EEC	53ED7BEF	61F06DED	77EA7DF0	7DEA7FE8	6CEE78EB

Figure 5.2

Conclusion:

The goal of this project is to show how video sources can be connected to the ADSP-BF535 with less glue logic as possible. In fact, the maximum resolution that can be achieved is video in formats up to CIF (352 x 288). The actual resolution is limited due to the limitation of Blackfins external port timing, the DMA structure and the internal memory.

The external port halts during the I/O processor loads the next DMA descriptor when it has been expired. That causes a large gap in the timing (mentioned in chapter 3) and would not meet the requirement set by the camera. A way out of this problem is to set up the DMA downloading each frame separately. So a DMA expires after receiving each frame and will be reloaded during the camera send blank data anyway (The camera sends blank data between each line and each frame).

The DMA Word Count Register is limited to the maximum of 65,536 (2^16). A frame of CIF format video in 4:2:2 standard is represented by 202,752 bytes (352*288 pixels * 2 bytes) . The Processor accesses over a 32-bit interface results in 50,688 words (202,752bytes /4 (bytes/word)). That fits in the DMAs Word Count Register. Resolutions higher than CIF could probably not be served by the DMA on a frame by frame basis. That causes the DMA to become reloaded during active video pixel transfers and results in data misses.

Building an interface like it is done in this note the access to SDRAM or SRAM is not supported anymore. Except the use of the PCI, SPORT, SPI and USB data can just be stored in L1 or L2 memory. The ADSP-BF535 provides 52k of L1 memory and 256k bytes of L2 memory. L2 memory is be able to keep one frame of video in CIF consisting of 202,752 bytes. Higher resolutions does not fit in it.

A picture of the system is shown in figure C1.

Video transfers with higher resolutions than CIF it is revered to the Note:

"Interfacing the ADSP-BF535 to ADV7185/3 NTSC/PAL video decoder over the External Memory Bus".

This Note is available soon.

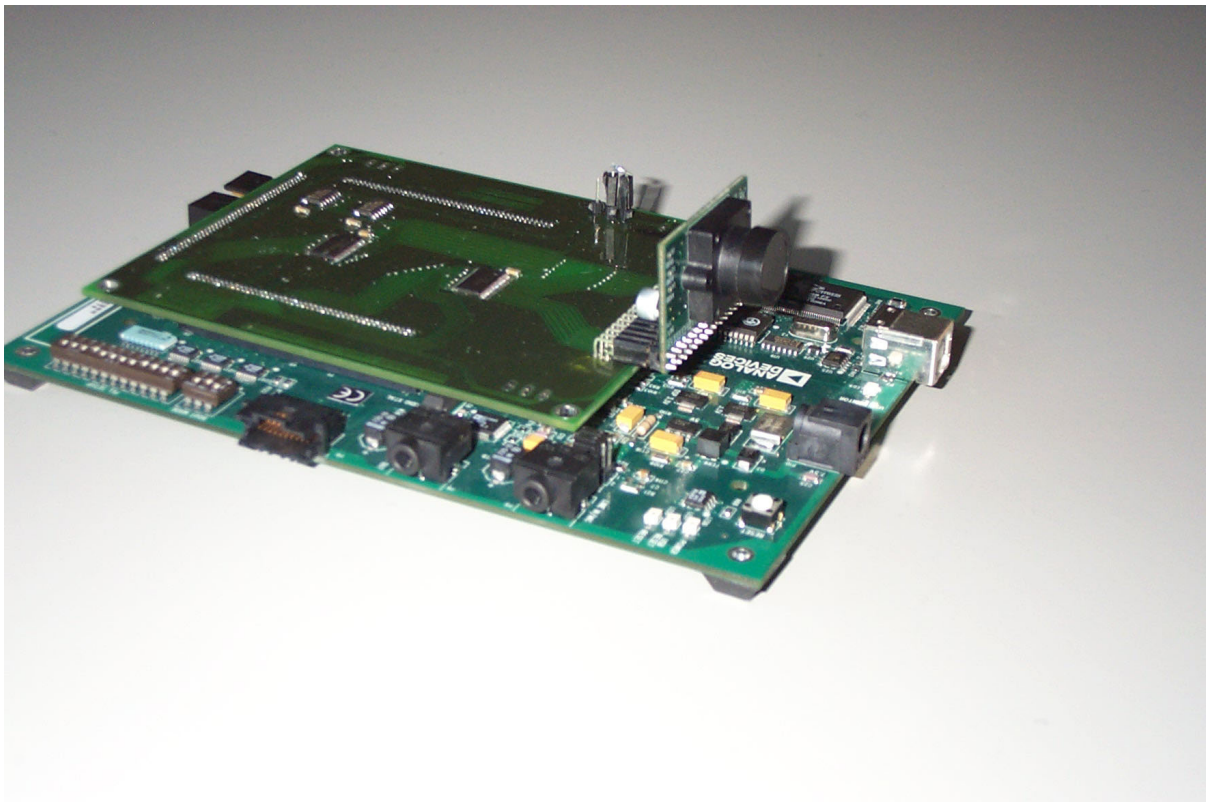

Figure C1

References:

-www.ovt.com

-OV6630 Datasheet

-OV7610MD Eva Board

-ADSP-BF535 Datasheet

-ADSP-BF535 Blackfin DSP Hardware Reference

-VisualDSP++™ 3.0

Document History

Version	Description
April 17, 2003	Ported code example to VisualDSP++ 3.1 Changed according to new Blackfin naming convention.
January 23, 2003	Typos. Schematics, Gerber files and PDFs are attached to the web site
January 09, 2003	Initial release
August 06, 2002	Rev. 0.2