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Estimating Power for ADSP-BF561 Blackfin® Processors

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Introduction

This EE-Note discusses the methodology for estimating total average power consumption of ADSP-BF561 Blackfin® embedded symmetric multiprocessors. Power estimates are based on characterization data measured over power supply voltage, core frequency (CCLK), and junction temperature (T_J). The intent of this document is to assist board designers in estimating their power budget for power supply design and thermal relief designs using Blackfin dual-core processors. These processors feature dynamic power management control, allowing the regulation of applied core voltage (V_{DDINT}) from an external I/O source (V_{DDEXT}). The ranges for these supplies differ depending on the part being used.

The total power consumption of the ADSP-BF561 Blackfin processor is the sum of the power consumed for both of the power supply domains, V_{DDINT} and V_{DDEXT}.

Please consult the following sections of the *ADSP-BF561 Blackfin Embedded Symmetric Multiprocessor Data Sheet*[1] for details specific to discussions throughout this EE-Note:

- See the *Recommended Operating Conditions* section for details regarding V_{DDINT} and V_{DDEXT} ranges.
- See the *Timing Specifications* section for details regarding required V_{DDINT} values to support the desired CCLK.
- See the *Ordering Guide* section for a comprehensive list of the various speed and temperature grade models available for ADSP-BF561 Blackfin processors.

Estimating Internal Power Consumption

The total power consumption due to internal circuitry (on the V_{DDINT} supply) is the sum of the static power component and dynamic power component of the processor's core logic. The dynamic portion of the internal power depends on the instruction execution sequence, the data operands involved, and the instruction rate. The static portion of the internal power is a function of temperature and voltage; it is not related to processor activity.

Analog Devices provides current consumption figures and scaling factors for discrete dynamic activity levels. System application code can be mapped to these discrete numbers to estimate the dynamic portion of the internal power consumption for ADSP-BF561 Blackfin processors in a given application.

Internal Power Vector Definitions

The following power vector definitions define the dynamic activity level placed on both cores, which applies to the internal power vectors shown in Table 1.

- $I_{DD-IDLE}$ - V_{DDINT} supply current for idle activity. Idle activity is each core executing the `IDLE` instruction only, with no core memory accesses, no DMA, and no interrupts.
- I_{DD-NOP} - V_{DDINT} supply current for no-op activity. No-op activity is each core executing the `NOP` instruction only, with no core memory accesses, no DMA, and no interrupts. This is a useful measurement for software-implemented delay loops.
- I_{DD-APP} - V_{DDINT} supply current for a specific application's activity. This activity is each core executing an application comprised of 30% dual-MAC instructions and 70% load-store and no-op instructions. All instructions and data are located in L1 SRAM, and peripherals are not enabled.
- I_{DD-TYP} - V_{DDINT} supply current for typical activity. Typical activity is each core executing an application comprised of 75% dual-MAC instructions and 25% dual-ALU instructions. All instructions and data are located in L1 SRAM, and peripherals are not enabled. This is the test vector used for the dissipation numbers found in the data-sheet.
- $I_{DD-HIGH}$ - V_{DDINT} supply current for high activity. High activity is each core executing an application comprised entirely of dual-MAC instructions. All instructions and data are located in L1 SRAM, and peripherals are disabled.
- $I_{DD-PEAK}$ - V_{DDINT} supply current for peak activity. Peak activity is each core executing 100% dual-MAC instructions fetched from internal memory, with memory DMA moving a data pattern from L1 Data A memory to L1 Data B memory. The bit pattern toggles all bits in each access.

The test code used to measure $I_{DD-PEAK}$ represents worst-case processor operation. This activity level is not sustainable under normal application conditions.

Estimating I_{DDINT} Dynamic Current, I_{DD-DYN}

There are two steps required to estimate dynamic power consumption due to internal circuitry (i.e., on the V_{DDINT} supply). The first step is to determine the dynamic baseline current, and the second step is to determine the percentage of activity for each discrete power vector with respect to the entire application.

I_{DD} Baseline Dynamic Current, $I_{DD-BASELINE-DYN}$

The ADSP-BF561 Blackfin processors' baseline dynamic current ($I_{DD-BASELINE-DYN}$) graph is shown in Figure 1. The value of $I_{DD-BASELINE-DYN}$ is derived using the I_{DD-TYP} dynamic activity level vs. core frequency. Each curve in the graph represents a baseline I_{DDINT} dynamic current for a specified power supply setting. Using the curve specific to the application, $I_{DD-BASELINE-DYN}$ for the V_{DDINT} power supply domain can be estimated at the `CCLK` of the processor's cores in the application. For example, with V_{DDINT} at 1.2 V and both cores operating with `CCLK` at 400 MHz, the corresponding $I_{DD-BASELINE-DYN}$ for the V_{DDINT} power supply domain would be approximately 340 mA.

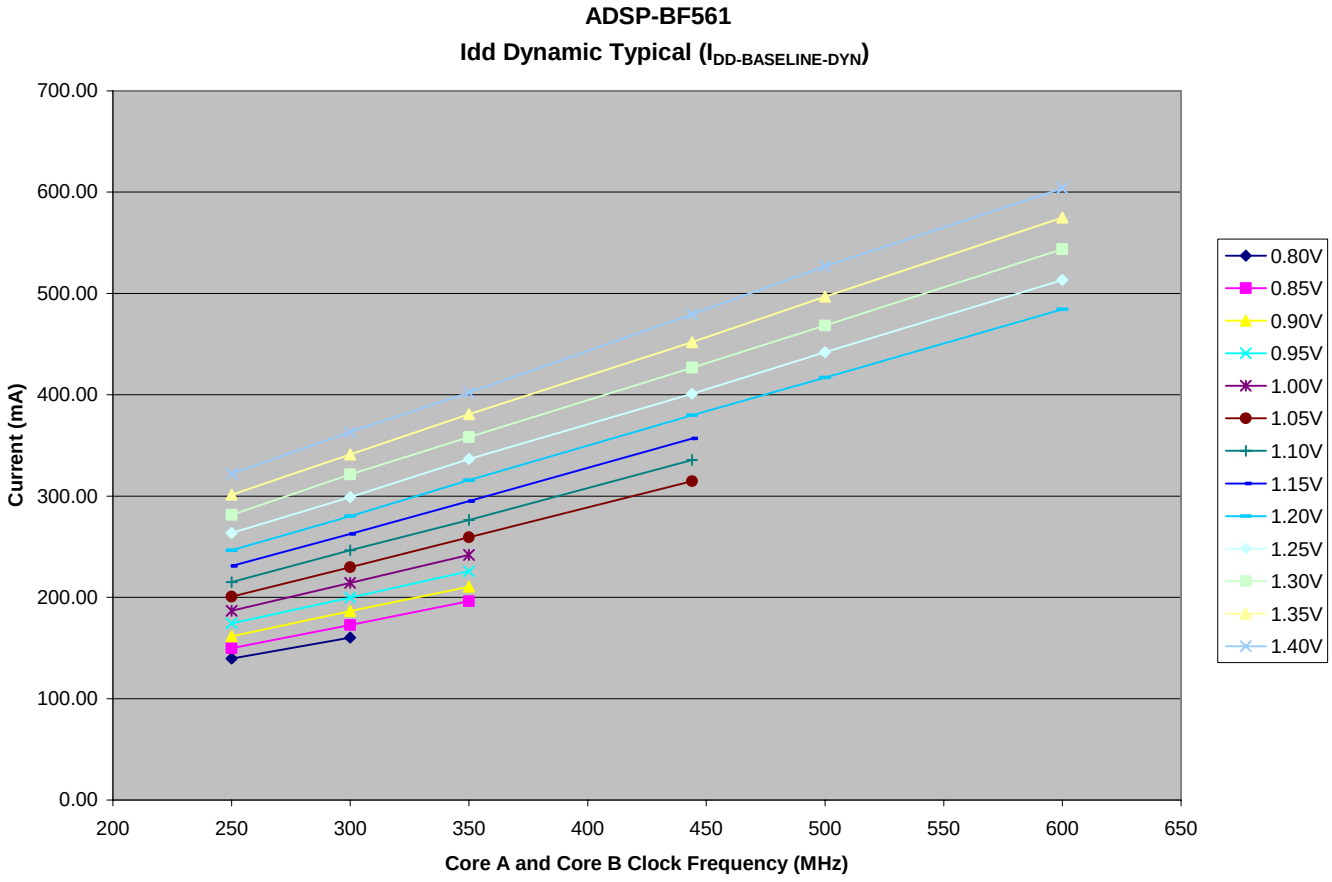

Figure 1. Baseline I_{DDINT} Dynamic Current

I_{DD} Dynamic Current Running Your Application

Table 1 lists the scaling factors for each activity level, which are used to estimate the dynamic current for each specific application. With knowledge of the program flow and an estimate of the percentage of time spent at each activity level, system developers can use the $I_{DD-BASELINE-DYN}$ shown in Figure 1 and the corresponding activity scaling factors (ASF) from Table 1 to determine the dynamic portion of the internal current (I_{DD-DYN}) for each ADSP-BF561 Blackfin processor in a system.

Power Vector	Activity Scaling Factor (ASF)
$I_{DD-PEAK}$	1.27
$I_{DD-HIGH}$	1.21
I_{DD-TYP}	1.00
I_{DD-APP}	0.92
I_{DD-NOP}	0.83
$I_{DD-IDLE}$	0.41

Table 1. Internal Power Vectors and Dynamic Scaling Factors

I_{DD-DYN} for an ADSP-BF561 Blackfin processor in a specific application is calculated according to Equation 1, where "%" is the percentage of the overall time that the application spends in that state:

$$\begin{aligned}&(\%\ \textit{Peak activity level}\ \mathbf{x}\ I_{DD\text{-}PEAK}\ \textit{ASF}\ \mathbf{x}\ I_{DD\text{-}BASELINE\text{-}DYN})\\&(\%\ \textit{High activity level}\ \mathbf{x}\ I_{DD\text{-}HIGH}\ \textit{ASF}\ \mathbf{x}\ I_{DD\text{-}BASELINE\text{-}DYN})\\&(\%\ \textit{Typ. activity level}\ \mathbf{x}\ I_{DD\text{-}TYP}\ \textit{ASF}\ \mathbf{x}\ I_{DD\text{-}BASELINE\text{-}DYN})\\&(\%\ \textit{App. activity level}\ \mathbf{x}\ I_{DD\text{-}APP}\ \textit{ASF}\ \mathbf{x}\ I_{DD\text{-}BASELINE\text{-}DYN})\\&(\%\ \textit{NOP activity level}\ \mathbf{x}\ I_{DD\text{-}NOP}\ \textit{ASF}\ \mathbf{x}\ I_{DD\text{-}BASELINE\text{-}DYN})\\+\ &(\%\ \textit{Idle activity level}\ \mathbf{x}\ I_{DD\text{-}IDLE}\ \textit{ASF}\ \mathbf{x}\ I_{DD\text{-}BASELINE\text{-}DYN})\\&\overline{\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad}\\&\textit{Total Dynamic Current for } V_{DDINT}\ (I_{DD\text{-}DYN})\end{aligned}$$

Equation 1. Internal Dynamic Current (I_{DD-DYN})

For example, after profiling the application code for a particular system, activity is determined to be proportioned as shown in Figure 2.

$$\begin{aligned}&\textit{(10\% Peak Activity Level)}\\&\textit{(20\% High Activity Level)}\\&\textit{(50\% Typ. Activity Level)}\\&\textit{(10\% App. Activity Level)}\\&\textit{(10\% NOP Activity Level)}\\+\ &\textit{(0\% Idle Activity Level)}\\&\overline{\qquad\qquad\qquad\qquad\qquad\qquad}\\&\textit{100\% Activity}\end{aligned}$$

Figure 2. Internal System Activity Levels

Using the ASF provided for each activity level in Table 1 (and with V_{DDINT} at 1.2 V and CCLK at 400 MHz), a value for I_{DD-DYN} consumption of a single dual-core processor can be estimated as follows:

$$\begin{aligned}&\textit{(10\% x } \mathbf{1.27} \textit{ x 340)}\\&\textit{(20\% x } \mathbf{1.21} \textit{ x 340)}\\&\textit{(50\% x } \mathbf{1.00} \textit{ x 340)}\\&\textit{(10\% x } \mathbf{0.92} \textit{ x 340)}\\&\textit{(10\% x } \mathbf{0.83} \textit{ x 340)}\\+\quad &\textit{(0\% x } \mathbf{0.41} \textit{ x 340)}\\&\overline{\qquad\qquad\qquad\qquad\qquad\qquad}\\&I_{DD\text{-}DYN} = 354.96\ mA = {\sim}355\ mA\end{aligned}$$

Figure 3. Internal Dynamic Current Estimation

The total estimated dynamic current on the V_{DDINT} power supply in this example is ~355 mA.

Estimating I_{DDINT} Static Current, $I_{DD-DEEPSLEEP}$

Deep Sleep mode for ADSP-BF561 Blackfin processors is when power is applied to both cores and L1 memories, but all clocks are turned off. In this mode, the $I_{DD-DEEPSLEEP}$ measurement can be taken, which is the baseline static component of overall average dissipation. The $I_{DD-DEEPSLEEP}$ current graphs for the ADSP-BF561 Blackfin processor are shown in Figure 4. The static current on the V_{DDINT} power supply domain is a function of junction temperature (T_J) and voltage, but it is ***not*** a function of frequency or activity level.

Therefore, unlike the dynamic portion of the internal current, the static current need not be calculated for each discrete activity level or power vector. Using the static current curve corresponding to the application (i.e., at specific V_{DDINT}), $I_{DD-DEEPSLEEP}$ can be estimated vs. T_J of the ADSP-BF561 Blackfin processor.

Appendix A discusses the methodology for estimating T_J. This process involves knowing the total power profile for the processor; therefore, this process will be iterative to arrive at a final calculation for expected power dissipation.

For example, in an application with V_{DDINT} at 1.2 V and an ADSP-BF561 Blackfin processor at a T_J of +100°C, the corresponding $I_{DD-DEEPSLEEP}$ for the V_{DDINT} power domain would be approximately 430 mA.

The static power of the ADSP-BF561 Blackfin processor is constant for a given voltage and temperature. Therefore, it is simply added to the total estimated dynamic current when calculating the total power consumption due to the internal circuitry of the processor. Note that the $I_{DD-DEEPSLEEP}$ currents shown in Figure 4 represent the worse-case static current as measured across the wafer fabrication process.

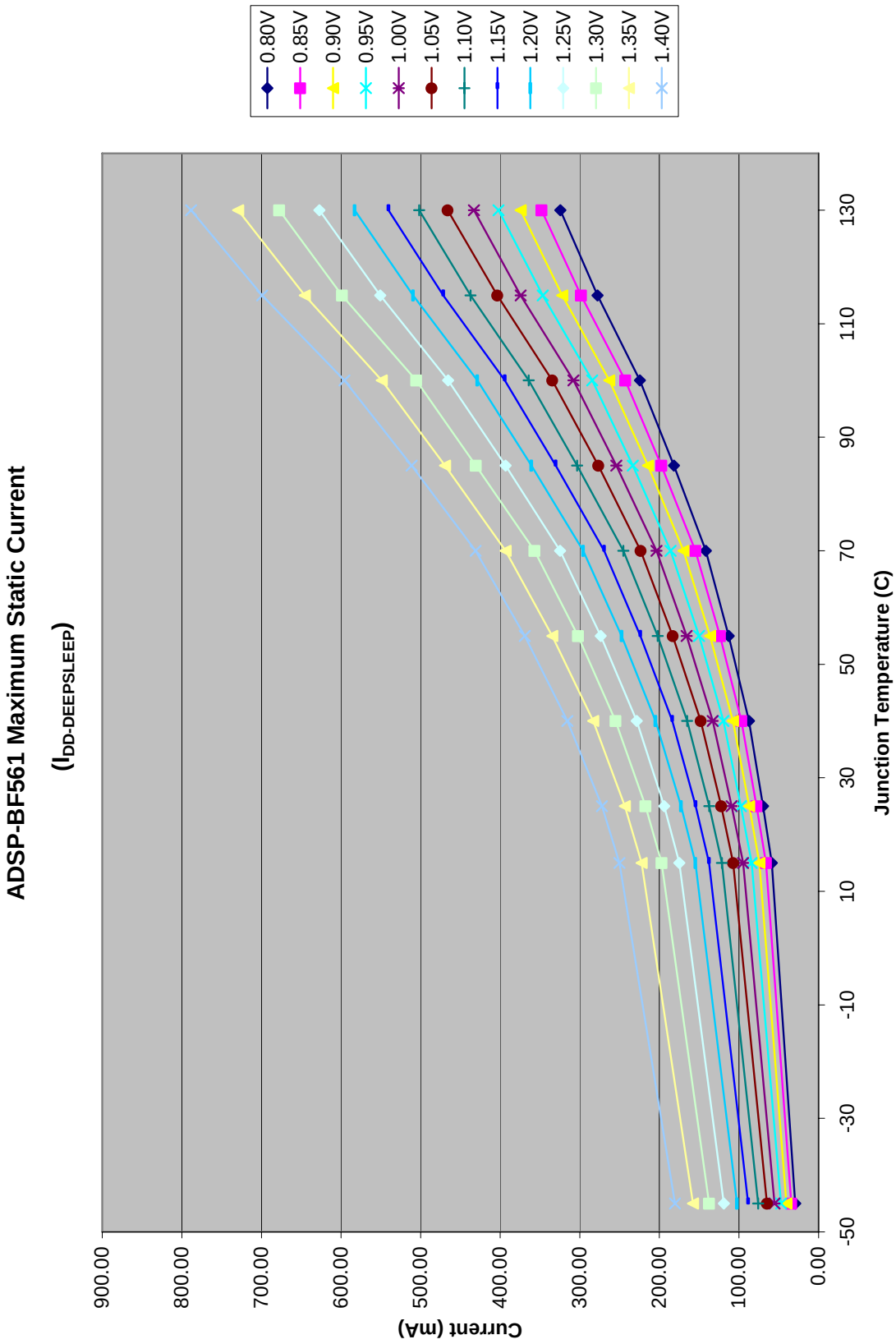

Figure 4. $I_{DD\_DEEPSLEEP}$ Static Current

Estimating Total I_{DDINT} Current

The total current consumption due to the internal cores' circuitry (I_{DDINT}) is the sum of the dynamic current component and the static current component, as shown in Equation 2.

$$I_{DDINT} = I_{DD\text{-}DYN} + I_{DD\text{-}DEEPSLEEP}$$

Equation 2. Internal Cores' Current (I_{DDINT}) Calculation

Continuing with the example of the ADSP-BF561 Blackfin processor operating at 1.2 V and 400 MHz (and with the code as profiled), assume that the resulting T_J is estimated to be +100°C. The total internal current consumed by the processor's cores under these conditions would be:

$$I_{DDINT} = 355 + 430 = 785\ mA$$

Equation 3. I_{DDINT} Estimation

Total Estimated Internal Power, P_{DDINT}

The resulting internal power consumption (P_{DDINT}) is given by Equation 4.

$$P_{DDINT} = V_{DDINT}\ x\ I_{DDINT}$$

Equation 4. Internal Power (P_{DDINT}) Calculation

Using Equation 4, the total estimated internal power consumed by the ADSP-BF561 processor in the application described in this example would be:

$$P_{DDINT} = 1.20V\ x\ 785\ mA = 942\ mW$$

Equation 5. P_{DDINT} Estimation

Estimating External Power Consumption

External power consumption (on the V_{DDEXT} supply) is dependent on the enabled peripherals in a given system. Each unique group of peripheral pins contributes to a piece of the overall external power, based upon several parameters:

- *O* - The number of output pins that switch during each cycle
- *f* - The maximum frequency at which the output pins can switch
- V_{DDEXT} - The voltage swing of the output pins
- C_L - The load capacitance of the output pins
- *U* - The utilization factor (the percentage of time that the peripheral is on and running)

In addition to the input capacitance of each device connected to an output, the total capacitance (C_L) should include the capacitance of the processor pin itself (C_{OUT}), which is driving the load.

Equation 6 shows how to calculate the average external current (I_{DDEXT}) using the above parameters:

$$I_{DDEXT} = O \ x \ f/2 \ x \ V_{DDEXT} \ x \ C_L \ x \ U$$

Equation 6. External Current (I_{DDEXT}) Calculation

The worst-case external pin power scenario occurs when the load capacitor charges and discharges continuously, requiring the pin to toggle each cycle. Since the state of the pin can change only once per cycle, the maximum toggling frequency is `f/2`. In terms of supply power, the worst-case V_{DDEXT} value is 3.6 V. Table 2 contains data for a realistic example of a PPI application, which runs several peripherals simultaneously. Actual results may vary, but again, the intent of this document is to help designers size the power supplies.

Estimated average external power consumption (P_{DDEXT}) can be calculated as follows.

$$P_{DDEXT} = V_{DDEXT} \ x \ I_{DDEXT}$$

Equation 7. External Power (P_{DDEXT}) Calculation

Using the sample Blackfin system configuration in Figure 5, the external current and, therefore, the external power consumption can be estimated.

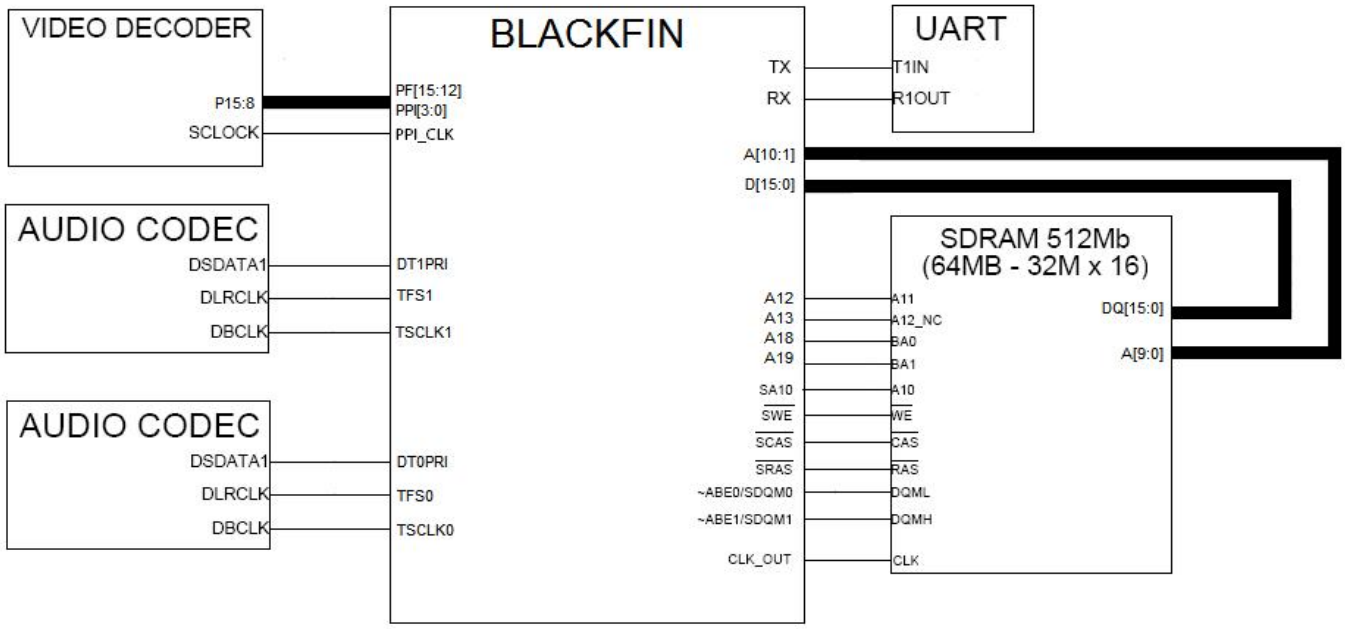

Figure 5. Blackfin System Sample Configuration

I_{DDEXT} (Equation 6) can be calculated for each class of pins that can drive, as shown in Table 2.

Peripheral	Freq (Hz)	# of pins	C/pin (F)	Toggle Ratio	Util	Vddext (V)	Pout @ 3.6V (mW)
PPI	27.00E+06	9	30.00E-12	1	1.00	3.6	47.24
SPORT0	4.00E+06	2	30.00E-12	1	1.00	3.6	1.56
SPORT1	4.00E+06	2	30.00E-12	1	1.00	3.6	1.56
UART	115.00E+03	2	30.00E-12	1	0.25	3.6	0.01
SDRAM	133.33E+06	36	30.00E-12	0.25	0.50	3.6	116.35
Total External Power Dissipation @ 3.6 V (est. mW)							166.71

Table 2. Sample Calculation for Total Average External Power

In the above example, the total average external power consumption is estimated to be ~165 mW. This number was obtained with the parameters listed in Table 2 by applying Equation 8. The chosen operating frequencies are reasonable for each of the peripherals, including the maximum allowed SDRAM frequency of 133.33 MHz. This model assumes that each output pin changes state every clock cycle, which is a worst-case model, except in the case of the SDRAM (because the number of output pins transitioning each clock cycle will be less than the maximum number of output pins). Table 2 was taken from the *External Power Spreadsheet*[2], which is associated with this EE-Note. It contains calculations for four sample systems. The reader can tailor this spreadsheet to the application, adding or deleting rows as necessary. Since the equation provides results in Watts (W), an additional multiplier of 1000 in the spreadsheet converts results into mW.

This equation is a more theoretically accurate version of the one used in the spreadsheet:

$$\overline{P}_{ext} = V_{DDext}{}^{2} \cdot \sum_{All-Output-Pins} C_L \cdot \overline{f}$$

Equation 8. Alternate External Power (P_{DDEXT}) Calculation

Rather than estimating average external power dissipated in each *peripheral*, the estimate applies to each *individual output pin*, based on the pin's load capacitance and average toggling frequency. The voltage swing is uniform across all output pins within the V_{DDEXT} supply domain, so it is multiplied by the summation of the dynamic charge changes on each output.

Using the PPI data in Table 2, nine output pins change every cycle at an average frequency of 27 MHz. Since toggling between on-to-off and off-to-on requires two cycles, F_{AVG} (13.5 MHz) is half the PPI clock. Since each pin changes at the same rate and the pin capacitance is presumed to be the same, the summation is simply nine times the value of any one PPI pin. Applying Equation 8:

$$\begin{aligned} P_{EXT\_AVG} &= V_{DDEXT}{}^{2} * 9\ pins * (F_{AVG} * C_L) \\ &= (3.6)^2 * 9 * 13.5e6 * 30e\text{-}12 \\ &= 12.96 * 0.003645 \\ &= 0.0472392W \\ &= 47.239mW \end{aligned}$$

As can be seen, the value derived using this equation is the same as the value estimated in Table 2. This model obtains the same estimate on a per-pin basis rather than a per-peripheral basis.

In addition to the peripheral pins, there is one other output pin on ADSP-BF561 Blackfin processors that will contribute to the V_{DDEXT} supply domain power profile if the system uses a crystal to provide the CLKIN signal to the processor. In this case, the processor drives the XTAL output pin when the PLL is active. The output drive frequency will be exactly the CLKIN rate, and the pin capacitance value can be obtained from the appropriate data-sheet. Note that the voltage swing will likely be less than V_{DDEXT} for most crystals, and using V_{DDEXT} in computations would be a worst-case model in terms of profiling power dissipation.

Finally, designers must be mindful of power supply efficiency when sizing the V_{DDEXT} supply. *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228)*[3] describes the internal voltage regulator and the associated external circuitry.

Total Power Consumption

For a given system, total power consumption is the sum of its individual components - power consumed by internal circuitry, power consumed due to switching I/O pins, and power consumed by the RTC circuitry, as follows:

$$P_{TOTAL} = P_{DDINT} + P_{DDEXT}$$

Equation 9. Total Power (P_{TOTAL}) Calculation

Where :

P_{DDINT} = Internal power consumption as defined by Equation 4

P_{DDEXT} = External power consumption as defined by Equation 7

For example, assuming that the processor in Figure 5 is operating under the conditions detailed in the example (the processor operating at 1.2 V, 400 MHz, and code as profiled in Figure 2), and also assuming that the resulting T_J has been estimated to be +100°C (see Appendix A for estimating T_J), the total estimated power consumed for the ADSP-BF561 processor would be:

$$P_{TOTAL} = 942\ mW + 166.71\ mW = \sim 1.11\ W$$

Figure 6. Total Power (P_{TOTAL}) Calculation for Sample in Figure 5 While Running Code Described in Equation 5

Conclusion

Several variables affect the power requirements of an embedded system. Measurements published in the ADSP-BF561 Blackfin processor data sheet are indicative of typical parts running under typical conditions. However, these numbers do not reflect the actual numbers that may occur for a given processor under non-typical conditions. In addition to the type of silicon that the customer could have, the ambient temperature, core and system frequencies, supply voltages, pin capacitances, power modes, application code, and peripheral utilization contribute to the average total power that may be dissipated.

The average power estimates obtained from methods described in this EE-Note indicate how much the ADSP-BF561 Blackfin processor loads a power source over time. These estimates are useful in terms of expected power dissipation within a system, but designs must support worst-case conditions under which the application can be run. Do not use this calculation to size the power supply, as the power supply must support peak requirements.

Appendix A

For ADSP-BF561 Blackfin processors, the total power budget is limited by the maximum allowed junction temperature (T_J) of the device. Please see the processor data sheet for the maximum T_J specification.

To guarantee correct operation, ensure that T_J does not exceed the maximum T_J specification. Use the following equation to determine T_J of the device while on the application's printed circuit board (PCB):

$$T_J = T_T + (P_{TOTAL} \times \psi_{JT})$$

Equation 10. Junction Temperature (T_J) Calculation

Where:

T_T = Package temperature (°C) measured at the top center of the package

P_{TOTAL} = Total power consumption (W) as defined in Equation 9

ψ_{JT} = Junction-to-top (of package) characterization parameter (°C/W)

Under natural convection, ψ_{JT} for a thin plastic package is relatively low. This means that under natural convection conditions, the typical T_J is just a little higher than the temperature at the top-center of the package (T_T). The die is physically separated from the surface of the package by only a thin region of plastic mold compound. Unless the top of the package is forcibly cooled by significant airflow, there will be very little difference between T_T and T_J. However, note that ψ_{JT} is affected by airflow and values for ψ_{JT} under various airflow conditions, and PCB design configurations are listed in the *Thermal Characteristics* section of the Blackfin processor data sheets for the two 256-ball mini-BGA (12 mm x 12 mm and 17 mm x 17 mm) and the 297-ball PBGA packages.

The *Thermal Characteristics* section of the data sheet also provides thermal resistance (θ_{JA}) values for all available packages. Data sheet values for θ_{JA} are provided for package comparison and PCB design considerations only and are not recommended for verifying T_J on an actual application PCB.

Industrial applications of the 17 mm x 17 mm mini-BGA package require thermal vias to an embedded ground plane on the PCB. Refer to JEDEC standard JESD51-9 for printed circuit board thermal ball land and thermal via design information.

References

[1] *ADSP-BF561 Blackfin Embedded Symmetric Multiprocessor Data Sheet.* Rev. A, May 2006. Analog Devices, Inc.

[2] *External Power Spreadsheet.* Associated file with *Estimating Power for ADSP-BF561 Blackfin Processors (EE-293).* June 2007. Analog Devices, Inc.

[3] *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228).* Rev 1, February 2005. Analog Devices, Inc.

Document History

Revision	Description
Rev 2 – June 27, 2007 by Joe B.	Updated to new format and includes official power characterization data
Rev 1 – July 13, 2006 by Joe B.	Initial release