ADSP-CM41x Board Design Guidelines for Optimal ADC Performance

Contributed by Leo Mathew *Rev 1 – March 30, 2017*

Introduction

ADSP-CM41xF are a family of dual core mixed-signal control processors based on the ARM® Cortex-M4™ core with floating point unit operating at frequencies up to 240 MHz, and the ARM® Cortex-M0™ processor core operating at frequencies up to 100 MHz consisting of two 16-bit SAR-type ADCs, one 14-bit ADC and one 12-bit DAC, along with the associated analog subsystem and a rich set of peripherals and accelerators. By integrating a rich set of industry-leading system peripherals and memory, the ADSP-CM41xF mixed-signal control processors are the platform of choice for next-generation applications that require RISC programmability and leading-edge signal processing in one integrated package.

When designing ADSP-CM41xF-based systems for optimal ADC performance, mixed-signal design aspects such as selection, placement, and partitioning of analog and digital components must be considered. As the processor, its peripherals, I/Os, and related digital circuits operate at higher clock rates, a significant amount of noise and radiation may degrade the ADC performance. Sustaining ADC performance in a hostile digital environment depends on good design techniques such as proper decoupling, signal routing and grounding. Design problems can result in inaccurate ADC readings, excessive electromagnetic interference (EMI), and unwanted system behavior. Careful management of the board design process ensures better system control and reliability required for precision measurement and control systems. It also significantly reduces development time. This document provides some guidelines for consideration while designing ADSP-CM41xF-based boards with a specific focus on how to achieve the best performance from the processor's ADCs.

ADC Front-End Circuit Design

The analog subsystem of the ADSP-CM41xF processor contains two 16-bit, high-speed, low-power Successive Approximation Register (SAR)-type ADCs. SAR ADCs offer high resolution, excellent accuracy, and low power consumption. ADC1 and ADC2 each have a maximum of 12 multiplexed analog input channels, while ADC0 has 7 multiplexed analog input channels. The board design guidelines given here mostly focus on the primary ADCs- ADC1 and ADC2 while most of the best practices can be utilized for ADC0 as well.

To get the best performance from SAR-type ADCs, designers should first focus on the design of the ADC front end, which interfaces the analog input signal to the ADC input channel. It consists of two parts: the driving operational amplifier (op-amp) and the RC filter shown in Figure 1.

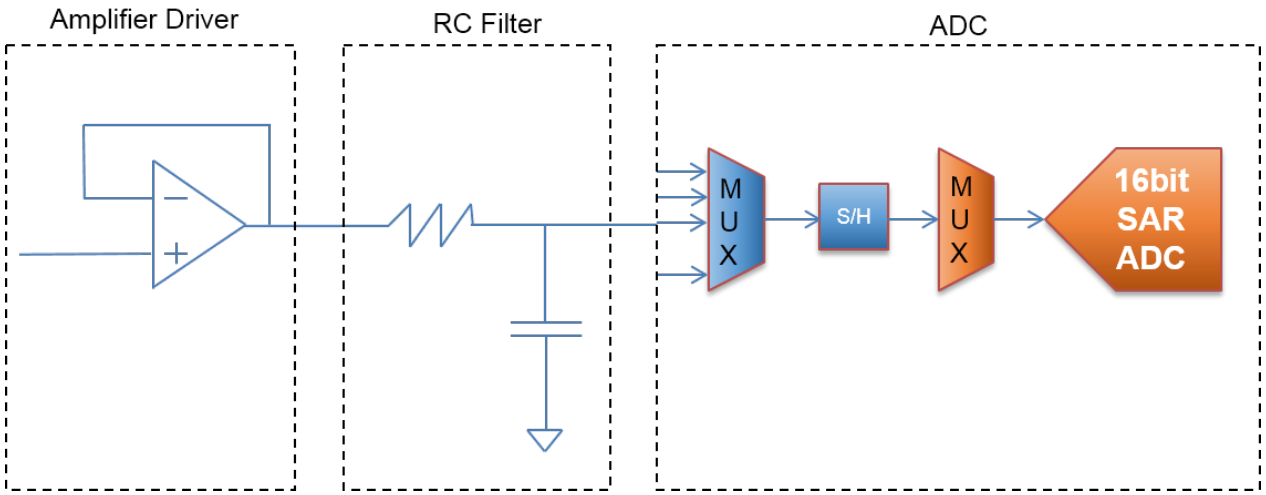

Figure 1. SAR ADC Front End Circuit Design

The amplifier conditions the input signal and acts as a low-impedance buffer between the signal source and the ADC input. The RC filter limits the amount of out-of-band noise arriving at the ADC input and helps to attenuate the kick from the switched capacitors in the ADC's input. The RC network also helps to relax the driving op-amp requirements.

Apart from the analog front end circuit, a signal conditioning circuit may also be required, depending upon the range of the input signal. The ADSP-CM41xF ADC accepts analog signals in the range of 0-3V, which can be achieved by conditioning the analog input signal.

RC Filter Design

The input signal bandwidth determines the low-noise needed over that frequency spectrum to get a good Signal-to-Noise Ratio (SNR). The RC filter network limits the bandwidth of the input signal and reduces the amount of noise fed to the ADC by the amplifier and other upstream circuitry. However, too much band-limiting will increase the settling time and distort the input signal.

To select a suitable RC filter, the RC bandwidth for the ADC channel must be calculated, which is described in the *Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter* article[2]. Using the theory described in this article, consider the case where the maximum input sine wave frequency to the ADC is 5 kHz, and the maximum input voltage is 3V (V_{PEAK} = 1.5V). The values of the external R-C components, R_{EXT} and C_{EXT}, can be calculated using the following specifications from the data sheet[1]:

- ADC Conversion Time (T_{CONV}) = 340ns
- ADC Acquisition Time (T_{ACQ}) = 280ns

The one LSB voltage value for a 16-bit ADC with 3V V_{REF} is 45.77µV; therefore, 1/4th the LSB voltage ($V_{1/4LSB}$, required to settle for best SINAD) is 11.44µV.

The voltage change of the sine wave for every sample (V_{CHANGE}) is:

$$2\pi * fin * V_{PEAK} * T_{CONV} = 2\pi * 5000 * 1.5 * 340e\text{-}9 = 16mV$$

V_{CHANGE} is then attenuated by the parallel combination of the on-chip internal capacitor (C_{INT} = 12pF) and external capacitor (C_{EXT}). Assuming C_{EXT} = 4.7nF, V_{STEP} is:

$$V_{CHANGE} * (C_{INT} / (C_{INT} + C_{EXT})) = 16e\text{-}3 * (12e\text{-}12 / (12e\text{-}12 + 4.7e\text{-}9)) = 40.8\mu V$$

From this, the number of time constants required to settle the input to 1/4th LSB during the acquisition time of the ADC (N_{TC}) can be computed:

$$\ln(V_{STEP} / V_{1/4LSB}) = \ln(40.8e\text{-}6/11.44e\text{-}6) = 1.27$$

The Time Constant (T_{AU}) then becomes:

$$T_{ACQ} / N_{TC}=280e\text{-}9 / 1.27 = 220.2ns$$

And the bandwidth can then be computed:

$$1 / (2\pi * T_{AU}) = 1 / (2\pi * 220.2e\text{-}9) = 723kHz$$

From this, the R_{EXT} value can then be calculated:

$$T_{AU} / C_{EXT} = 220.2e\text{-}9 / 4.7e\text{-}9 = 46.85\ \Omega$$

For this example, 47 Ω resistor value can be used. It is not advised to choose C_{EXT} lower than 3.3nF, as the voltage kick observed due to the sampling action of the ADC may not get fully replenished by the smaller external capacitor. Higher values of C_{EXT} can be chosen, but when used with lower bandwidth buffers, it might result in too much harmonic distortion at the input of the ADC. The resistor value ensures that the op-amp will not oscillate, and the capacitor value ensures that the ADC will have sufficient charge for each conversion. A capacitor with a low-voltage coefficient (which determines the THD of the system) should be chosen.

Note that nominal RC values calculated here are useful guidelines, not a final solution. Choosing the right balance between the R_{EXT} and C_{EXT} components requires knowledge of the input frequency range, how much capacitance the amplifier can drive, and the acceptable level of distortion. Experiment with actual hardware that optimizes the RC values to arrive at the best performance. Place the RC filter as close as possible to the ADC channel pins of the processor to achieve best results. For more information on calculating the RC values beyond the previously referenced article[2], refer to the on-line filter tool provided by Analog Devices, located at http://www.analog.com/filterwizard.

Driving Amplifier Design

It is recommended to have a driving amplifier circuit in the path before feeding the input signal to the ADC input channel. Avoid loading the input signal and thereby errors in ADC measurement. Generally, a low-noise operational amplifier (op-amp) in Voltage Follower mode is used for this purpose. The main factors which affect op-amp selection are input signal bandwidth, settling time requirements, noise and distortion amplifier specifications, and its own effect on system noise. It must have sufficient slew rate and fast transient response to charge the R_{EXT}-C_{EXT} according to input signal changes. In addition to these characteristics, another consideration is the powering of the op-amp.

The ADA4899-1 is an ultra-low-noise (1nV/√Hz) and distortion (<−117 dBc @1 MHz) unity-gain stable voltage feedback op-amp, making it ideal for 16-bit ADC systems which need high slew rates and low noise at unity gain. As for the power, the ADA4899 op-amp needs a dual-5V power supply (+5V and -5V) for the best performance.

If the application strictly demands full range from 0V-3V, or if the user intends to do linearity testing such as DNL or INL using the sine-wave histogram method, then it is recommended to provide a negative power supply with a minimum -2.0V at the -Vs pin of the ADA4899 buffer. There is some distortion close to 0V,

which can contribute to INL degradation. The board can integrate a charge-pump voltage inverter (ADM8828) to generate this negative supply (-5V), as shown in Figure 2.

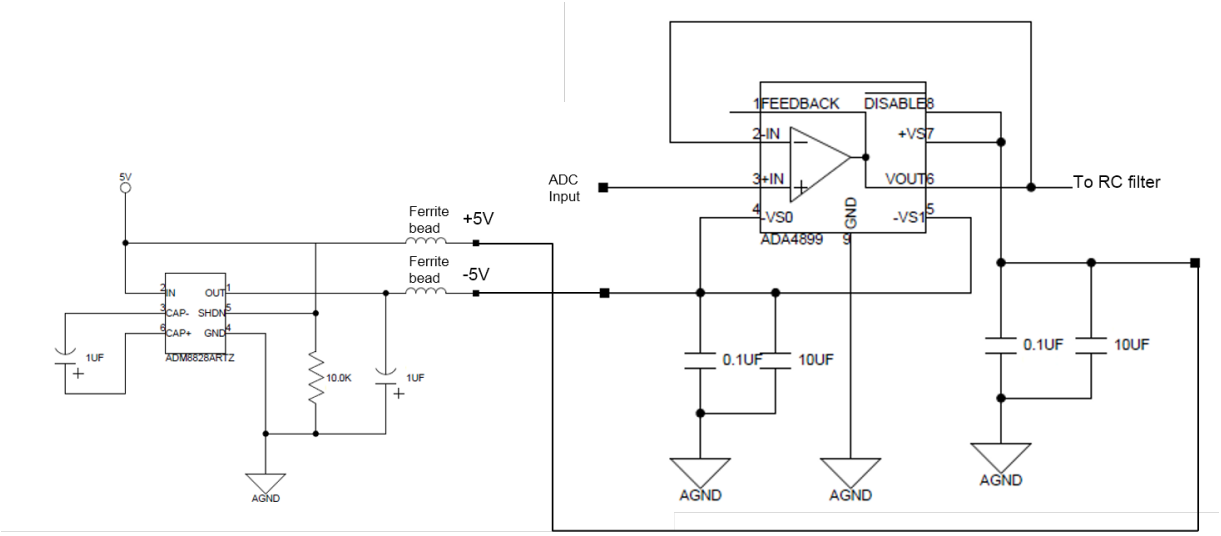

Figure 2. Op-Amp as Driving Amplifier

For a slightly relaxed requirement, the -Vs pin of the op-amp can be connected to ground.

The DISABLEb pin of the ADA4899-1, if brought to within 0.7 V of the positive supply, reduces the input bias current by a factor of 100; hence, connect the DISABLEb pin to +5V and do not leave it floating.

Note that the combination of R_{EXT} and C_{EXT} determines the stability of the operational amplifier. A single-supply AD8655 op-amp can also be used for the driving amplifier if the application does not demand full range and cannot provide a negative supply.

Signal Conditioning Circuit Design

To allow a variety of input signals to be interfaced with the ADSP-CM41xF ADC, signal conditioning must be performed on the analog inputs to get them in the range of 0-3V. Some key components of a signal conditioning circuit are the filter, attenuator, amplifier, and level shifter, depending upon the type of analog signal supplied. If the application provides analog signals in the suitable range for the ADC, it may not be required to add a signal conditioning circuit in the system.

For example, if the analog input is coming directly from a sensor, the signal can first pass through a filter in order to reduce the noise and limit the bandwidth. Then, depending on the range of the analog input, the signal can either be attenuated or amplified to match the range of the ADC. The attenuated/amplified signals can pass through a level-shifter (for bipolar analog signals).

Analog Input Scaling

Most signal conditioning designs use different types of circuits to amplify or attenuate the analog signal. Modern analog circuits consist of basic integrated operational amplifiers, which contain many circuit components but are typically portrayed as a simple functional block.

Amplifier Stage

Many sensors, such as LVDT, thermocouples, generate low-level output signals. These sensor outputs are often weak and must be amplified to occupy as much of the ADC's dynamic range as possible. The amplifying stage can be designed with the help of a non-inverting op-amp, as shown in Figure 3.

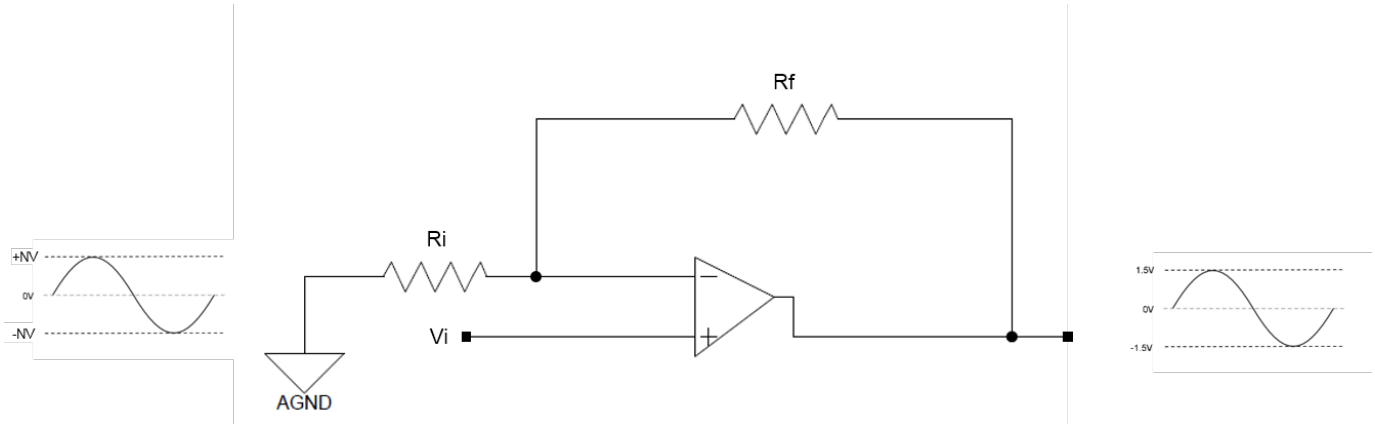

Figure 3. Non-Inverting Op-Amp Circuit

The gain of the amplifier can be set by configuring the feedback (R_f) and input (R_i) resistor values according to the gain equation:

$$V_o / V_i = 1 + (R_f / R_i)$$

For bipolar analog signals with amplitude less than 1.5V, the signals may be amplified before being provided to the ADC. The gain should be configured such that the amplifier output is in the range of -1.5V to +1.5V.

Attenuator Stage

For high-voltage analog signals, the signals must be attenuated to levels acceptable to the ADC. One approach to attenuator circuit design is to use a buffered voltage divider. The circuit shown in Figure 4 consists of a voltage divider followed by an op-amp in the Voltage Follower configuration.

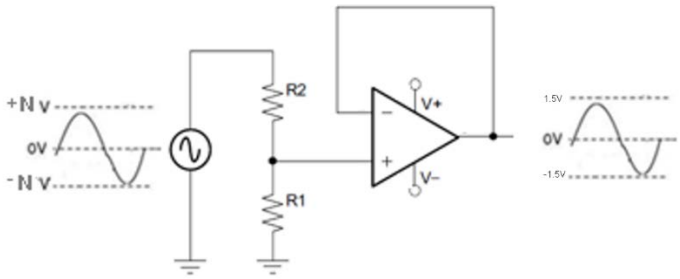

Figure 4. Attenuator Circuit

The attenuation factor can be set by configuring the R1 and R2 resistors according to the equation:

$$V_o / V_i = R1 / (R1+R2)$$

For bipolar analog signals with amplitude greater than 1.5V, the signals should be attenuated before being provided to the ADC. Configure the attenuation factor such that the attenuator output is in the range of -1.5V to +1.5V.

Level Shifter

Bipolar analog signals coming out of the amplifier/attenuator circuit pass through a level shifter to make them unipolar and in the range of 0-3V. A level shifter can be implemented in an AC coupling scheme for this purpose, as shown in Figure 5.

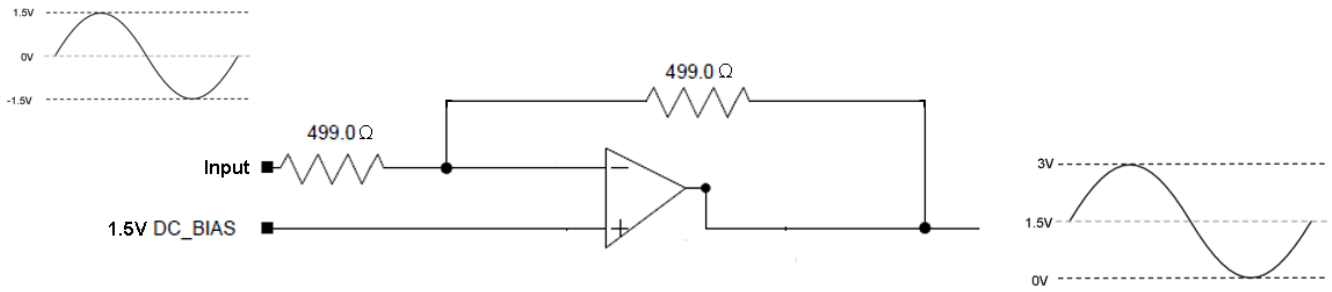

Figure 5. 1.5V Level Shifter

A DC offset of 1.5V is provided by the micro-power, low-dropout (LDO) voltage reference (ADR443BRZ). The voltage reference requires only 500mV above the nominal output voltage on the input to provide a stable output voltage of 3V. A buffered voltage divider can be used to produce 1.5V which is used to level-shift the bipolar analog input.

The level-shifting scheme should be implemented on the board such that the DC offset can be bypassed, if required, depending upon the type of analog signal supplied (unipolar or bipolar). To sample unipolar analog signals, the 1.5V DC_BIAS input must be connected to ground.

Analog Signal Flow Chain

The complete analog signal chain consists of both the signal conditioning circuit and the analog front end circuit, as previously discussed. However, a signal conditioning circuit is optional and depends upon the range of the input signal.

To achieve the best performance, the analog input should be a noise-free signal. Figure 6 provides a complete analog signal chain circuit for the case where attenuation is required. The analog input from a sensor or signal generator passes through an attenuator or an amplifier, depending on the range of the input signal, to scale the signal range to -1.5V to +1.5V. The signal then passes through a 1.5V level shifter to shift the range to 0-3V. After conditioning the analog input signal, the driving amplifier helps to drive the ADC, and then the signal passes through the RC filter before being supplied to the ADSP-CM41xF ADC input channel.

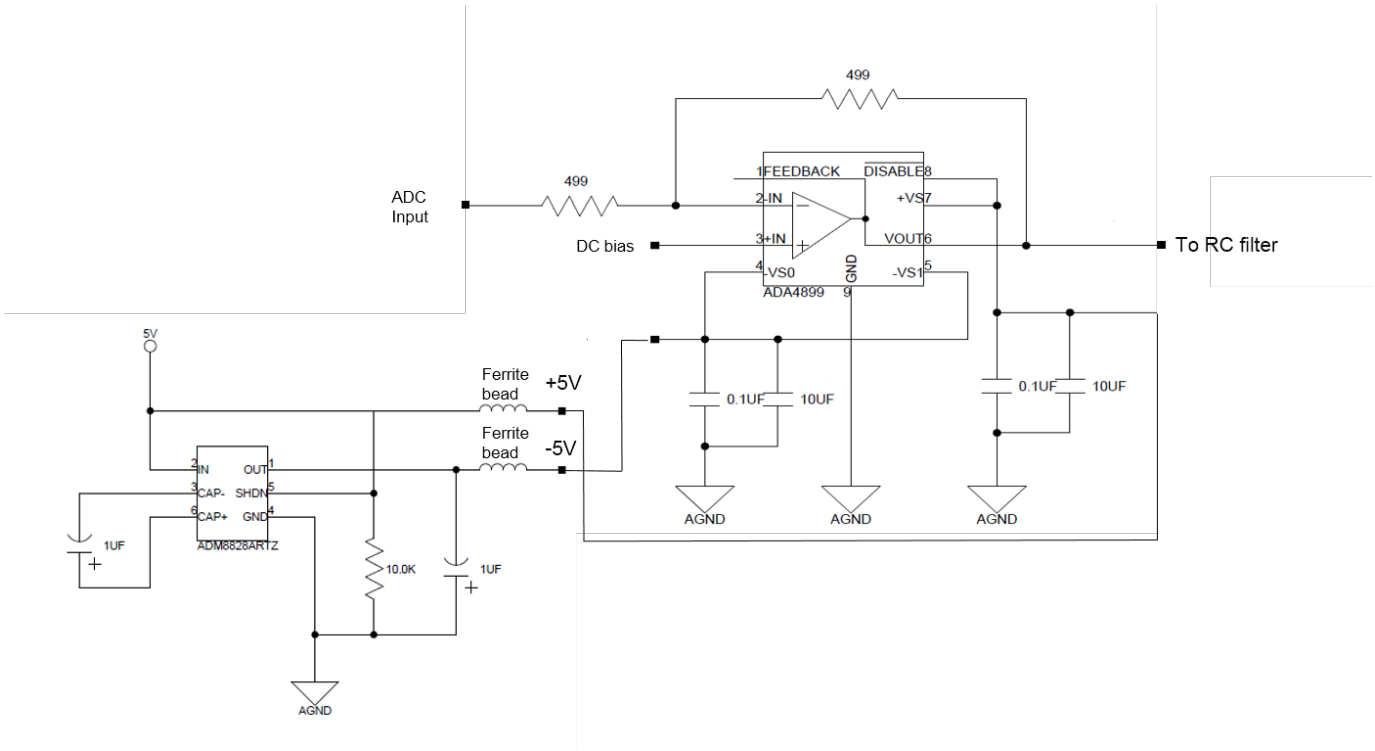

Figure 6. Analog Signal Flow Chain

Power Supply Design

The power supply is a very important aspect of the board design and one of the major factors in controlling noise and radiation. A clean and stable power supply is required for all system designs. In a mixed-signal system, having separate power supplies for the analog and digital circuits is highly desirable.

Thoughtfully determining the power supply architecture that is the best fit for the application is extremely important. The SMPS (switching mode power supply) has high efficiency, which makes it an ideal choice for designs where saving power is critical, such as in battery-powered applications; however, switching supplies introduce high-frequency noise to the power supply net. Linear regulators have some advantages, such as low noise with a high power supply rejection ratio, fast response to load changes, and low cost.

The ADSP-CM41xF processor has three main power domains:

- VDD_EXT – 3.3V digital power domain for flash memory, peripherals, and I/O
- VDD_INT – 1.2V digital power domain for M4 core operation
- VDD_ANA – 3.3V analog power domain used by the processor's analog subsystem

It is recommended that all three power domains be separately generated from LDO regulators rather than switching regulators. Switching regulators can increase ground bounce noise and lead to a leakage path in the analog power domain. Further, the VDD_EXT and VDD_ANA power domains should not be shared, despite the fact that they are both 3.3V. As such, separate power planes should be created for VDD_EXT and VDD_ANA, and it is critically important that digital power planes do not overlap analog power planes.

Also, VDD_EXT and VDD_ANA should have separate ground planes with VDD_EXT referring to DGND and VDD_ANA referring to AGND that. Each power plane should have a corresponding overlap of the ground plane in one of the adjacent layers.

Figure 7 shows a typical power supply design for an ADSP-CM41xF system.

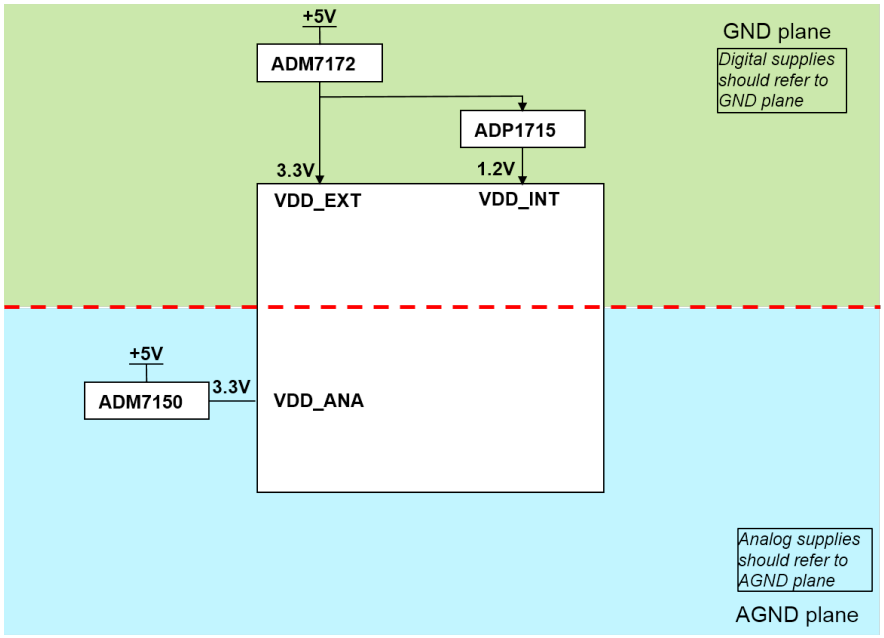

Figure 7. Typical Power Supply Network for an ADSP-CM41xF System

The VDD_INT supply can be internally generated using a STD2805T4 PNP transistor connected to the VREG_BASE pin of the processor.

Bypass/Decoupling Capacitors

A proper decoupling scheme is needed on both the analog and digital power supplies. Good decoupling is important to control the noise within the system and to ensure that power supply drop is lower than the specified limits. For the digital portion, the capacitors on the VDD_EXT and VDD_INT power supplies serve as mini-charge-reservoirs for the respective domains. For the analog subsystem, the bypass capacitors on the VDD_ANAn power supplies help to redirect high frequency noise that may otherwise enter the sensitive analog portion of the chip through the power supply pins.

The analog subsystem of the processor also brings out a few pins for bypassing purposes:

- BYP_An – the on-chip analog power regulation bypass filter node for the ADC
- BYP_D0 – the on-chip digital power regulation bypass filter node for the analog subsystem
- REFCAPn – analog output of the band-gap generator filter node

Bypass capacitors on the BYP_An and REFCAP pins should be connected to analog ground (AGND), and bypass capacitor on the BYP_D0 pin should be connected to digital ground (DGND). In addition to these recommendations, the VREF pins should also be properly terminated with bypass or decoupling capacitors to analog ground (AGND).

The recommended bypass/decoupling capacitor values for the analog subsystem are:

- VDD_ANA0, VDD_ANA1, and VDD_COMP: parallel 0.01µF, 0.1µF and 10µF
- VREF0 and VREF1: parallel 0.1µF and 10µF
- BYP_A0, BYP_A1 and BYP_A2: 10µF
- REFCAP0, REFCAP1 and REFCAP2: 0.1µF

Important note: The ESR value of VREF capacitors should be less than 10mΩ (Reference part number used in CM41xF EZKIT: JMK107BJ106MA-T).

Figure 8 and Figure 9 show the recommended decoupling scheme for the analog and digital sections of the processor:

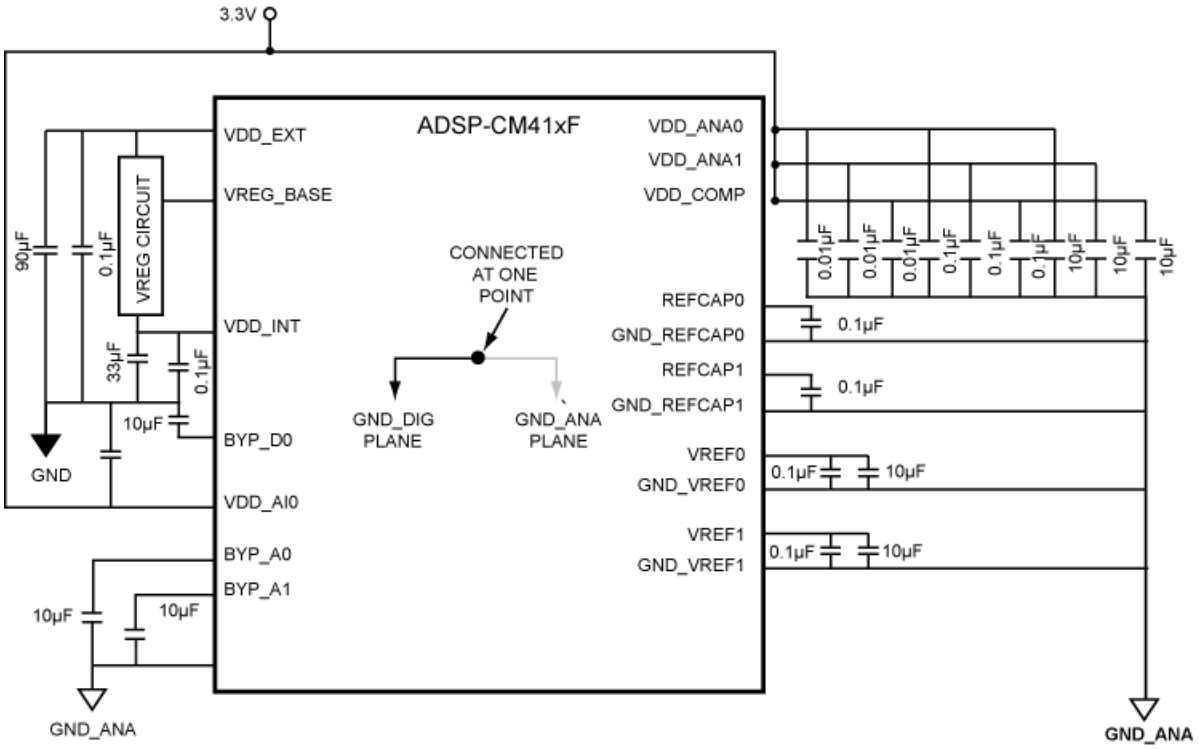

Figure 8. Recommended Decoupling Scheme for ADSP-CM411F, ADSP-CM412F, ADSP-CM413F, ADSP-CM416F, ADSP-CM417F

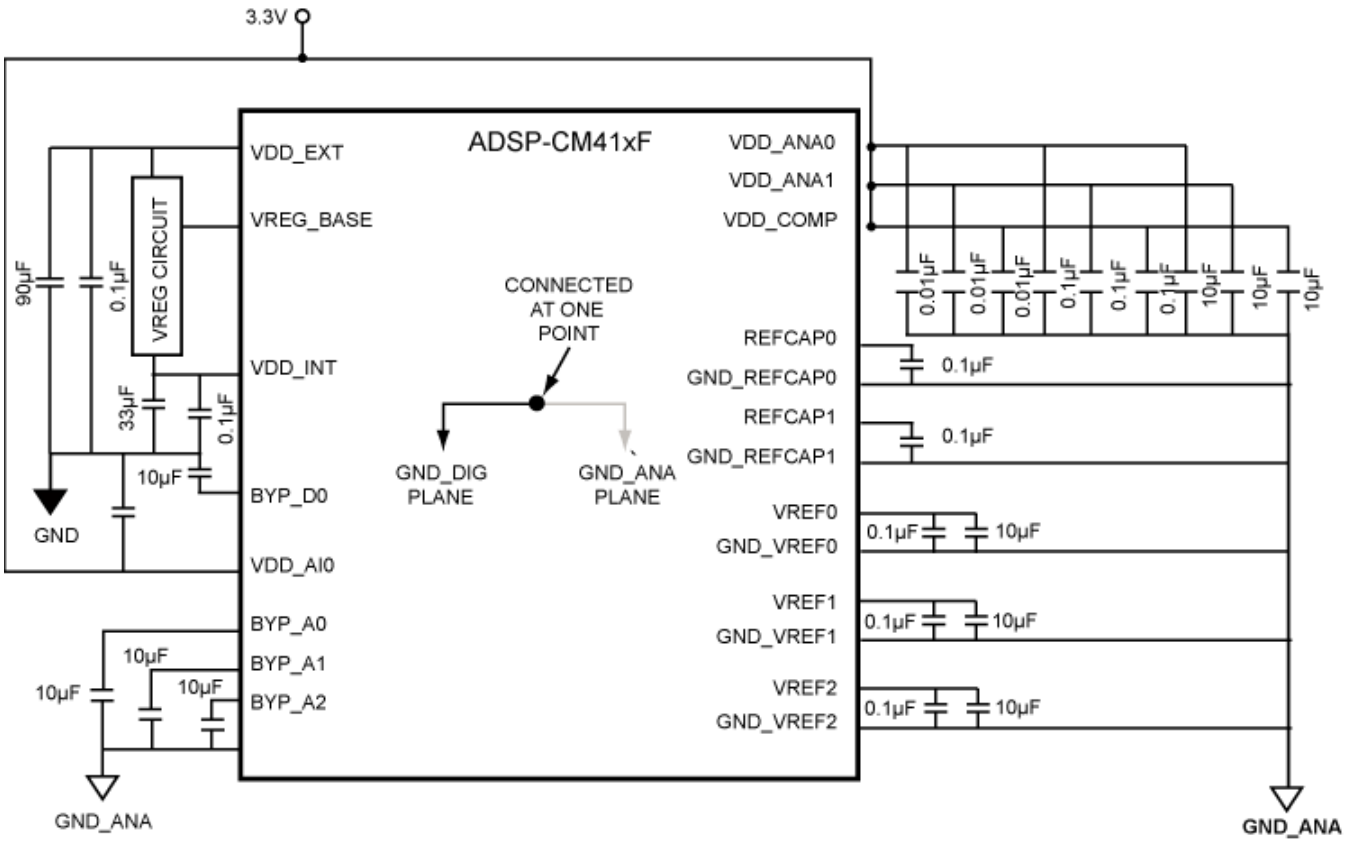

Figure 9. Recommended Decoupling Scheme for ADSP-CM418F, ADSP-CM419F

The digital power supplies (VDD_EXT and VDD_INT) should be decoupled with 10µF capacitor. In addition, connect 0.1µF and 0.01µF capacitors in parallel for individual VDD_EXT and VDD_INT pins.

To achieve the best outcome from this decoupling scheme, the capacitors must be placed as close as possible to the respective pins, ideally adjacent to the device, with the smallest capacitors closest to the pins and with the widest possible trace. Ceramic capacitors are the best choice for these decoupling capacitors. The capacitors should have low Effective Series Resistance (ESR) and Inductance (ESL), which provides a low-impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

Note: Place high frequency capacitors closest to the pins and then the bulk capacitors.

Unused Processor Pins

Handle the unused GPIO pins of the processor in one of the following ways:

- Configure in GP output mode and driven low
- Configure in GP input mode with input buffer enabled (set INEN bit) such that these pins is tri-stated and the internal pull-up resistor on them is disabled.

Board Layout Guidelines

Though PCB layout is one of the last steps in the design process, it is the most critical. Grounding of analog and digital components is one of the most debated topics in a mixed-signal system design. A common concern is how to isolate the analog and digital grounds so that the noisy digital circuitry does not interfere with the analog circuitry and affect its performance. Analog circuitry is highly susceptible to noise and can be easily affected by large, fast-switching current spikes drawn by the digital circuitry. Ideally, the sensitive analog components are totally isolated from the noisy digital circuitry in terms of placement, routing and plane creation. It is also possible that high-speed digital logic might get interference from the low-level analog circuits. The following are some guidelines for better ADC performance.

- It is beneficial to use separate ground planes for the analog and digital circuitry, using the split-plane ground technique. Separating the analog current return path from the noisier digital current return path can improve ADC performance.
- Use a large-area, low-impedance ground plane to provide a better return path for decoupling high-frequency currents and to minimize EMI/RFI emissions. Currents should be efficiently returned to their sources through the smallest possible loop.
- The analog and digital ground planes should not overlap one another. This configuration avoids, or at least minimizes, capacitive coupling between them, which may cause RF emissions from one plane to another.
- Placement of components is very important with analog and digital circuits kept in separate sections. Analog traces should be routed under the analog sections only, with respect to their analog reference planes. Digital traces should run only with digital reference planes to maintain the homogeneous nature of current density (i.e., digital currents must not flow in the analog section of the ground plane and vice versa). This is the decisive factor in ensuring how well analog circuitry signals flow through the PCB, as well as how the planes are split to keep analog characteristics isolated from the digital section. Arrange the different blocks in a way that minimizes the interaction between the potentially noisy circuit blocks and sensitive analog circuits.
- Some of the common recommendations with respect to signal traces are:
  - minimize trace length
  - keep trace width constant throughout the length of the trace
  - the traces should not have sharp 90 degree turns
- The best layer stack-up strategy is to use a ground plane under each new signal or power plane. The return current of one signal will have a minimal effect on another signal. Placing the ground planes close to a signal source reduces inductance (The idea is to reduce the loop area and hence the EMI). But, for cost reasons, each signal layer can be placed in between a ground plane and a power plane.
- It is suggested that, for each power plane a corresponding ground plane should be made to overlap it in one of the adjacent layers. In case of ground/power planes of the same net running on multiple layers, there should be sufficient number of stitching vias to eliminate any necking effect. Also, the ground plane should not have many discontinuities. This layout is particularly a problem in areas directly under the chip, where multiple power nets are to be routed efficiently and sufficient number of stitching vias need to be present.
- The components in analog circuitry and the ADSP-CM41xF processor should be soldered directly to the respective signal, power or ground pads to minimize series inductance and resistance. The use of

traditional IC sockets is not recommended, as they may add extra inductance and capacitance to degrade the device performance. If sockets must be used, as in prototyping, the leads should be mechanically very tiny and should have as little self-inductance and self-capacitance as possible.

Design Evaluation

CM41xF EZKIT is designed based on the recommendations and guidelines described in this EE-note. The following sections provide some important layout details.

ADSP-CM419F BGA Evaluation Board

Figure 10 shows an evaluation board that serves as an example of effective partitioning. The layout places analog components and associated circuitry on the right side of the PCB and digital circuitry on the left. The analog ground (AGND) and digital ground (DGND) planes are physically separated, and traces are separately routed underneath the respective ground and power planes.

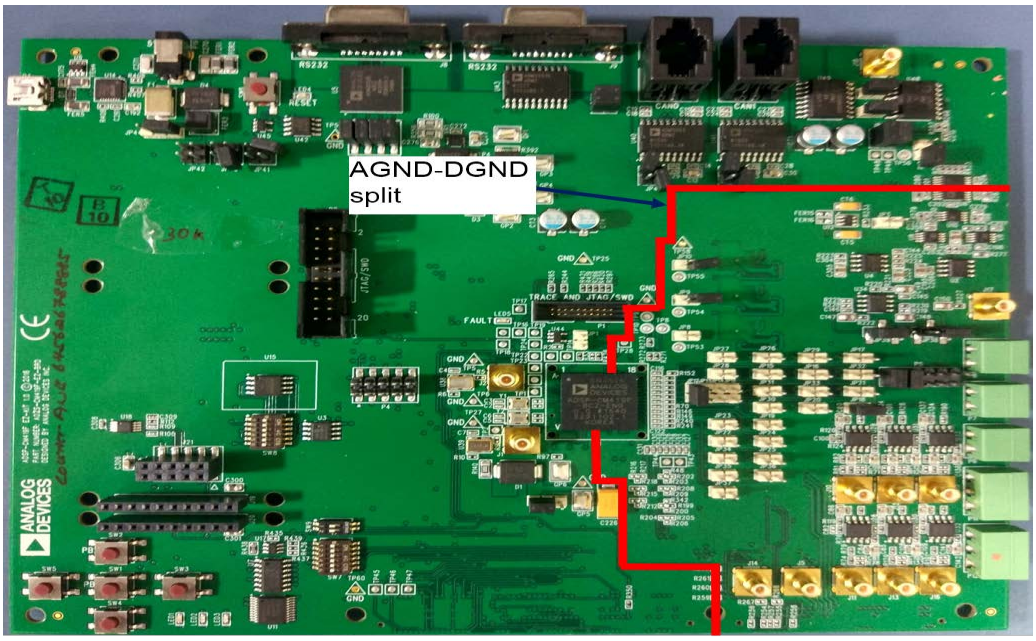

Figure 10. ADSP-CM419F BGA Evaluation Board

Figure 11 through Figure 14 show some layout schematics for this board.

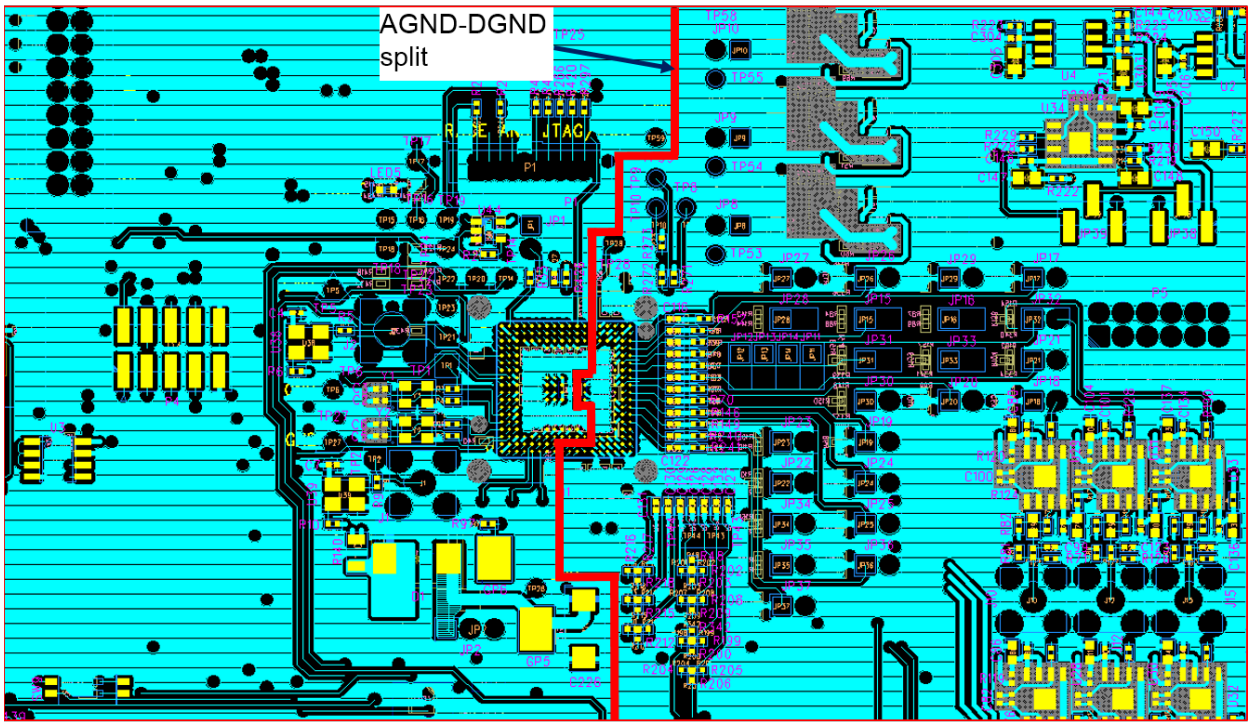

Figure 11. Spacing between Analog and Digital Signals

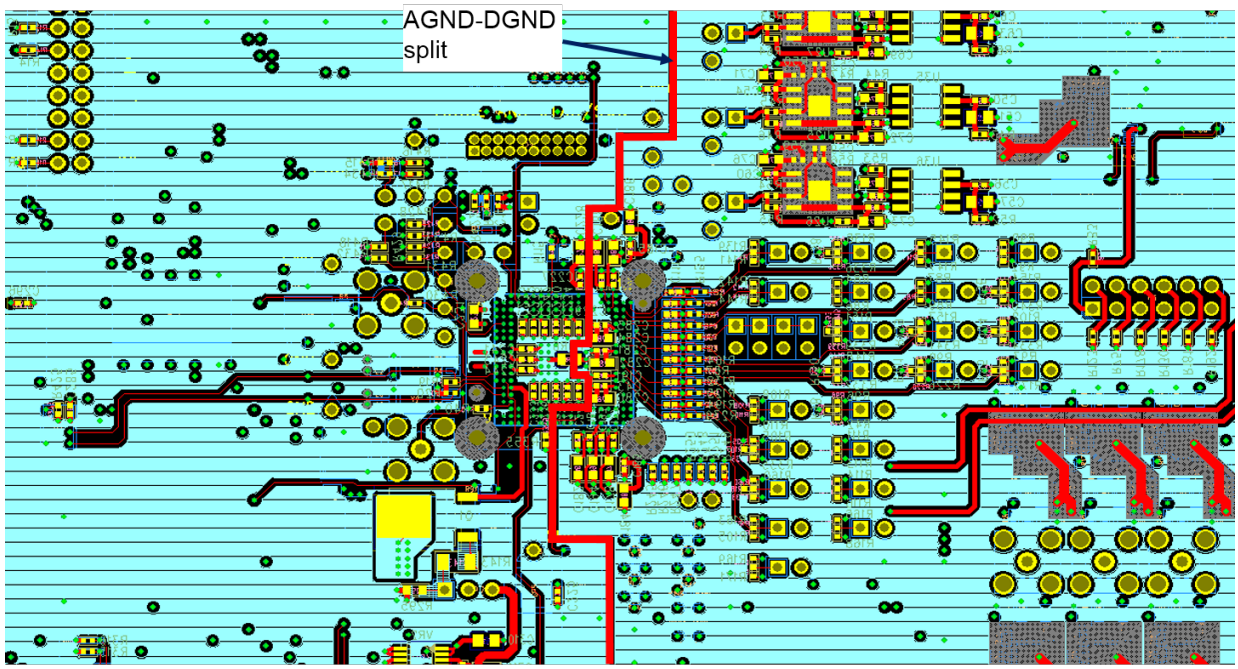

Figure 12. Analog and Digital Ground-Splitting Technique

Both the analog and digital ground planes must be tied together at a single point directly under the chip through a low-impedance bridge or, preferably, a ferrite bead (as shown in Figure 13).

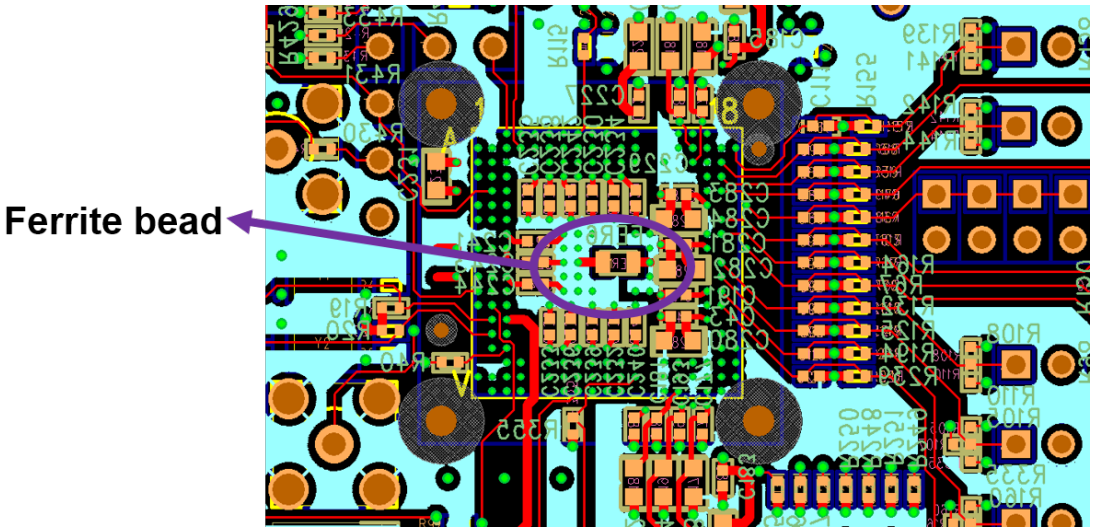

Figure 13. Analog and Digital Grounds Tied Together through a Ferrite Bead directly under the chip

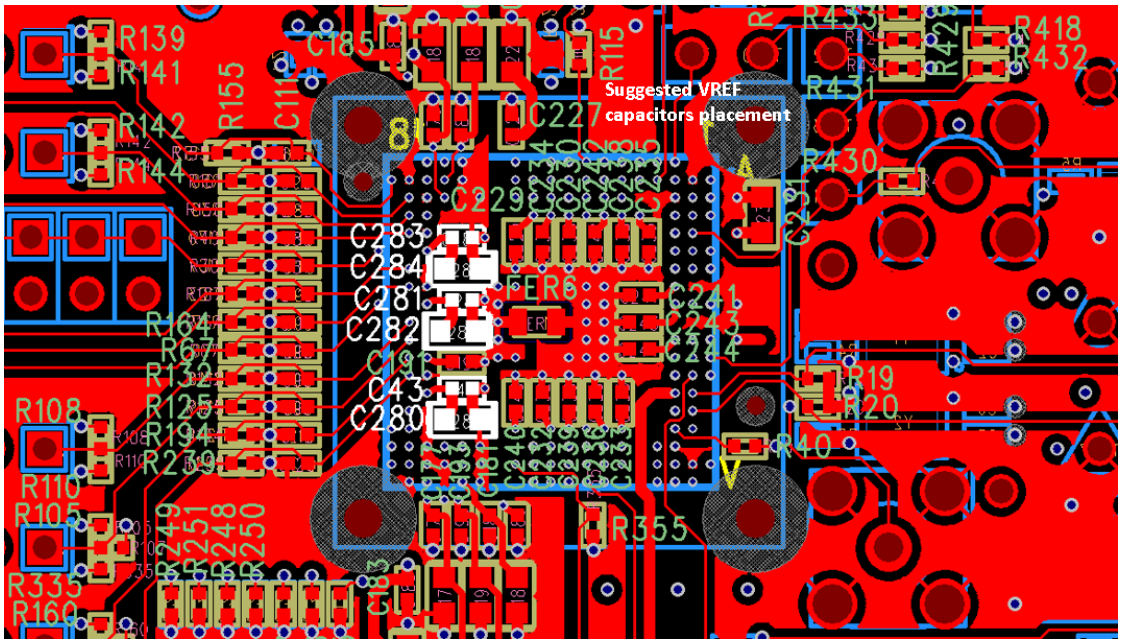

Figure 14. Recommended Placement of Reference Capacitors (as Close to Pin as Possible)

References

[1] *ADSP-CM411F/412F/413F/416F/417F/418F/419F: Mixed-Signal Dual-Core Control Processor with ARM Cortex-M4/M0 and 16-bit ADCs Preliminary Data Sheet* (Rev. PrB), February 2016. Analog Devices, Inc.

[2] *Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter.* Analog Dialog Volume 46, December 2012. Analog Devices, Inc.

[3] *ADSP-CM40x Board Design Guidelines for Optimal ADC Performance (EE-380).* Rev 1, December 9, 2015. Analog Devices, Inc.

Readings

[4] *ADSP-CM41x Mixed-Signal Control Processor with ARM Cortex-M4/M0 and 16-bit ADCs Hardware Reference (Rev. 0.2), May 2016. Analog Devices, Inc.*

[5] *The Data Conversion Handbook.* 3rd ed. Analog Devices, Inc, 2005.

Document History

Revision	Description
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