AN-1541
APPLICATION NOTE

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Preliminary Technical Data

ADSP-CM417F Family Arc Detection Module

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INTRODUCTION

Arcing is a potential danger in photovoltaic (PV) systems. Arcing can occur when the dc line of a PV system breaks, creating an open circuit. Due to constant high power flowing through the dc line, an arc generates across this open circuit. This arc builds and increases in power and causes fire and major damage to the PV system and potentially to people.

To ensure the safe use of a PV system, there is an industry recognized safety standard called UL1699B. The UL1699B standard describes the need for safety monitoring and reaction in a PV system. One such requirement is the detection of an arc within the allowed arc detection response time. For example, with systems over 900 W, an arc detection solution must detect and disconnect in under 800 ms. Fires in solar farms and the resulting personal safety hazards are driving the need for an arc detection solution to be implemented in a PV system. In fact, in North America, an arc detection solution is required by law. This need for an arc detection solution has caused manufacturers and designers of PV inverters to implement an affordable and reliable solution. The ADSP-CM417F family of devices, which includes the ADSP-CM411F, the ADSP-CM412F, the ADSP-CM413F, the ADSP-CM416F, the ADSP-CM417F, the ADSP-CM418F, and the ADSP-CM419F, is designed to meet the UL1699B standard.

The Analog Devices, Inc., arc detection solution is founded on the ADSP-CM417F controller microprocessor family. The ADSP-CM417F family is designed to monitor and control the dc energy harvested from a PV panel as well as contribute to the conversion of this dc energy to ac energy that is suitable to be supplied to the grid. The ADSP-CM417F family also provides safety features that are vital to the health of all aspects of the PV system. Additionally, the ADSP-CM417F family has other applications in battery management and charging.

Analog Devices successfully integrates building blocks for arcing detection into control processor architecture. These building blocks include an internal analog-to-digital converter (ADC), windowing, and a hardware fast Fourier transform (FFT) engine. The Analog Devices arc detection solution is demonstrated on the ADSP-CM417F family 6-channel, arc detection board. This demonstration includes a graphical user interface (GUI) where a user can edit ADC and software parameters as well as examine raw data.

ARC DETECTION BOARD PHOTOGRAPH

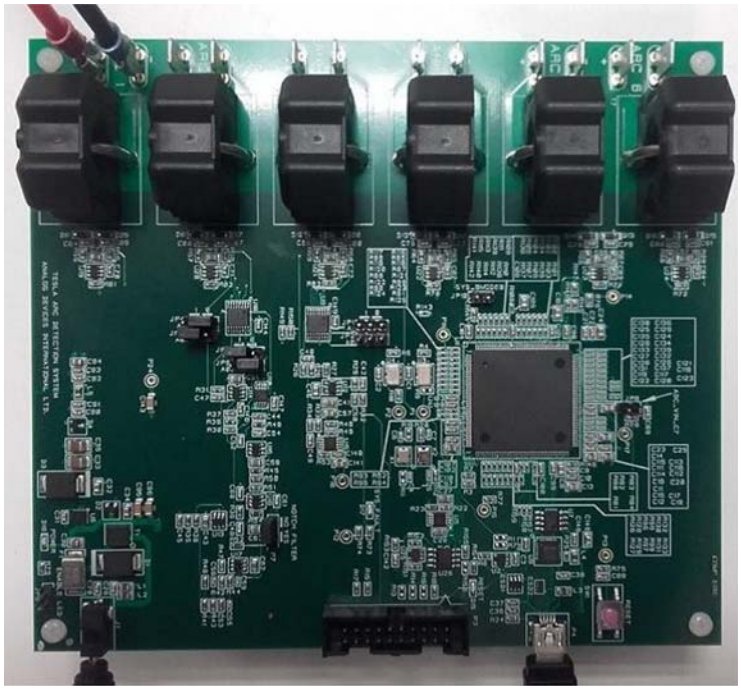

Figure 1.

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HARDWARE OVERVIEW

An arc is noisy. When an arc is occurring, the frequency noise floor of the dc line increases over a range of frequencies. Performing an FFT of this dc line and examining its frequency components is an effective way of determining whether an arc is detected.

The ADSP-CM417F family processor monitors the PV panel dc line for arcs. When an arc occurs, the ADSP-CM417F family device detects the arc and performs a rapid shutdown. The ADSP-CM417F family devices are made up of two independent processors, the Cortex-M4 and the Cortex-M0. The Cortex-M0 provides vital safety features for PV systems. Arc detection is one such feature. This feature allows the Cortex-M4 to focus completely on the gate control of the dc-to-dc and ac-to-ac converters as well as overall monitoring of the system and wireless communications. The Cortex-M0 ADC, ADC0, measures the dc line. The output of this ADC is fed to a hardware FFT engine for frequency analysis without any processor intervention. The result of this frequency analysis is displayed on a monitor and can be examined on the **Arc Detection Configurator** GUI under the **Monitor** tab.

Before the measured dc line signal reaches ADC0, the signal must first cross a galvanic isolation barrier. The arc detection board has six available channels. Each channel can monitor six different PV strings through a Rogowski coil placed across the isolation barrier. This coil outputs a voltage that is proportional to the ac current flowing through the dc line. The dc current is ignored.

This voltage output is then input to a gain stage value of 11. The purpose of this gain stage is to allow the FFT block (FFTB) to easily detect any amplitude increase of the dc line noise floor. At this point, the six channels are connected to six inputs of the ADG728. The ADG728 is an 8-channel matrix switch. This matrix switch has one output, meaning that one of the six inputs to the ADG728 can be selected as an output, which is achieved by communication between the ADSP-CM417F family device and the ADG728 through the I²C serial communication protocol. Jumper JP3 and Jumper JP4 determine the bit address of the ADG728. For the ADSP-CM417F family device to recognize the bit address of the ADG728, set JP3 to 1 and JP4 to 0.

The output of the ADG728 is connected to another gain stage. The gain value of this stage is 10. This stage includes the AD5258 64-position digital potentiometer. Similar to the ADG728, using the I²C serial communication protocol, the ADSP-CM417F family device can transmit and receive data to and from the AD5258. In addition, set JP5 to 0 and JP6 to 1. The AD5258 is programmed to maximize the gain value of this stage. Including the first stage, the total gain value of the signal chain is 111. The output of the second gain stage is connected to a band-pass filter. The band-pass filter is designed to have its lower cutoff frequency at 50 kHz and upper band-pass filter at 220 kHz. This design is necessary to prevent any interference influencing the ADSP-CM417F family device decision making process when deciding if an arc is detected or not. The output of this filter is connected to ADC_VIN_D0, the first channel of the Cortex-M0 ADC. The signal chain includes an optional final notch filter stage. This signal is included in the signal chain by the position of Jumper JP7.

When an arc is detected, the D18 light emitting diode (LED) labeled POWER toggles. The ADSP-CM417F family device toggles a general-purpose input/output (GPIO) pin. This pin is connected to D18 by a jumper wire located under the arc detection board. Jumper JP9 must remain open for D10 to toggle. A mini-USB can connect the arc detection board (P4) to a PC, enabling the use of the arc detection software GUI.

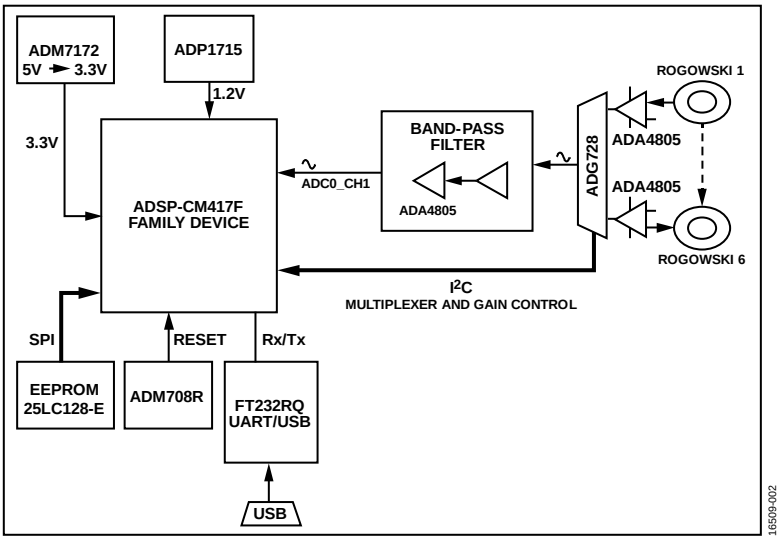

Figure 2. Block Diagram of Arc Detection Board

SOFTWARE OVERVIEW

A problem in any arc detection solution is the potential of false arcs. A false arc occurs when the Cortex-M0 detects an arc occurring when an arc is not occurring. This false detection can happen if the dc line induces noise. For example, the PV inverter itself induces noise in the system on the dc line. The ADSP-CM417F family arc detection solution must be able to recognize and discriminate between the noise induced by the PV inverter (as well as random noise) and the noise induced by an arc. A false arc causes the Cortex-M0 to shut down a string of PV panels for no reason, preventing the PV inverter from harvesting energy. This loss of energy is undesirable and must be prevented. The Cortex-M0 processor prevents the detection of false arcs by utilizing an arc detection software algorithm.

The software makes use of the spectral characteristics of arc signals to distinguish arcing noise from other noise signals.

The comb filter present as part of the FFTB in the ADSP-CM417F family processors helps remove the switching noise present in the signals. The output of the comb filter is windowed and a 512-point FFT is applied on the signal. The spectral output is compared against a reference spectrum and a proprietary decision logic is applied to make a robust decision whether incoming signal is an arcing noise or not.

A signal chain of the decision process is shown in Figure 3. All blocks through spectral comparison are done in the hardware accelerators of the ADSP-CM417F family, freeing valuable core resources for other tasks. The software also features an automatic profiling capability, which, if enabled, updates the plant profiling automatically for various environmental conditions.

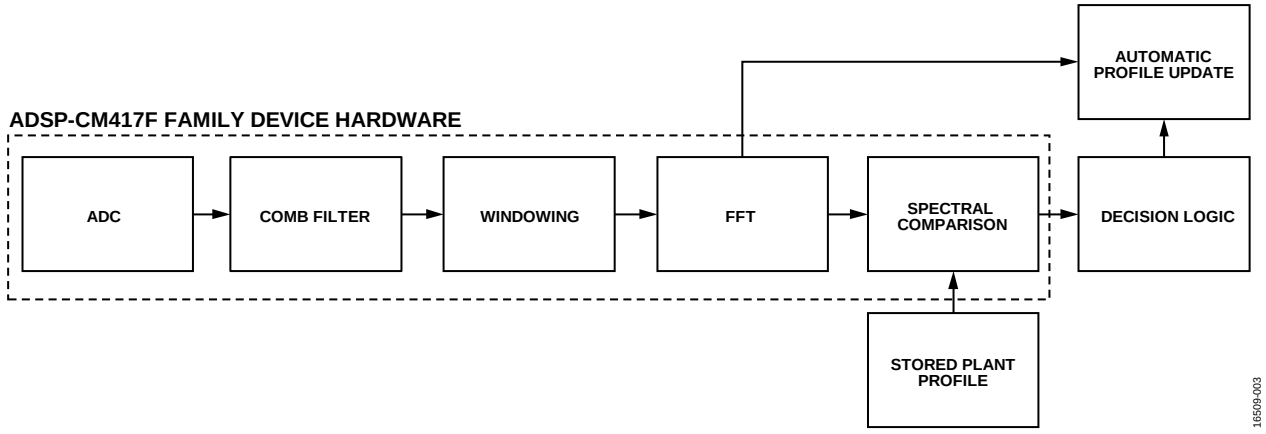

Figure 3. Arc Detection Software Signal Chain

SOFTWARE CONFIGURATION

The arc detection software includes a Windows-based GUI for easy configuration of various parameters.

CONFIGURE TAB

Figure 4 shows the arc detection GUI **Configure** tab.

Communication

The parameters in this group control the communication between the ADSP-CM417F family arc detection board and the host.

The **Port** box selects the universal asynchronous receiver transmitter (UART) port connected to the arc detection board.

The **Baudrate** box selects the baud rate for the connection between the arc detection board and the Windows-based PC (the default setting is 115200).

The **TimeOut** box selects the time (in milliseconds) to wait for a response from the arc detection board. A timeout error is flagged if there is no response from the arc detection board after this interval.

FFT

The parameters in this group control the FFTB of the ADSP-CM417F family device.

The **Switching Noise Frequency** box selects the switching frequency of the inverter. The comb filter is configured to remove this frequency from the spectrum before feeding to the FFT. A value of 0 disables the comb filter.

The **Sampling Frequency** box selects the ADC sampling frequency.

The **Number of Channels** box selects the number of input channels connected to the ADC.

The **Limit Spectra File** box selects a file that populates the limit spectra buffer of the FFTB with the values provided in the file. The limit spectra buffer is then used for spectral comparison. The file must be in binary format, and values in the file must be 32-bit unsigned integers (interpreted in 0.32 format). This option is useful if there is already a plant profile available offline. If the plant profile is not available offline, this box can be left blank and a profile can be calculated by clicking the Record Spectra button.

The **Window Coefficients File** box selects a file while loading the window buffer of the FFTB with the values provided in the file. The window buffer is then used as the coefficient for windowing the output of the comb filter before calculating the FFT. The file must be in binary format and values must be 16-bit unsigned integers (interpreted in 0.16 format) for ½ the window length.

Profile Calculation

The parameters in this group control the plant profiling calculation of the arc detection board.

The **Enable Auto Profile** check box enables automatic profiling. The plant profiles are calculated internally every frame and applied for spectral comparison per the configured intervals.

The **Reference Scale** box scales the spectral values calculated by the algorithm by the selected value before using these values as reference for spectral comparison. The minimum expected value is 1.0. If this value is increased, the probability of false positives decreases. However, this decrease also means that the probability of false negatives increases.

The **Auto Update Interval (ms)** box selects the interval (in milliseconds) to apply the updated plant profile.

The **Auto Reset Interval (ms)** selects the interval (in milliseconds) to reset the plant profile. By default, the plant profiling algorithm calculates the new profile, taking the previous one as its base. The plant profile is cleared each reset interval. Therefore, if this profile clear is not desired, set this box to an appropriately high value.

The **Record Spectra** button records the spectral characteristics of an input channel. The channel number for recording can be configured in the box adjacent to the **Record Spectra** button. The recorded spectra are used for calculating the plant profile for spectral comparison and are saved in the flash memory present in the arc detection board.

Algorithm

The parameters in this group control the core decision logic of the arc detection board.

The algorithm works by looking at each FFT frame and determining whether it is an arc. The **Number of Analysis Blocks** box sets the number of frames in a window. If the number of frames with an arc in a window set using the **Number of Analysis Blocks** box is greater than the number selected in the **Allowed Error Blocks** box, an arc error is flagged.

The **Minimum Bins in Cluster** box and the **Minimum Consistent Bins** box control how an FFT frame is marked as a frame with an arc. Increasing these values reduces the probability of false positives but also increases the probability of false negatives.

MONITOR TAB

The GUI also provides the capability to monitor the signals from various points in the signal chain.

The **X Axis** and **Y Axis** boxes determine whether the axes of the plot displayed in the left pane are in **Linear** scale or **Log** scale.

The following data from the arc detection board can be plotted in the GUI by selecting the corresponding check box:

- **Windows Coefficients** selects the coefficients used for windowing.
- **Comb Output** selects the output of the comb filter.
- **Magnitude Spectra** selects the magnitude spectra of the frame used for the last spectral comparison.
- **Reference Spectra** selects the reference spectra used for spectral comparison.

DEBUG TAB

The GUI can also be used to dump various signals into files. The following data from the arc detection board can be saved to a file for further analysis by clicking the corresponding option button and then clicking the **Save** button.

- **Mag+Comb** selects the FFT magnitude spectra and the comb filter output.
- **Magnitude** selects the FFT magnitude spectra.
- **Limit Spectra** selects the FFT limit spectra.
- **ADC** selects the ADC output.
- **Comb Output** selects the output of the comb filter.

If the **CSV Format** check box is selected, the files are written in .csv format. Otherwise, the files are written in binary format.

The **Get Log** button fetches the log messages from the arc detection board and displays these messages in the **Log Window** pane to the left of the button.

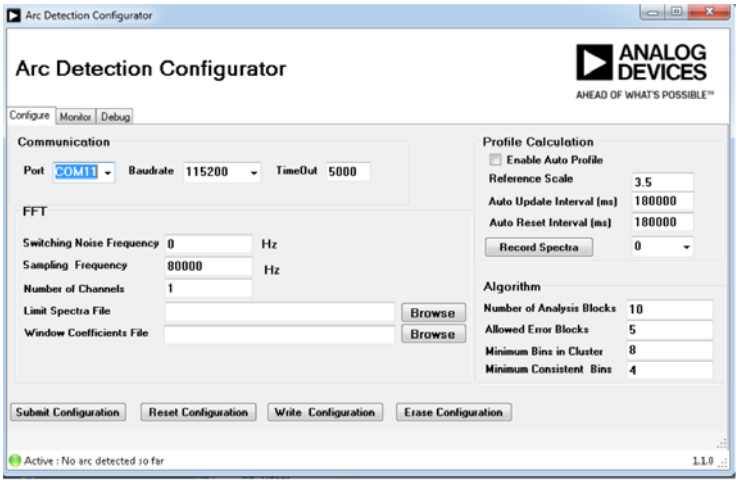

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*Figure 4. Arc Detection GUI **Configure** Tab*

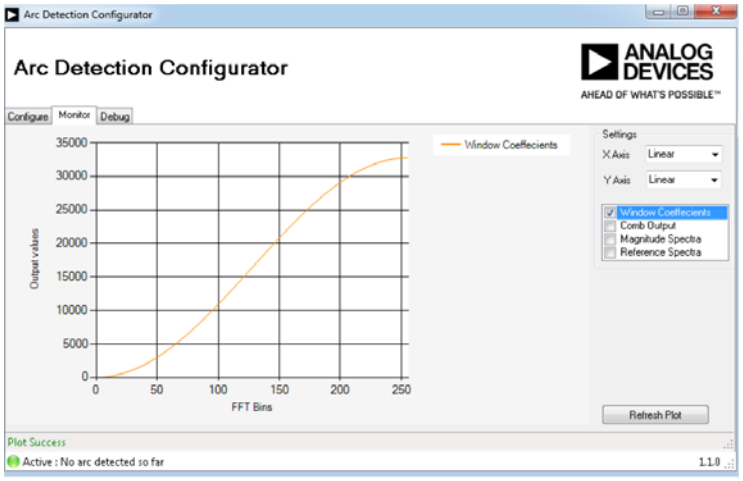

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*Figure 5. Arc Detection GUI **Monitor** Tab*

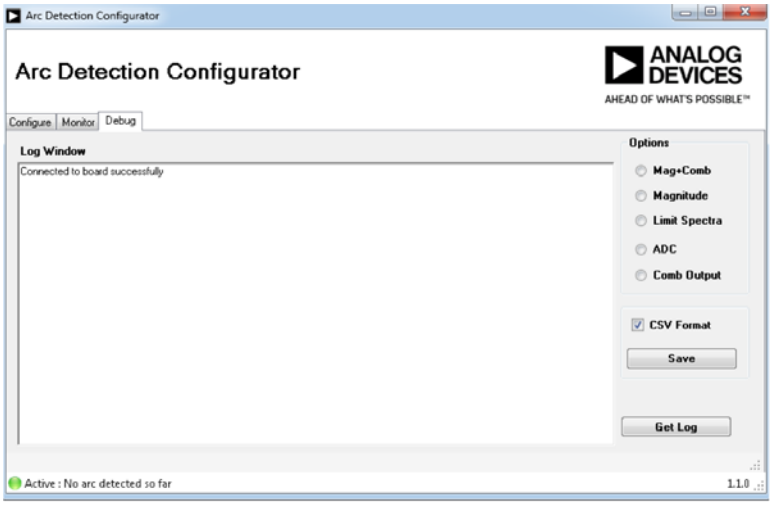

*Figure 6. Arc Detection GUI **Debug** Tab*

RESULTS

The ADSP-CM417F family arc detection solution was tested under the following lab conditions. Figure 9 shows a block diagram of the arc detection test setup. A dc power supply was used to simulate the output of a PV panel. This power supply provided voltage and current values of up to 300 V and 3 A, respectively. A 100 Ω resistor was connected to the output of the power supply for the purpose of current manipulation. An arc generator connected the resistor to a PV inverter in series through a 150 m cable. A spectrum analyzer was placed on the dc input of the inverter to monitor the frequency domain of the dc line. This spectrum analyzer is shown in Figure 7 and Figure 8. An ADSP-CM417F family arc detection board was connected to the system in series with the PV inverter. This test setup allowed the testing of the ADSP-CM417F family devices for arc detection.

The ADSP-CM417F family arc detection solution detected all arcs generated in the lab, resulting in a detection rate of 100%. This solution is capable of detecting arcs in PV systems with a 150 m cable installed.

Figure 7 shows a frequency analysis of the dc line when an arc is not being generated. Any noise seen in the spectrum is caused by the PV inverter and/or interference.

Figure 8 shows a frequency analysis of the dc line when an arc is being generated. By comparing Figure 8 to Figure 7, it can be seen that when an arc is generated, the noise floor increases over a range of frequencies.

Figure 10 shows the arc detection GUI monitor monitoring the dc line when an arc is not being generated. It shows that no noise is being generated. These results were achieved with an ADC sampling frequency of 512 kHz and no switching noise frequency (the comb filter was off).

Figure 11 shows the arc detection GUI monitor monitoring the dc line when an arc is being generated. It can be seen that the noise floor has increased across 50 FFT bins. These results were achieved with an ADC sampling frequency of 512 kHz and no switching noise frequency (the comb filter was off).

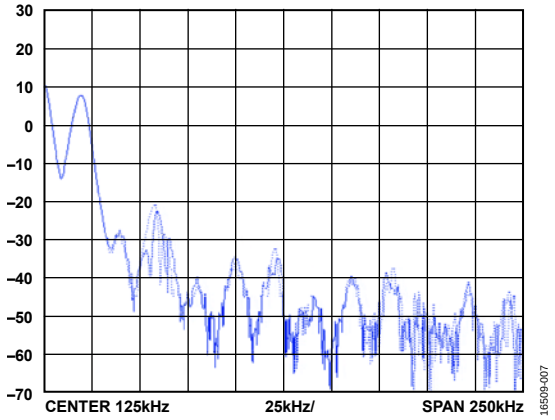

Figure 7. Frequency Spectrum DC Line with No Arcs Occurring

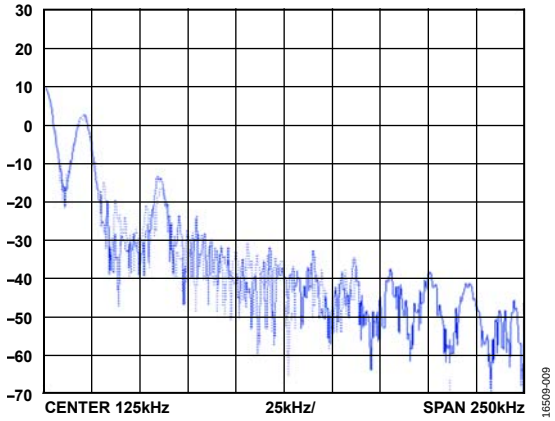

Figure 8. Frequency Spectrum DC Line with an Arc Occurring

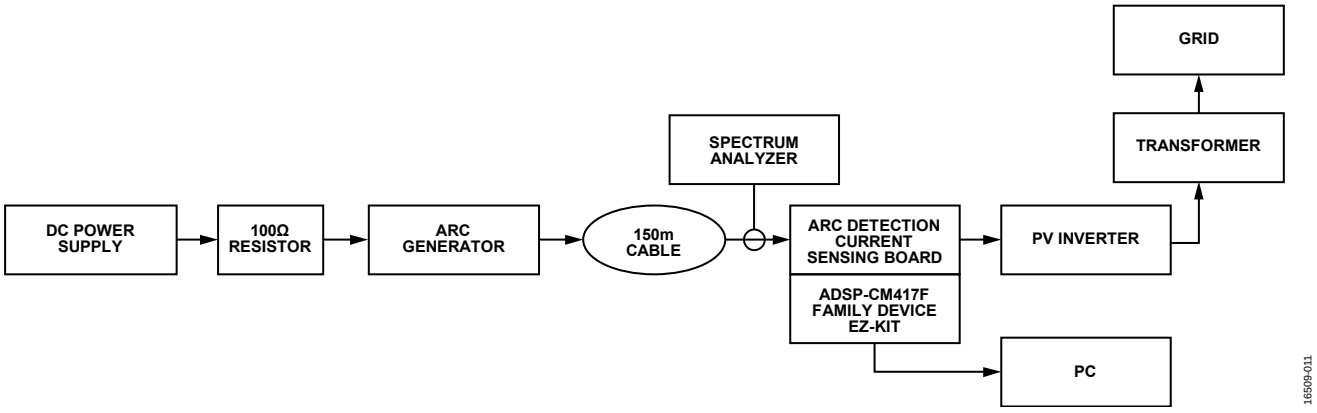

Figure 9. Block Diagram of Arc Detection Testing Setup

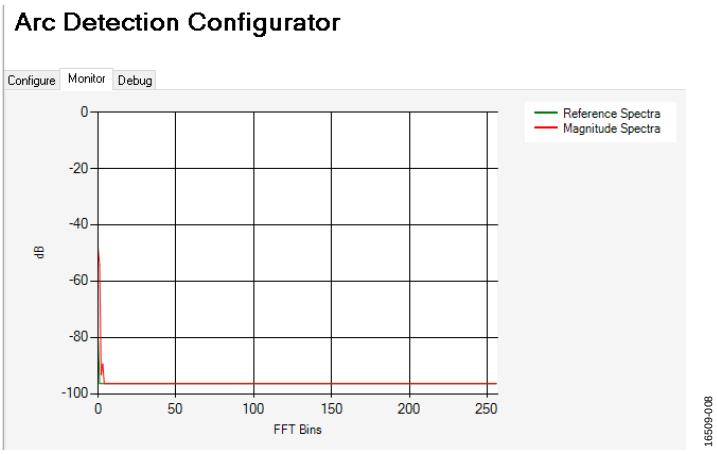

Figure 10. Arc Detection Configurator GUI Frequency Analysis of DC Line with No Arcs Occurring

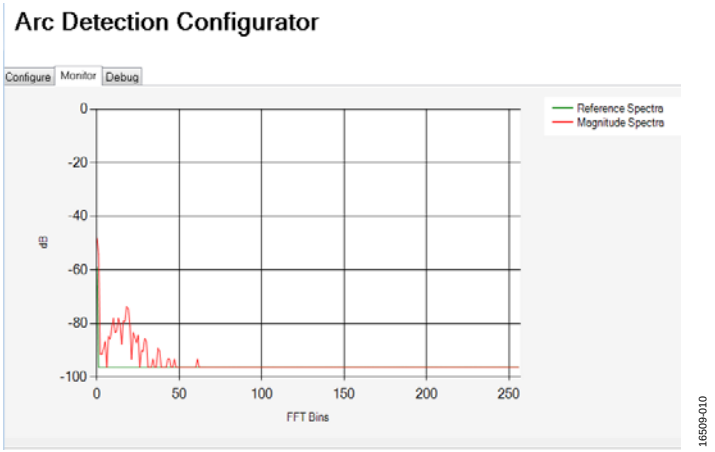

Figure 11. Arc Detection Configurator GUI Frequency Analysis of DC Line with an Arc Occurring