General-Purpose TigerSHARC® Processor

Highest Performance Floating-Point Processor

Key Features

Static Superscalar Architecture Optimized for High Throughput Floating-Point Applications

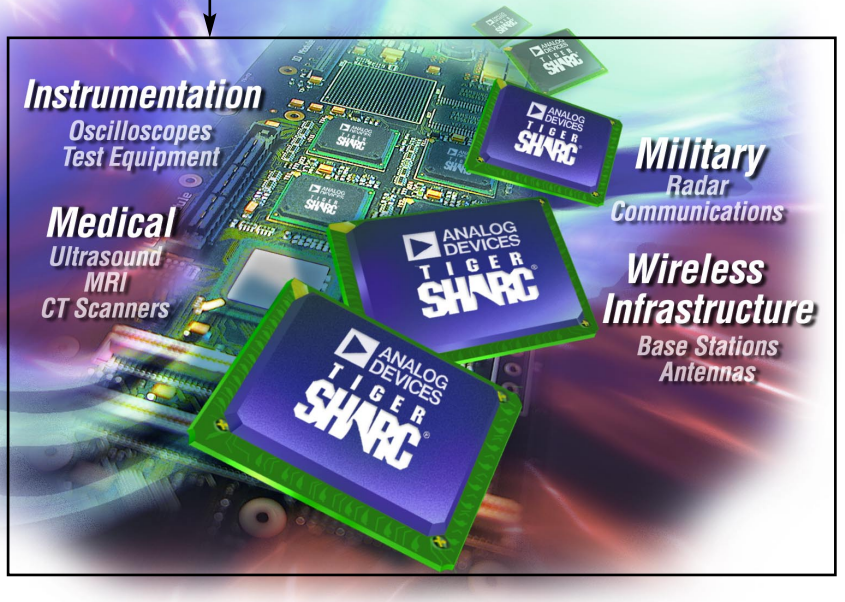
- Eight 16-bit MACs/cycle with 40-bit accumulation
- Two 32-bit MACs/cycle with 80-bit accumulation
- Specific support for Viterbi decoding through the implementation of Add, Compare, Select (ACS) sequencing
- Add-subtract instruction and bit reversal in hardware for FFTs
- Two 32-bit IEEE floating-point MACs/cycle

Highly Integrated

- 6 Mbit on-chip SRAM
- Glueless multiprocessing
- Four link ports—1 Gbyte/sec transfer rate
- 64-bit external port—800 Mbytes/sec
- 14 DMA channels

Flexible Programming in Assembly and C Languages

- User-defined partitioning between program and data memory
- 128 general-purpose registers
- Algebraic assembly language syntax
- Optimizing C compiler
- VisualDSP++™ tools support
- Single-instruction, multiple-data (SIMD) instructions, or direct issue capability
- Predicated execution
- Fully interruptible with full computation performance



The TigerSHARC Processsor Executes 2.4 Billion 40-bit MACs Per Second and Achieves the World's Highest Floating-Point DSP Performance.

A Breakthrough Architecture

The ADSP-TS101S general-purpose TigerSHARC Processor targets numerous signal processing applications requiring massive data throughput and provides the industry's highest floating-point performance. These applications include but are not limited to wireless infrastructure equipment and power sensitive embedded applications such as military hardware, medical equipment, industrial instrumentation, and software-defined radios.

On one piece of silicon, ADI has combined the 300 MHz TigerSHARC core, 6 Mbits of SRAM memory, a 14-channel zero-overhead DMA engine, and I/O processing capable of an aggregate throughput of 1.8 Gbytes. This positions the TigerSHARC Processor as the best in class in terms of MFLOPS delivered per watt, per dollar, and per square millimeter of silicon area. Equally important, the two types of integrated multiprocessing support (link ports and a cluster bus) enable glueless scalability. This means the TigerSHARC Processor will gluelessly scale up to eight devices on the cluster with global memory. Four on-board link ports provide a high bandwidth point-to-point connection that is complementary to the cluster multiprocessing.

ANALOG DEVICES

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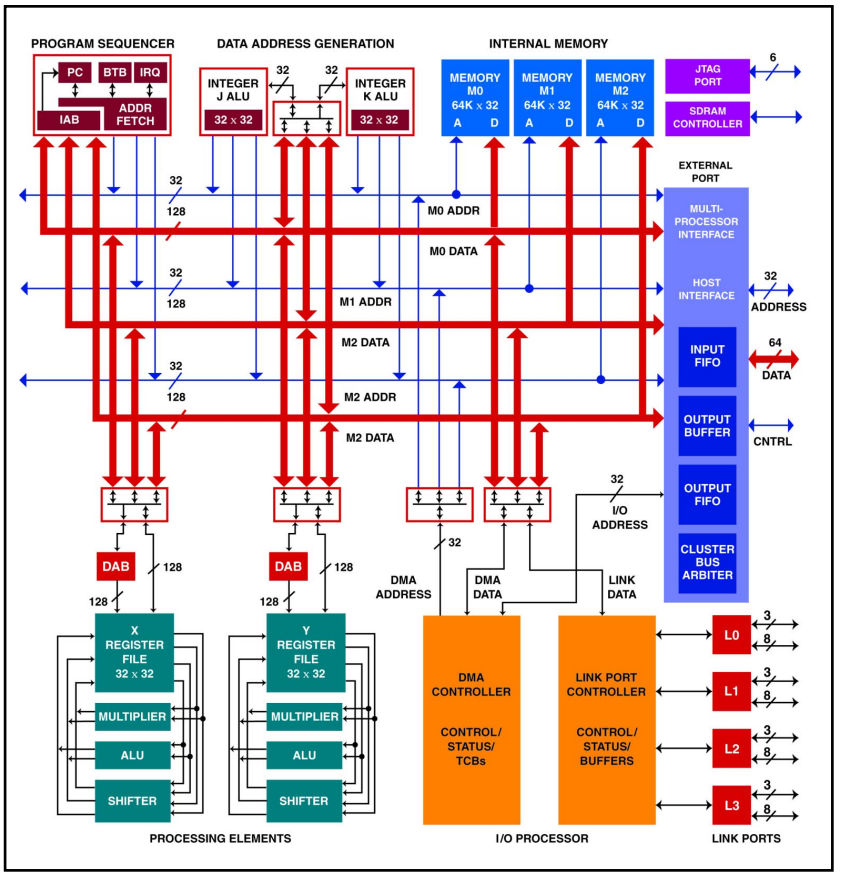
The TigerSHARC Processor embodies a breakthrough architecture that boasts native support of 1-, 8-, 16-, and 32-bit fixed-point and floating-point data types on a single chip. Each of these data types is critical in many of the various applications where the TigerSHARC Processor is used. One example of this is in 3G wireless applications. In this case, the support of multiple data types, as well as the enhanced instruction set, matches algorithm requirements and allows for a software radio approach. Chip rate and symbol rate tasks found within the 3G baseband signal processing can be accomplished in the TigerSHARC Processor. The soft transceiver approach to baseband signal processing provides a level of flexibility unmatched by alternative approaches requiring costly external ASIC or FPGA devices. The end result is that OEM manufacturers can offer efficient and flexible solutions using a general-purpose processor while providing significant systems cost reduction.

The glueless scalability of TigerSHARC Processors enable common building blocks and even common design implementations to be used across programs. A complete set of TigerSHARC Processor documentation along with VisualDSP++ integrated development tools are available today enabling all aspects of DSP hardware and software development.



TigerSHARC Processor Block Diagram

Static Superscalar Architecture

The TigerSHARC architecture blends best practices in microprocessor design to enable the highest performance programmable DSP for real-time systems.

The TigerSHARC Processor employs a static superscalar architecture. It incorporates many aspects of conventional superscalar processors, including a load/store architecture, branch prediction, and a large interlocked register file. Up to four instructions can be executed in parallel in each cycle. The term “static superscalar” is applied because instruction-level parallelism is determined prior to runtime and encoded in the program.

It is the instruction parallelism that allows the reduction in overall cycle count required to perform 3G-related functions such as channel decoding, despreading, and path search.

Additionally, the TigerSHARC Processor has the capability of supporting single-instruction, multiple-data (SIMD) operations through the use of both computational blocks in parallel and SIMD-specific computations. The programmer has the option of directing both computation blocks to operate on the same data (broadcast distribution) or different data (merged distribution).

All the registers are interlocked, supporting a simple programming model that is independent of the implementation latencies and is fully interruptible. Branch prediction is supported via a 128-bit entry branch target buffer (BTB) that reduces latency.

Eight MACs/Cycle

There are two computation blocks (processing blocks X and Y) in the ADSP-TS101S architecture, each containing a multiplier, ALU, and a 64-bit shifter. With the resources in these blocks, it is possible to execute in a single cycle eight 40-bit MACs on 16-bit data, two 40-bit MACs on 16-bit complex data, or two 80-bit MACs on 32-bit data. With 8-bit data types, the architecture executes 16 operations per cycle.

The TigerSHARC Processor is a register-based load/store architecture in which each computation block has access to a fully orthogonal 32-word register file.

TigerSHARC Processor Benchmarks

Peak Rates at 300 MHz		
1-Bit Performance	19.2 Billion MACs/Second	
16-Bit Performance	2.4 Billion MACs/Second	
32-Bit Fixed-Point Performance	600 Million MACs/Second	
32-Bit Floating-Point Performance	1,800 MFLOPS	
16-Bit Algorithms	**Execution Time at 300 MHz**	**Clock Cycles**
256-Point Complex FFT (Radix 2)	3.7 µs	1,100
50-Tap FIR on 1024 Input	24.0 µs	7,200
Single FIR MAC	0.47 ns	0.14
Single Complex FIR MAC	1.9 ns	0.57
32-Bit Algorithms	**Execution Time at 300 MHz**	**Clock Cycles**
1024-Point Complex FFT (Radix 2)	32.5 µs	9,750
50-Tap FIR on 1024 Input	91.7 µs	27,500
Single FIR MAC	1.8 ns	0.54
Single Complex FIR MAC	7.2 ns	2.16

Memory Architecture

The ADSP-TS101S features a short vector memory architecture organized internally in three 128-bit wide banks. Quad (four words, 32 bits each), long (two words, 32 bits each), and normal word accesses move data from the memory banks to the register files for operations. In a given cycle, four 32-bit instruction words can be fetched and 256 bits of data can be loaded to the register files or stored into memory. Data in 1-, 8-, 16-, and 32-bit words can be stored in contiguous, packed memory. Internal and external memories are organized in a unified memory map. The partition between program and data memory is completely user-determined. The internal memory bandwidth for data and instructions is 12 Gbytes/second.

Integrated I/O Capabilities

The ADSP-TS101S integrates many features, including a 32- or 64-bit external port, a 14-channel DMA (direct memory access) controller, and four bidirectional link ports, all aimed at providing unparalleled interface capabilities without the use of any additional external glue logic. The external port enables interfacing to a host processor, off-chip memory, additional TigerSHARC Processors, and other memory-mapped peripherals.

The DMA controller found on the ADSP-TS101S operates independently and invisibly to the processor core, allowing DMA operations to occur while the TigerSHARC core continues to execute program instructions. In the case of large-scale applications that require a number of TigerSHARC Processors, the four patented bidirectional link ports permit direct chip-to-chip connections without the need for complex external circuitry.

Instruction Set Summary

The ADSP-TS101S instruction set directly supports all arithmetic types, including signed, unsigned, fractional, and integer data type; and there is optional saturation (clipping) arithmetic for all cases. Specific instructions have also been added to the TigerSHARC core to enable software-based implementations of functions traditionally done in hardware. These include a special complex MAC operation for chip rate processing and an Add-Compare-Select (ACS) operation for channel decoding algorithms. With these instructions, the ADSP-TS101S provides the performance of an ASIC with the flexibility of a DSP for both the symbol rate and chip rate processing found in 3G baseband signal processing applications.

Development Tools and Third-Party Developers

The TigerSHARC Processor is supported by CROSSCORE™ Analog Devices' wide range of DSP software and hardware development tools. The CROSSCORE components include the VisualDSP++ software development environment, EZ-KIT Lite™ evaluation systems, and Emulators for rapid on-chip debugging. VisualDSP++ is an integrated software development environment, allowing for fast and easy development, debug, and deployment. Emulators are available for PCI and USB host platforms. The EZ-KIT Lite evaluation system provides an easy way to investigate the power of the Analog Devices family of processors and begin to develop applications.

The TigerSHARC Processor architecture is supported by ADI's third-party network, the DSP Collaborative™ DSP Collaborative developers help shorten customer time-to-market by providing products and services such as completely populated TigerSHARC Processor design hardware, algorithms/source code, reference designs, and consultant services. To see a listing of TigerSHARC Processor third-party developers and their product offerings, visit *www.analog.com/tigersharc*.

TigerSHARC Processor General-Purpose Toolbox

Development Can Start Right Away

Accelerate the design and development cycle of wireless base station applications. Available today are DSP code generation tools, 3G library software, multiprocessor development boards, and third-party products to help expedite wireless application development and reduce the time it takes to bring products to market.

CROSSCORE

The CROSSCORE components include the VisualDSP++ software development and debugging environment, the EZ-KIT Lite evaluation systems, and Emulators.

TigerSHARC EZ-KIT Lite

The ADSP-TS101S EZ-KIT Lite provides developers with a cost-effective method for initial evaluation of the TigerSHARC Processor family. The EZ-KIT Lite includes two ADSP-TS101S processors on the desktop evaluation board and fundamental debugging software to facilitate architecture evaluations via a USB-based, PC-hosted tool set. With this EZ-KIT Lite, users can learn more about ADI's ADSP-TS101S hardware and software development and prototype applications. The ADSP-TS101S EZ-KIT Lite provides an evaluation suite of the VisualDSP++ development environment with the C/C++ compiler, assembler, and linker. All software tools are limited for use with the EZ-KIT Lite.

3G Physical Layer Library Software

The TigerSHARC Processor 3G Library contains complete functionality for Layer 1 baseband processing. The latest versions of WBCDMA (3GPP), CDMA2000 (3GPP2), and TDSCDMA standards are all supported. Functionality is programmed in both C and optimized TigerSHARC assembly with a C interface. Reference designs for IP-based functions are also included.

VHDL/Verilog Link Port Interface Model

The Link Port Interface Model is intended to simplify the FPGA design process when interfacing TigerSHARC link ports to XILINX FPGAs. The model is written in IEEE standard VHDL and is compatible with Virtex E and Virtex II family devices.

Multiprocessor System Analysis

A multiprocessor system analysis of TigerSHARC cluster bus loading and frequency of operation provides guidelines for system implementation. Details include maximum frequency of operation for an 8 TigerSHARC Processor system including a host and memory along with design, termination, and layout recommendations.

Board Design Schematics

Example schematics illustrate TigerSHARC Processor connectivity and system implementation for a multiprocessor board.

IBIS Models

I/O Buffer Information Specification (IBIS) models are provided for the ADSP-TS101S as a behavioral model of I/O. This is useful for transmission line simulation of a TigerSHARC digital system. It can be used with various commercially available system simulation packages for signal integrity analysis of TigerSHARC system designs.

Third-Party Products

A number of third-party board level products, software, and engineering services are available today from industry leading companies, including:

- Delphi Communication Systems
- Transtech DSP
- Bittware
- Toracomm
- PA Consulting Group
- Enea OSE Systems
- Plexus

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