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Estimating Power for ADSP-TS201S TigerSHARC® Processors

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Rev 2 – October 16, 2006

Introduction

This EE-Note discusses techniques for estimating the power consumption for an ADSP-TS201S TigerSHARC® processor. This document assists board designers by providing data and recommendations, allowing them to estimate their budgets for power supply and thermal relief designs for a given system. An Excel spreadsheet also accompanies this document to assist in power estimation (refer to [Appendix C](#) for more information.). The data provided within this document applies to silicon revision 2.0 only; contact Analog Devices for more information on data pertaining to older ADSP-TS201S silicon revisions.

ADSP-TS201S processors are members of the ultra-high-performance, static superscalar, 32-bit TigerSHARC processor family. This processor is offered in two different speed grades, which allow the core to operate at a maximum clock frequency of either 500 (-050 speed grade) or 600 MHz (-060 speed grade). The processor also requires three separate external voltage supplies, as shown in [Table 1](#).

ADSP-TS201S Voltage Domain	Core Clock Rate 500 MHz (-050)	Core Clock Rate 600 MHz (-060)
V_{DD}	1.05V +/- 5%	1.20V +/- 5%
V_{DD_DRAM}	1.50V +/- 5%	1.60V +/- 5%
V_{DD_IO}	2.50V +/- 5%	2.50V +/- 5%

Table 1. Voltage Supply Requirements

Power Consumption

The total power consumed by the ADSP-TS201S device is the sum of the power consumed on each of the voltage domains (V_{DD} , V_{DD_DRAM} , V_{DD_IO}) of the processor. This sum consists of the internal core logic, the I/O logic, the internal DRAM, and the related circuitry for each of these domains.

The following sections explain how to derive power numbers for a given system based on the different internal dynamic activity levels (instruction, data, and DMA sequence), I/O activity, and environmental operating conditions. Details describing the activity levels are also provided.

V_{DD} Current Consumption

The total internal current consumption (I_{DD}) on the V_{DD} supply is the sum of the static and dynamic components of the processor.

Since the dynamic activity of the processor is dependent on the instruction execution sequence of the application code and the data operands involved, a good understanding of the instruction execution is important in estimating the dynamic current (I_{DD_DYN}) consumed by the processor core. The dynamic current consumption can be calculated by multiplying the weighted average of the different activity levels by a baseline dynamic current characteristic. For details on this

characteristic, see *IDD_BASELINE Dynamic Current Characteristic Graph*.

A precise understanding of the application program can be achieved by profiling the program execution (or by accurately estimating the average code activity levels for specific portions of the program). The goal of profiling is to determine the percentage of execution time each activity level occupies. These dynamic core activity levels are explained in detail in the following section.

Internal Dynamic Activity Level Definitions

The following definitions apply to the internal dynamic activity levels (I_{DD_DYN}) shown in Table 2. Excluding the I_{DD_DMA} and I_{DD_IDLE} activity levels, each activity level contains no stall cycles, and therefore represents worst-case processor core activity.

- **IDD_CLU_HIGH** – Sustained high activity operations of the CLU. This activity level is as the following instructions executing in parallel per instruction cycle: A SIMD cross correlations with transfer trellis register (dual operation, CLU) instruction (*XCORRS*); A SIMD complex multiply-accumulate with transfer MR register (dual operation, short word) instruction; two parallel 128-bit *SDAB* data fetches. The data fetched and operated on are random; the data and instructions reside in independent memory segments to allow the highest data throughput and to ensure that no stall cycles are incurred. This $I_{DD_CLU_HIGH}$ activity level also includes a concurrent external port DMA sequence, as described in the I_{DD_DMA} activity level.
- **IDD_CLU_TYP** – Sustained typical activity operations of the CLU. This activity level is defined as the following instructions executing in parallel per instruction cycle: A SIMD permute (byte word) instruction; Two parallel 128-bit *SDAB* data fetches; A “NOP;” instruction. The data fetched and operated on are random; the data and

instructions reside in independent memory segments to allow the highest data throughput and to ensure that no stall cycles are incurred. This $I_{DD_CLU_TYP}$ activity level also includes a concurrent external port DMA sequence, as described in the I_{DD_DMA} activity level.

- **IDD_CLU_LOW** – Sustained low activity operations of the CLU are defined as the following instructions executing in parallel per instruction cycle: A SIMD Trellis Function of the Form $STR_{sd} = TMAX(TR_{md} + Rmq_h, TR_{nd} + Rmq_l)$; (*TMAX*) instruction; A SIMD long-word shifter rotate instruction; Two parallel 128-bit *SDAB* data fetches. The data fetched and operated on are random; the data and instructions reside in independent memory segments to allow the highest data throughput and to ensure that no stall cycles are incurred. This $I_{DD_CLU_LOW}$ activity level also includes a concurrent external port DMA sequence, as described in the I_{DD_DMA} activity level.
- **IDD_FFT** – Sustained high activity floating point operations of the computational units of the processor core. This activity level is defined as a SIMD "Add/Subtract (Dual Operation, Floating-Point)" instruction executing in parallel along with a SIMD floating-point multiply. Also executing in parallel are one of the following instructions: Two Dual Register Merged Read Accesses (via the circular buffer instruction option); A Dual Register Merged Read Access in parallel with a Dual Register Merged Write Access (both via the circular buffer instruction option); or a Dual Register Merged Write Access (via the circular buffer instruction option) in parallel with a “NOP;” instruction. The data fetched and operated on are random; data and instructions reside in independent memory segments to allow the highest data throughput and to ensure that no stall cycles are incurred. This I_{DD_FFT} activity

level also includes a concurrent external port DMA sequence, as described in the I_{DD_DMA} activity level.

- **IDD_COMPUTE_HIGH** – Sustained high activity operations of the computational units of the processor core. This activity level is defined as the following instructions executing in parallel per instruction cycle: A SIMD Multiply (Quad-Short Word); A SIMD Add (Quad-Short Word); Two Dual Register Merged Read Accesses (via the circular buffer instruction option). The data fetched and operated on are random; data and instructions reside in independent memory segments to allow the highest data throughput and to ensure that no stall cycles are incurred. This $I_{DD_COMPUTE_HIGH}$ activity level definition also includes a concurrent external port DMA sequence, as described in the I_{DD_DMA} activity level definition below.
- **IDD_COMPUTE_TYP** – Sustained typical activity operations of the computational units of the processor core. This activity level is defined as the following instructions executing in parallel per instruction cycle: A SIMD Multiply (Quad-Short Word); Two Dual Register Merged Read Accesses (via the circular buffer instruction option). The data fetched and operated on are random; data and instructions reside in independent memory segments to allow the highest data throughput and to ensure that no stall cycles are incurred. This $I_{DD_COMPUTE_TYP}$ activity level also includes a concurrent external port DMA sequence, as described in the I_{DD_DMA} activity level.
- **IDD_CTRL** – Control activity is defined as a continuous decision-making sequence of instructions and predicted branches. The branch prediction is deliberately set to be incorrect 50% of the time to allow for equal distribution. This I_{DD_CTRL} activity level definition also includes the DMA activity

level as described in the I_{DD_DMA} activity level.

- **IDD_DMA** – DMA activity is defined as a single-channel external port DMA from external memory to internal memory, using quad-word transfers of 32 words total. The DMA is chained to itself (in order to run continuously), and does not use interrupts. After initializing the DMA sequence, the processor core is not involved; it executes the “IDLE; ;” instruction only.
- **IDD_IDLE** – V_{DD} supply current for idle activity. This activity level is defined as the processor core executing an “IDLE; ;” instruction only, with no active DMAs or interrupts.

Estimating Dynamic Current Consumption

Two steps are involved in estimating the dynamic current consumption on the V_{DD} domain. The first step determines the dynamic baseline current. The second step determines the percentage of activity for each of the discrete vectors with respect to the entire application code.

$I_{DD_BASELINE}$ Dynamic Current Characteristic Graph

The ADSP-TS201S $I_{DD_BASELINE}$ dynamic current characteristic graph is shown in Figure 1. (Appendix B contains a larger image of this graph.) Each line in the graph represents a baseline I_{DD} dynamic internal current value for a specific given voltage.

To calculate the baseline dynamic current ($I_{DD_BASELINE}$) on the V_{DD} voltage domain, take the line on the graph that represents the operating voltage of the processor and find the point on this line for the specific operating frequency of each processor in the system. From this point on the curve, the baseline value for the dynamic current can be determined by finding its point of

intersection with the vertical axis on the left side labeled “Dynamic Current”.

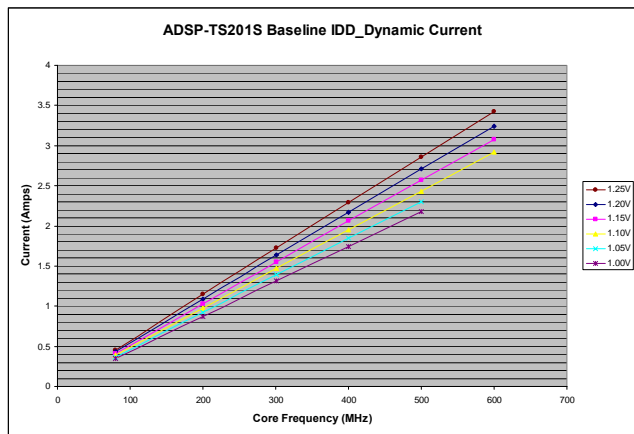


Figure 1. Dynamic Baseline Current Characteristic

Assume that the TigerSHARC processors in the example system are operating at 500 MHz at 1.05 V. From the graph in Figure 1, these two parameters will yield a result of 2.30 A for the dynamic baseline current.

From the activity level definitions described in *Internal Dynamic Activity Level Definitions*, and after profiling the application program, the percentage of overall execution time for each activity level can be determined.

Table 2 lists the scale factor for each activity level, which are used to estimate the dynamic current (I_{DD_DYN}) for a specific application.

Power Vector Name	Activity Factor Value
$I_{DD_CLU_HIGH}$	1.18
$I_{DD_CLU_TYP}$	0.93
$I_{DD_CLU_LOW}$	0.75
I_{DD_FFT}	1.04
$I_{DD_COMPUTE_HIGH}$	1.00
$I_{DD_COMPUTE_TYP}$	0.88
I_{DD_CTRL}	0.47
I_{DD_DMA}	0.25
I_{DD_IDLE}	0.23

Table 2. Internal Dynamic Core Current (I_{DD_DYN})

The processor core dynamic current can be calculated by multiplying the value of the dynamic baseline current by the activity factor value for each discrete vector, and then multiplying this result by the percentage of time spent for each vector in the application program. This step is shown in Equation 1.

$$\begin{aligned}
 & (\% I_{DD_CLU_HIGH} \times I_{DD_CLU_HIGH} \text{ Activity Factor} \times I_{DD_BASELINE}) \\
 & (\% I_{DD_CLU_TYP} \times I_{DD_CLU_TYP} \text{ Activity Factor} \times I_{DD_BASELINE}) \\
 & (\% I_{DD_CLU_LOW} \times I_{DD_CLU_LOW} \text{ Activity Factor} \times I_{DD_BASELINE}) \\
 & (\% I_{DD_FFT} \times I_{DD_FFT} \text{ Activity Factor} \times I_{DD_BASELINE}) \\
 & (\% I_{DD_COMPUTE_HIGH} \times I_{DD_COMPUTE_HIGH} \text{ Activity Factor} \times I_{DD_BASELINE}) \\
 & (\% I_{DD_COMPUTE_TYP} \times I_{DD_COMPUTE_TYP} \text{ Activity Factor} \times I_{DD_BASELINE}) \\
 & (\% I_{DD_CTRL} \times I_{DD_CTRL} \text{ Activity Factor} \times I_{DD_BASELINE}) \\
 & (\% I_{DD_DMA} \times I_{DD_DMA} \text{ Activity Factor} \times I_{DD_BASELINE}) \\
 & + (\% I_{DD_IDLE} \times I_{DD_IDLE} \text{ Activity Factor} \times I_{DD_BASELINE}) \\
 & = \text{Total Weighted Average Dynamic Current for } V_{DD} \\
 & = I_{DD_DYN}
 \end{aligned}$$

Equation 1. I_{DD_DYN} Core Dynamic Current

Example: Assume that for a given system, the profile of the application code is as follows:

- 5% $I_{DD_CLU_HIGH}$ Activity Level
- 5% $I_{DD_CLU_TYP}$ Activity Level
- 10% $I_{DD_CLU_LOW}$ Activity Level
- 25% I_{DD_FFT} Activity Level
- 25% $I_{DD_COMPUTE_HIGH}$ Activity Level
- 0% $I_{DD_COMPUTE_TYP}$ Activity Level
- 30% I_{DD_CTRL} Activity Level
- 0% I_{DD_DMA} Activity Level
- 0% I_{DD_IDLE} Activity Level

Example 1. Internal System Activity Level

From the percentages of this example, the core dynamic current (I_{DD_DYN}) for a single processor can be calculated using Equation 1 as follows:

$$\begin{aligned}
 & (5\% \times 1.18 \times 2.30) \\
 & (5\% \times 0.93 \times 2.30) \\
 & (10\% \times 0.75 \times 2.30) \\
 & (25\% \times 1.04 \times 2.30) \\
 & (25\% \times 1.00 \times 2.30) \\
 & + (30\% \times 0.47 \times 2.30) \\
 & = 1.92 \text{ A}
 \end{aligned}$$

Example 2. Total Estimated Dynamic Current

Therefore, the total estimated dynamic current on the V_{DD} supply is 1.92 A.

I_{DD_STATIC} Baseline Characteristic Curve

The I_{DD_STATIC} baseline characteristic curve is used to calculate the static power on the V_{DD} voltage domain. Because the static power consumed on V_{DD} is a function of temperature and voltage (and *not* a function of frequency), this static power level does not need to be calculated for each discrete internal power vector definition. The static power is simply added to the total estimated dynamic current value (I_{DD_DYN}), which was calculated earlier.

Figure 2 shows the static baseline current for typical devices. A typical device is defined as a device whose static current consumption lies at the mid-point of the probability density distribution of the entire population of devices. The curves in Figure 2 can be used to calculate the statistical average static power for all of the ADSP-TS201S devices in a system.

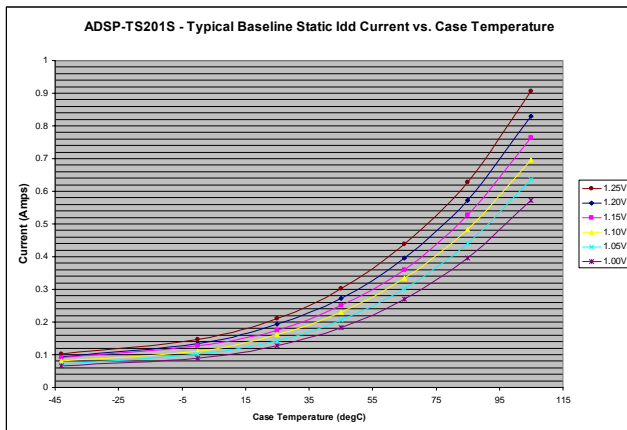


Figure 2. Typical Static Current Characteristic Graph

Each line in Figure 2 represents a baseline static internal current value at a given voltage. To calculate the total static current (I_{DD_STATIC}) on the V_{DD} voltage domain, take the line on the graph that represents the voltage of the device and find the point on this line for the specific case

temperature at which the processors in the system will operate. From this point on the curve, the value for the baseline static current can be estimated by finding the point of intersection on the vertical axis on the left side of the graph labeled, “Static Current”.

For the example system, assume that all of the processor cores operate at $V_{DD} = 1.05$ V, and that due to system conditions, the maximum value for T_{CASE} is 25°C. Therefore, from these operating conditions, Figure 2 shows that the static current consumed on the V_{DD} voltage domain is 0.14 A.

Total Estimated Core Current (I_{DD})

To find the total I_{DD} current consumption for each processor in a specific system, simply add the total dynamic and static current components on the V_{DD} supply domain, as shown in Equation 2:

$$I_{DD} = I_{DD_DYN} + I_{DD_STATIC}$$

Equation 2. Total I_{DD} Current

For the example system, calculate the total I_{DD} current as follows:

$$\begin{aligned} I_{DD} &= I_{DD_DYN} + I_{DD_STATIC} \\ &= 1.92 \text{ A} + 0.14 \text{ A} \\ &= 2.06 \text{ A} \end{aligned}$$

Example 3. Total I_{DD} Current Estimation

V_{DD_A} Current Consumption

Each ADSP-TS201S processor includes an analog phase lock loop (PLL) and related circuitry to provide clock signals to the core and peripheral logic. This circuitry is powered from an external source that supplies power to the V_{DD_A} pins of the processor. Since this logic is always active, it must be considered when calculating the overall power consumed by each processor core.

There are two different speed grades (500 and 600 MHz) for the ADSP-TS201S processor, as well as two specific V_{DD_A} voltage requirements

for each operating frequency. Thus, there are two different values for the typical and maximum I_{DD_A} current for each speed grade, respectively.

For 500 MHz speed grade devices, the typical current ($I_{DD_A (TYP)}$) consumed by the analog circuitry of each processor is 20 mA. The maximum I_{DD_A} current ($I_{DD_A (MAX)}$) for each processor at 500 MHz is 50 mA.

$$I_{DD_A(TYP)} = 20 \text{ mA}$$

Equation 3. Typical 500 MHz I_{DD_A} Current

$$I_{DD_A(MAX)} = 50 \text{ mA}$$

Equation 4. Maximum 500 MHz I_{DD_A} Current

For 600 MHz speed grade devices, the I_{DD_A} current increases slightly due to the increased operating voltage of the device. The typical current ($I_{DD_A (TYP)}$) consumed by the analog circuitry of each processor is 25 mA. The maximum I_{DD_A} current ($I_{DD_A (MAX)}$) for each processor at 600 MHz is 55 mA.

$$I_{DD_A(TYP)} = 25 \text{ mA}$$

Equation 5. Typical 600 MHz I_{DD_A} Current

$$I_{DD_A(MAX)} = 55 \text{ mA}$$

Equation 6. Maximum 600 MHz I_{DD_A} Current

Total Estimated Internal Power (P_{DD})

Since V_{DD_A} is derived from V_{DD} , the total estimated power (P_{DD}) consumed on the V_{DD} voltage domain can be calculated as follows:

$$P_{DD} = V_{DD} \times (I_{DD} + I_{DD_A(TYP)})$$

Equation 7. Total Internal Average Power Calculation

For the example system, calculate P_{DD} using Equation 7 to determine a total internal average power as shown in Example 4:

$$\begin{aligned} P_{DD} &= V_{DD} \times (I_{DD} + I_{DD_A(TYP)}) \\ &= 1.05 \text{ V} \times (2.06 \text{ A} + 0.02 \text{ A}) \\ &= 2.18 \text{ W} \end{aligned}$$

Example 4. Total Internal Average Power

V_{DD_DRAM} Current Consumption

The internal DRAM of the ADSP-TS201S processor *must* be supplied from an external voltage source.

The voltage requirement for the V_{DD_DRAM} supply is dependent upon the operating frequency of the processor. For 500 MHz speed grade devices (-050), the V_{DD_DRAM} voltage domain requires a 1.50 V supply. For 600 MHz devices (-060), the internal DRAM should be supplied with 1.60 V.

For a 500 MHz device, the typical current consumed by the internal DRAM ($I_{DD_DRAM (TYP)}$) is 250 mA. This value represents the current consumed during typical core and I/O activity using the internal DRAM. The typical power consumed by the internal DRAM ($P_{DD_DRAM (TYP)}$) of the processor is 375 mW.

$$I_{DD_DRAM(TYP)} = 250 \text{ mA}$$

Equation 8. Typical I_{DD_DRAM} Consumption (500 MHz)

$$\begin{aligned} P_{DD_DRAM(TYP)} &= V_{DD_DRAM} \times I_{DD_DRAM(TYP)} \\ &= 1.5 \text{ V} \times 250 \text{ mA} \\ &= 375 \text{ mW} \end{aligned}$$

Example 5. Typical P_{DD_DRAM} Consumption (500 MHz)

The total maximum current consumed by the internal DRAM of a 500 MHz device ($I_{DD_DRAM (MAX)}$) is 400 mA. Therefore, the total maximum power consumed by the internal DRAM ($P_{DD_DRAM (MAX)}$) of the processor is 600 mW.

$$I_{DD_DRAM (MAX)} = 400 \text{ mA}$$

Equation 9. Maximum I_{DD_DRAM} Consumption (500 MHz)

$$\begin{aligned} P_{DD_DRAM (MAX)} &= V_{DD_DRAM} \times I_{DD_DRAM (MAX)} \\ &= 1.5 \text{ V} \times 400 \text{ mA} \\ &= 600 \text{ mW} \end{aligned}$$

Example 6. Maximum P_{DD_DRAM} Consumption (500 MHz)

For a 600 MHz device, the typical current consumed by the internal DRAM ($I_{DD_DRAM (TYP)}$) is 280 mA. This value represents the current consumed during typical core and I/O activity using the internal DRAM. The typical power consumed by the internal DRAM ($P_{DD_DRAM (TYP)}$) of the processor is 448 mW.

$$I_{DD_DRAM (TYP)} = 280 \text{ mA}$$

Equation 10. Typical I_{DD_DRAM} Consumption (600 MHz)

$$\begin{aligned} P_{DD_DRAM (TYP)} &= V_{DD_DRAM} \times I_{DD_DRAM (TYP)} \\ &= 1.6 \text{ V} \times 280 \text{ mA} \\ &= 448 \text{ mW} \end{aligned}$$

Example 7. Typical P_{DD_DRAM} Consumption (600 MHz)

The total maximum current consumed by the internal DRAM of a 600 MHz device ($I_{DD_DRAM (MAX)}$) is 430 mA. Therefore, the total maximum power consumed by the internal DRAM ($P_{DD_DRAM (MAX)}$) of the processor is 688 mW.

$$I_{DD_DRAM (MAX)} = 430 \text{ mA}$$

Equation 11. Maximum I_{DD_DRAM} Consumption (600 MHz)

$$\begin{aligned} P_{DD_DRAM (MAX)} &= V_{DD_DRAM} \times I_{DD_DRAM (MAX)} \\ &= 1.6 \text{ V} \times 430 \text{ mA} \\ &= 688 \text{ mW} \end{aligned}$$

Example 8. Maximum P_{DD_DRAM} Consumption (600 MHz)

V_{DD_IO} Current Consumption

The total external power consumption (P_{DD_IO}) on the V_{DD_IO} voltage domain is comprised of three components: the External Port, the Link Ports, and the associated circuitry for the external pins, output drivers, and control logic. Also, each of these three current components are comprised of static and dynamic sub-components.

External Port Dynamic Current Estimation

The dynamic current consumption of the External Port on the V_{DD_IO} supply is caused by the switching of the output pins and is system dependent. For each unique group of pins, the magnitude of power consumed depends on:

1. The number of output pins that switch during each cycle, O
2. The load capacitance of the output pins, C
3. Their voltage swing, V_{DD_IO}
4. The maximum frequency at which the pins can switch, f

The load capacitance should include the input capacitance of each connected device as well as the processor's own input capacitance (C_{IN}). For additional accuracy, trace capacitance should be included, if possible. The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum frequency of $\frac{1}{2}$ SCLK.

Note that the total power measured on the V_{DD_IO} supply domain is calculated on a total system basis with regard to the dynamic External Port activity; it is not a cumulative result from the calculation of each processor in the system, since only one processor can be the bus master at any given time.

Equation 12 shows how to calculate the average dynamic current for the address, data, and control pins on the V_{DD_IO} supply that is consumed by the External Port, given the above four parameters:

$$I_{DD_IO_EP_DYN} = O \times C \times V_{DD_IO} \times f$$

Equation 12. External Port Average Dynamic Current

Example: Calculate the average current consumed by the External Port pins on the V_{DD_IO} supply with the following assumptions:

- The example system consists of four ADSP-TS201S processors with one bank of shared external memory (64-bit), where $C_{IN} = 3$ pF per TigerSHARC device.
- Two $1\text{ M} \times 32$ -bit SDRAM chips are used, each with a load of 5 pF per pin (trace capacitance is neglected for this example).
- Continuous burst of quad-word (128-bit) writes occur every cycle at a rate of SCLK, with 50% of the data pins switching (this represents random data).
- The external address increments sequentially on a transaction boundary (every quad-word). For sequential addressing, the number of address bits switching approaches 2 bits.
- The control pins switch for refresh cycles and page boundary crossings.
- SCLK = 62.5 MHz (bus cycle time).

Using Equation 12, the average dynamic current ($I_{DD_IO_EP_DYN}$) consumed by the External Port pins on the V_{DD_IO} supply is calculated for each class of pins that can drive as shown in Table 3.

Pin Type	# of Pins	% Switching	$x C$	$x V_{DD_IO}$	$x f$	= $I_{DD_IO_EP_DYN}$
Data	64	50	5 pF + 4 x C_{IN}	2.5 V	31.25 MHz	0.0425 A
Addr	32	6.25	10 pF + 4 x C_{IN}	2.5 V	15.625 MHz	0.0017 A
Ctrl	8	50	10 pF + 4 x C_{IN}	2.5 V	156.25 KHz	0.0001 A

Table 3. External Port Current Calculation Example

From the data in Table 3, the total average dynamic current consumed by the External Port of a single processor in the example system is

calculated by summing the data from the right-most column of the table:

$$\begin{aligned}
 &0.0425\text{ A} \\
 &0.0017\text{ A} \\
 &\underline{+0.0001\text{ A}} \\
 I_{DD_IO_EP_DYN} &= 0.0443\text{ A}
 \end{aligned}$$

Example 9. External Port Total Average Dynamic Current Calculation

Note that the total average dynamic power measured on the V_{DD_IO} domain is calculated on a total system basis with regard to the External Port switching. For the External Port system example, the results given in Example 9 are for the entire External Port dynamic power consumption for the example four-processor system. In other words, this result is not added to the total current for each processor in the system, since only one processor can drive the cluster bus at any given time.

External Port Static Current

One final component to discuss here is the static current consumed by the internal circuitry of the processor supplied by the V_{DD_IO} domain. The static current consumed by the External Port circuitry on the V_{DD_IO} domain is approximately 7.0 mA. Note that this 7 mA value is contributed by each processor in the system when calculating the overall current budget on the V_{DD_IO} domain.

$$I_{DD_IO_EP_STATIC} = 7.0\text{ mA}$$

Equation 13. External Port Static Current Consumption

Total Estimated External Port Current ($I_{DD_IO_EP}$)

The total External Port current consumed by each processor on the cluster bus on the V_{DD_IO} domain is calculated as follows:

$$\begin{aligned}
 & I_{DD_IO_EP_DYN} / N \\
 + & I_{DD_IO_EP_STATIC} \\
 = & I_{DD_IO_EP}
 \end{aligned}$$

Where: N = the total number of ADSP-TS201S processors in the cluster

Equation 13. Total Estimated External Port Current per Processor

For the example system, the value of $I_{DD_IO_EP}$ for each processor can be estimated as shown in the following example:

$$\begin{aligned}
 & 44.3 \text{ mA} / 4 \\
 + & 7.0 \text{ mA} \\
 = & 18.1 \text{ mA}
 \end{aligned}$$

Example 10. Total Estimated External Port Current Calculation per Processor

Link Port Current Estimation

The Link Port current ($I_{DD_IO_LP}$) consumption on V_{DD_IO} domain is comprised of three different components: the external dynamic current, the internal static current, and the internal dynamic current.

The external dynamic current for a transmitting Link Port is negligible and can be ignored for the current consumption estimations. (This statement also holds true for a receiving Link Port.)

The output pins of the Link Ports are driven by current-mode drivers; thus the logic value of the differential output pins is determined by the *direction* of the current, *not* by the voltage value on the output pin. Therefore, there is no “ $C \times V \times F$ ” dependency on the external dynamic current of the Link Ports. Also, external capacitive loading on the LVDS drivers has no effect on the current consumed by the Link Ports.

A portion of the internal static current is due to the active circuitry of the Link Port and its related logic; this component is independent of the data width of the Link Port (1-bit or 4-bit mode).

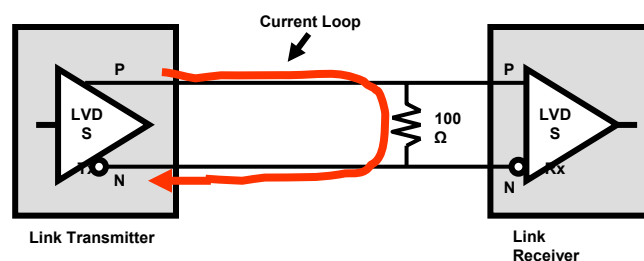


Figure 3. LVDS Current Loop Through Terminating Resistor

The remainder of the internal static current of the Link Port is determined by the termination scheme on the differential pin pairs. Because the LVDS Link Ports utilize current-mode drivers, there is a contribution to the internal static current due to the current loop that connects the “P” and “N” differential-mode drivers via the 100 Ω terminating resistor across the “P” and “N” pins of the LVDS receiver. Figure 3 shows a graphical depiction of this current loop.



The Link Ports on revision 2.0 silicon have a 100 Ω terminating resistor incorporated on-chip across the Link Port receive LVDS P/N clock and data pin pairs. Therefore, the external 100 Ω terminating resistor (as shown in Figure 3) may not be required on the PCB, depending on the frequency of the Link Port receiver. For more information on this topic, please refer to *ADSP-TS20xS TigerSHARC System Design Guidelines (EE-179)*.

The internal dynamic current depends on the switching frequency of the output driver circuits and the capacitance of the related internal circuits. (Keep in mind that the majority of the dynamic switching is due to the differential data and clock pairs of the Link Port; although the single-ended block completion output and acknowledge signals are active during Link Port activity, their contributions to the overall switching can be ignored.)

Table 4 shows the total current value per Link Port for different frequencies, data widths, data activity levels, and termination schemes. (The unused LVDS data pin-pairs for 1-bit mode in this table were left unconnected, as described in the following paragraphs.) The values shown were taken at $T_{CASE} = 85^{\circ}\text{C}$ and $V_{DD_IO} = 2.5\text{ V}$.

	1-bit		4-bit	
freq (MHz)	typ (mA)	max (mA)	typ (mA)	max (mA)
no connect	13.25	13.25	13.25	13.25
0	20.50	20.50	31.00	31.00
125	33.25	35.00	34.25	36.00
150	33.75	36.25	35.00	37.00
250	36.25	40.00	37.25	41.00
300	37.25	42.25	38.75	43.00
333	37.75	43.50	39.25	44.25
400	39.55	46.50	41.25	46.75
500	41.75	50.50	43.75	50.50

Table 4. Link Port Current Consumption per Link Port

The first column lists the different Link Port operating frequencies. The “no connect” entry refers to a transmitting Link Port that is not connected to an LVDS receiver. In this case, there is no current loop present to contribute to the internal static current because there is an open circuit on the differential pair. The “0 MHz” entry refers to a Link Port that is connected to an LVDS receiver, but it is not active or enabled. The other entries in this column refer to the respective frequencies of the active Link Port. The “typ” and “max” columns refer to the switching activity on the LVDS outputs. The “typ” label refers to 50% of the data pins switching per link clock edge; the “max” label refers to 100% of the data pins switching per link clock edge. (Note that the Link Ports drive and receive data on each edge of the link clock.)

Link Port 1-Bit Mode Termination Schemes

For 1-bit operating mode, Analog Devices, Inc. recommends the following termination scheme to ensure the minimal amount of current consumed by each transmitting Link Port. Terminate the active LVDS data pin pair with the $100\ \Omega$ resistor across the P/N receive pin pair, but leave the remaining three unused transmitting LVDS data pin pairs unconnected. This will result in the lowest-possible current consumption by the Link Port, and will also save board space and reduce the number of components in the bill of materials (BOM) for the system board, since no signals need to be brought out from the processor package.

Assume that a processor in the example system has two active Link Ports (both receive and transmit channels active per Link Port), one in 1-bit mode and the other in 4-bit mode running at 250 MHz, with both switching at a “typical” data rate. (Note that the external dynamic power consumed by the Link Port is due to the transmitting link only.) Also assume that one of the remaining two inactive Link Ports is connected to an LVDS receiver, and the other is left unconnected.

Link Port 0: unconnected

Link Port 1: connected/1-bit mode/0 MHz

Link Port 2: 1-bit mode/250 MHz/typical switching

Link Port 3: 4-bit mode/250 MHz/typical switching

Example 11. Link Port Configuration

The total current consumed by the Link Ports ($I_{DD_IO_LP}$) for this example system can be calculated as shown in Example 12:

$$\begin{aligned}
 I_{DD_IO_LP} &= L.P.0 + L.P.1 + L.P.2 + L.P.3 \\
 &= 13.25 + 20.50 + 36.25 + 37.25 \\
 &= 107.25\text{ mA}
 \end{aligned}$$

Example 12. Total Link Port Current Estimation

Total Estimated I/O Current (I_{DD_IO})

The total current I_{DD_IO} consumed on the V_{DD_IO} domain can be calculated by the sum of the total estimated External Port and Link Port current:

$$I_{DD_IO} = I_{DD_IO_LP} + I_{DD_IO_EP}$$

Equation 15. Total Estimated I/O Current

Therefore, for the example system with two active Link Ports per processor, and the above mentioned activity on the Cluster Bus, for each processor in the system, I_{DD_IO} can be calculated as follows:

$$\begin{aligned} I_{DD_IO} &= I_{DD_IO_LP} + I_{DD_IO_EP} \\ &= 107.25 \text{ mA} + 18.1 \text{ mA} \\ &= 125.35 \text{ mA} \end{aligned}$$

Example 13. Total Estimated I/O Current

Total Estimated I/O Power (P_{DD_IO})

The total power (P_{DD_IO}) consumed on the V_{DD_IO} domain for each processor can be calculated by multiplying the total estimated I/O current I_{DD_IO} by V_{DD_IO} :

$$P_{DD_IO} = V_{DD_IO} * I_{DD_IO}$$

Equation 16. Total Estimated I/O Power

Therefore, for the example system P_{DD_IO} can be calculated for each processor, as follows:

$$\begin{aligned} P_{DD_IO} &= V_{DD_IO} * I_{DD_IO} \\ &= 2.5 \text{ V} * 125.35 \text{ mA} \\ &= 313.4 \text{ mW} \end{aligned}$$

Example 14. Total Estimated I/O Power

Power Supply Design

The previous three sections have shown how to estimate the average current consumption values on the V_{DD} , V_{DD_DRAM} , and V_{DD_IO} voltage domains for a given system. This section

describes the parameters used when designing the power supply for the TigerSHARC system.

The power supply must be capable of handling worst-case sustainable power consumption for extended periods of time for each of the processor's three voltage domains.

Use the 600 MHz or 500 MHz “Maximum Baseline Static Current” curves (for the appropriate core processor operating frequency in your system) and the “Baseline Dynamic Current” curves to calculate the maximum I_{DD} current consumption that the power supply system design must be able to provide for the processor core. Additionally, use guard-banded values for the external I/O current and worst-case internal DRAM current requirements (I_{DD_IO} , and I_{DD_DRAM} , respectively), as well as the maximum specified voltages for V_{DD} , V_{DD_IO} , and V_{DD_DRAM} .

Using these values ensures that the power supply design will provide maximum sustainable power at its highest efficiency (typically around 90-95%), to all of the voltage domains during sustained periods of maximum activity.

The “Maximum Baseline Static Current” curves show the maximum static current consumed by an individual ADSP-TS201S device for a given processor speed-grade (500MHz or 600MHz). These two specific curves differ from the “Typical Static Baseline Current” graph, which represents the statistical average value for all ADSP-TS201S processors, and is independent of the specific processor speed-grades.

For the V_{DD} voltage domain, the power supply design must be capable of supplying the maximum sustainable power consumption under the worst-case operating conditions. The “Maximum Baseline Static” and “Baseline Dynamic” characteristic curves can be used to find the worst-case current for I_{DD} . For our example, assume the following worst-case system conditions apply:

- V_{DD} = maximum system value (1.05 V + 5%)
- f = 500 MHz (core clock frequency)
- T_{CASE} = maximum system value (55°C)

Multiply this value by the highest activity factor that is used in the system to achieve the value for the worst-case sustainable current draw on the core supply of the processor on the V_{DD} domain.

Assume the above parameters for the following example calculation:

Step 1:

$$\begin{aligned} I_{DD_DYN} &= I_{DD_BASELINE} \times I_{DD_COMP_HIGH} \text{ Activity Factor} \\ &= 2.30 \text{ A} \times 1.00 \\ &= 2.30 \text{ A} \end{aligned}$$

Step 2:

$$\begin{aligned} I_{DD} &= I_{DD_DYN} + I_{DD_STATIC} \\ &= 2.30 \text{ A} + 0.74 \text{ A} \\ &= 3.04 \text{ A} \end{aligned}$$

Step 3:

$$\begin{aligned} P_{DD} (max) &= V_{DD} \times (I_{DD} + I_{DD_A(max)}) \\ &= 1.10 \text{ V} \times (3.04 \text{ A} + 0.05 \text{ A}) \\ &= 3.40 \text{ W} \end{aligned}$$

Example 15. V_{DD} Power Supply

Therefore, from this example, the power supply must be capable of providing 3.40 W on the V_{DD} supply under sustained periods of activity at high efficiency for each processor in the system.

For the V_{DD_IO} voltage domain, the power supply design for this example must be capable of supplying a guard-banded conservative power consumption estimate for I/O activity ($V_{DD_IO} = 2.63 \text{ V}$). This ensures sufficient overhead in the

power supply design during sustained periods of high activity on the I/O domain.

$$P_{DD_IO} (max) = I_{DD_IO} \times V_{DD_IO} (max)$$

Equation 17. V_{DD_IO} Power Supply Example

For the V_{DD_DRAM} voltage domain, the power supply design must be capable of handling an estimated maximum value of 600 mW for this domain (P_{DD_DRAM}) for sustained periods of activity.

$$\begin{aligned} P_{DD_DRAM} (max) &= I_{DD_DRAM} (max) \times V_{DD_DRAM} (max) \\ &= 600 \text{ mW} \end{aligned}$$

Example 16. V_{DD_IO} Power Supply

Thermal Relief Design

The overall system power estimation can also be used to estimate a thermal relief budget. Equation gives a value for the total maximum estimated thermal power for a single ADSP-TS201S device in a given system.

Using maximum values in this equation is recommended for a thermal relief design that will allow the system to operate within specified thermal parameters under all operating conditions, since using these maximum values provides sufficient headroom (i.e., guard-band) in the thermal relief system design.

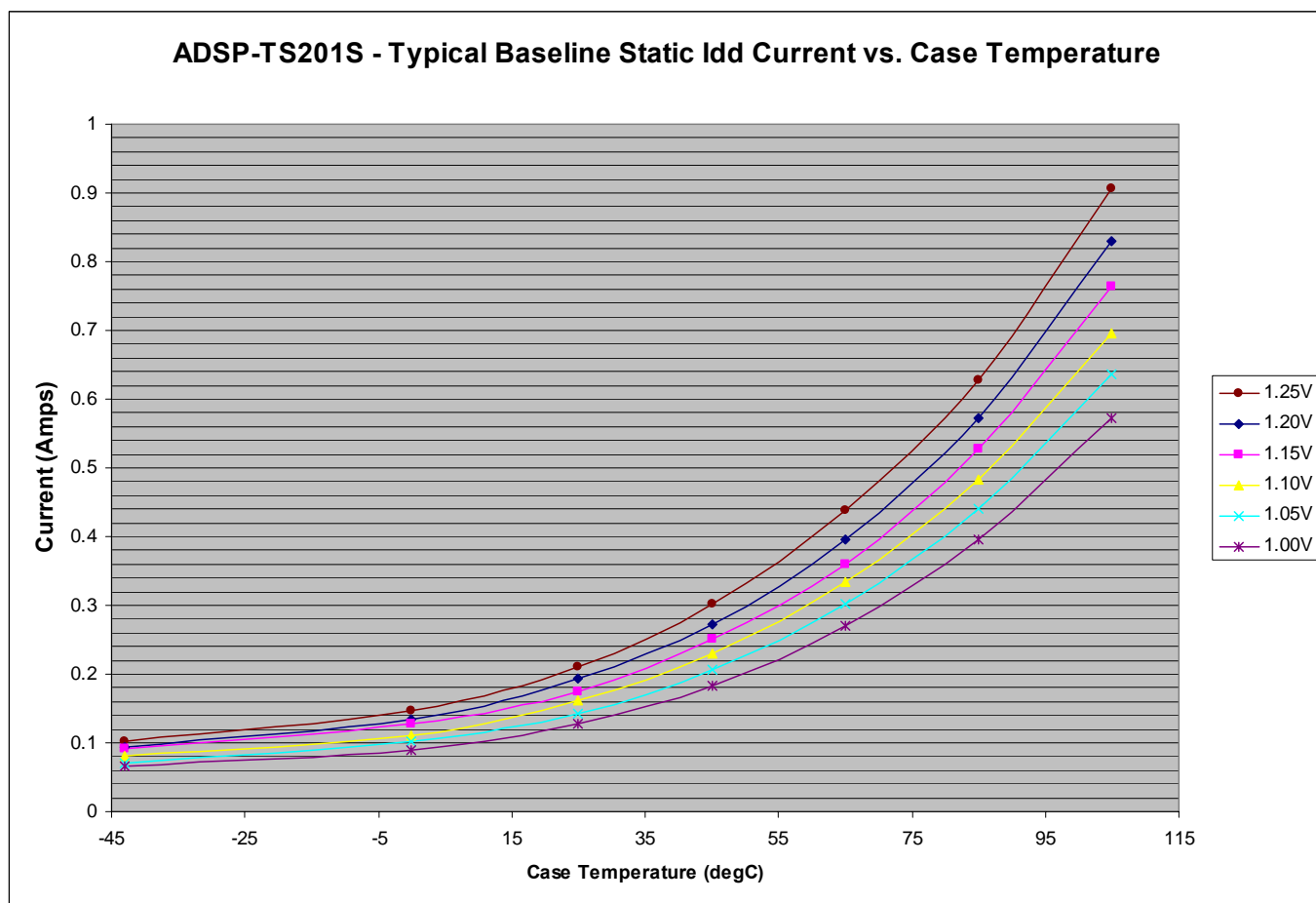
$$P_{TOTAL} = P_{DD} (max) + P_{DD_IO} (max) + P_{DD_DRAM} (max)$$

Equation 18. Total Estimated Thermal Power

Appendix A

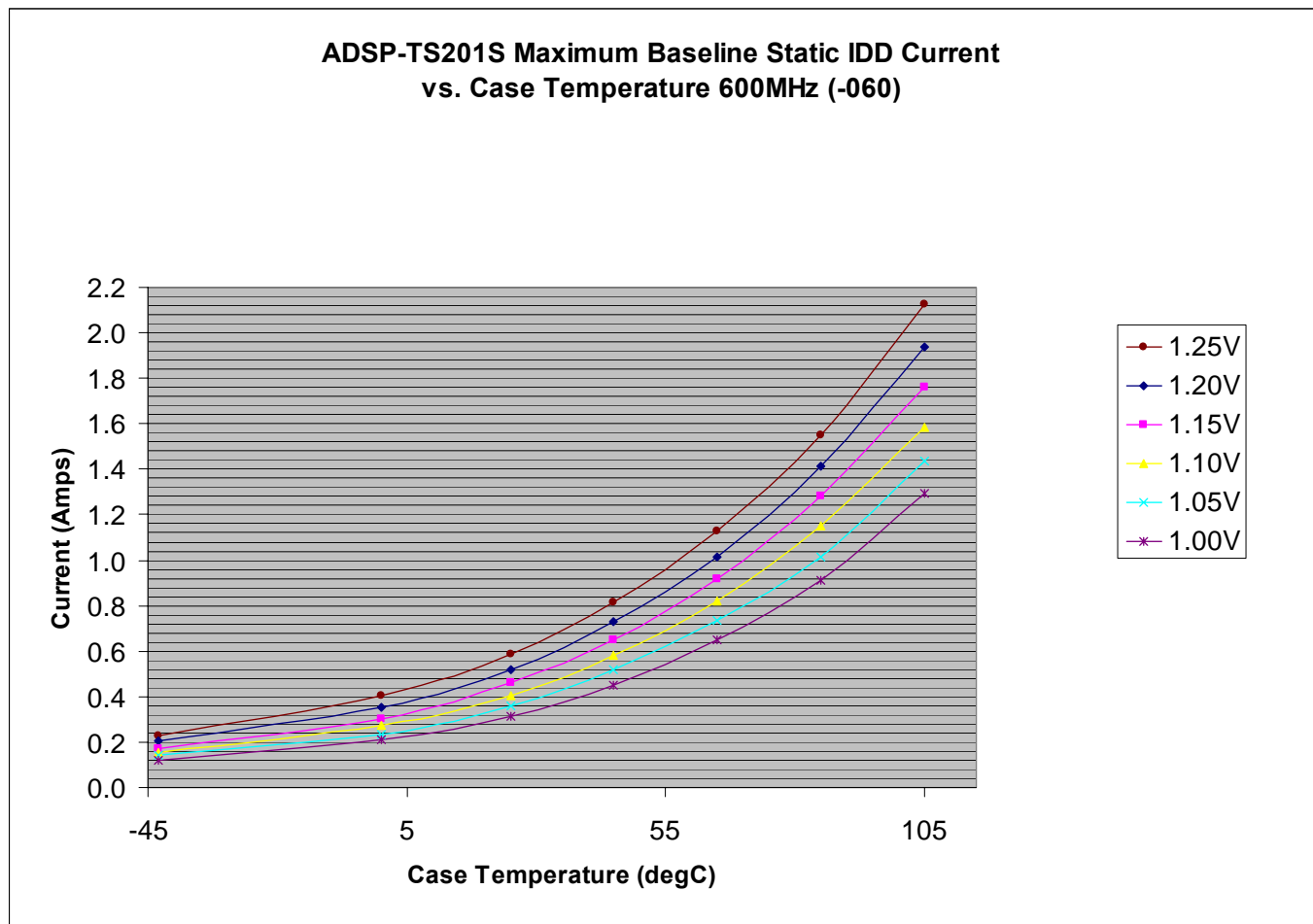
Appendix A contains three different baseline static graphs; typical baseline static current, maximum baseline static current for 600 MHz devices (-060), and maximum baseline static current for 500 MHz devices (-050). Each of these three specific graphs represent the differences in the overall static current due to process variation, which therefore yields different values for I_{DD_STATIC} . Note that the total static current is a function of voltage and temperature, and is also process dependent.

Typical Baseline Static Current



The “Typical Baseline Static I_{DD} Current” graph also appears in [Figure 2](#) on page 5 of this document. Consider the curves in this graph when calculating the *average* static power consumed by each processor in a system. This data represents the statistical average I_{DD_STATIC} static current for the ADSP-TS201S processor.

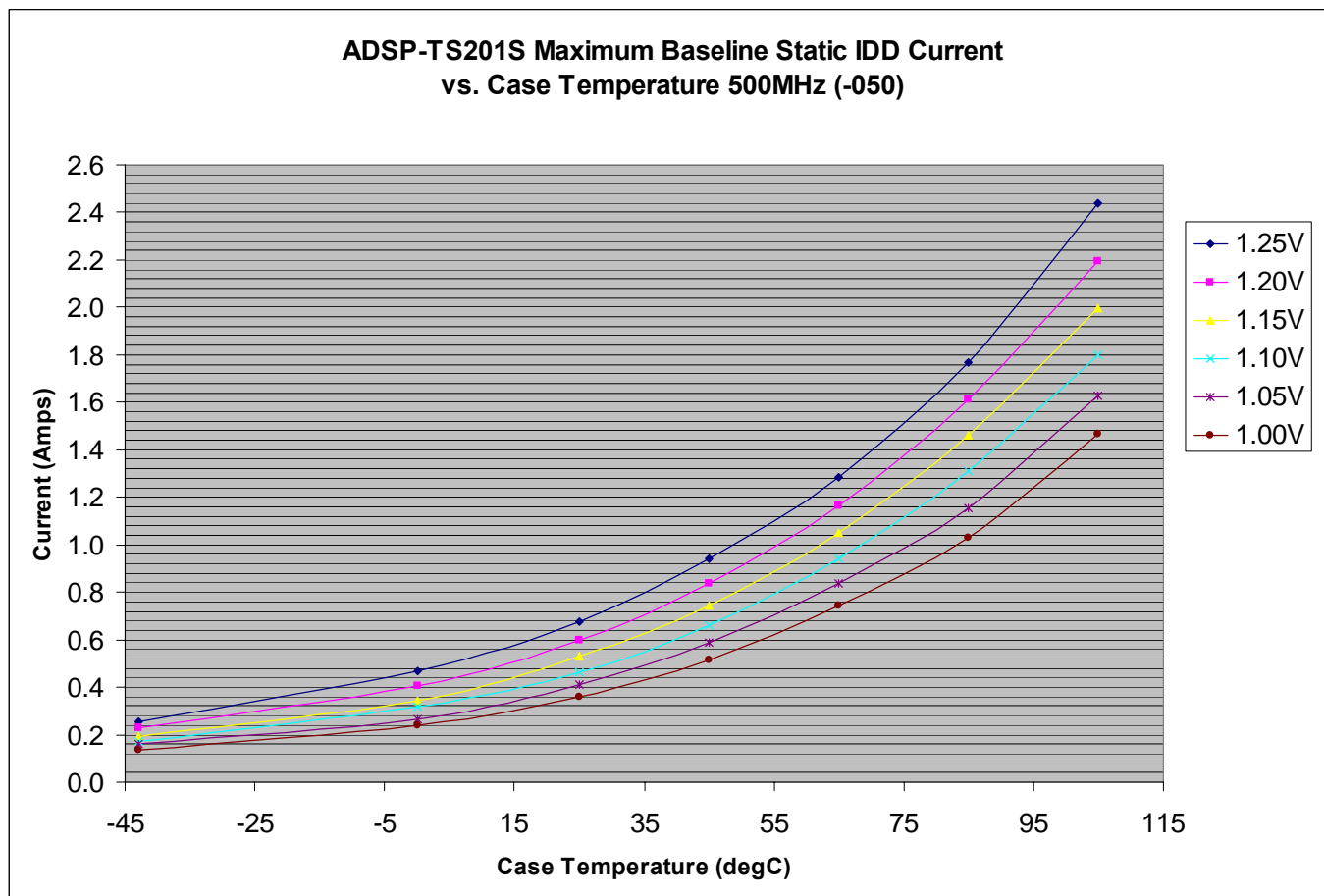
Maximum Baseline Static Current (600 MHz)



The curves in the “Maximum Baseline Static I_{DD} Current 600 MHz (-060)” graph are used to calculate the *maximum* static current and power consumed by each processor in a system. These curves represent worst-case data for each given voltage, specifically for the 600 MHz (-060) speed-grade only. (For 500 MHz (-050) speed-grade devices, refer to the “Maximum Baseline Static I_{DD} Current (500 MHz)” graph on the following page.) These curves should be used when estimating the *maximum* static current and power consumption for each 600 MHz processor in a system, when specifying a power supply or thermal relief design.

Note that the value for the maximum static current for 500 MHz devices is greater at higher case temperatures than for 600 MHz devices at the same given temperature. The reason for this is because of the fact that the 600 MHz devices have a lower temperature rating (85°C vs. 105°C). Thus, since the dynamic power of the 600 MHz devices is higher than for the 500 MHz devices (due to their higher V_{DD} voltage and switching frequency), therefore the static power *must* be lower for the 600 MHz at the same given temperature as a 500 MHz device.

Maximum Baseline Static Current (500 MHz)

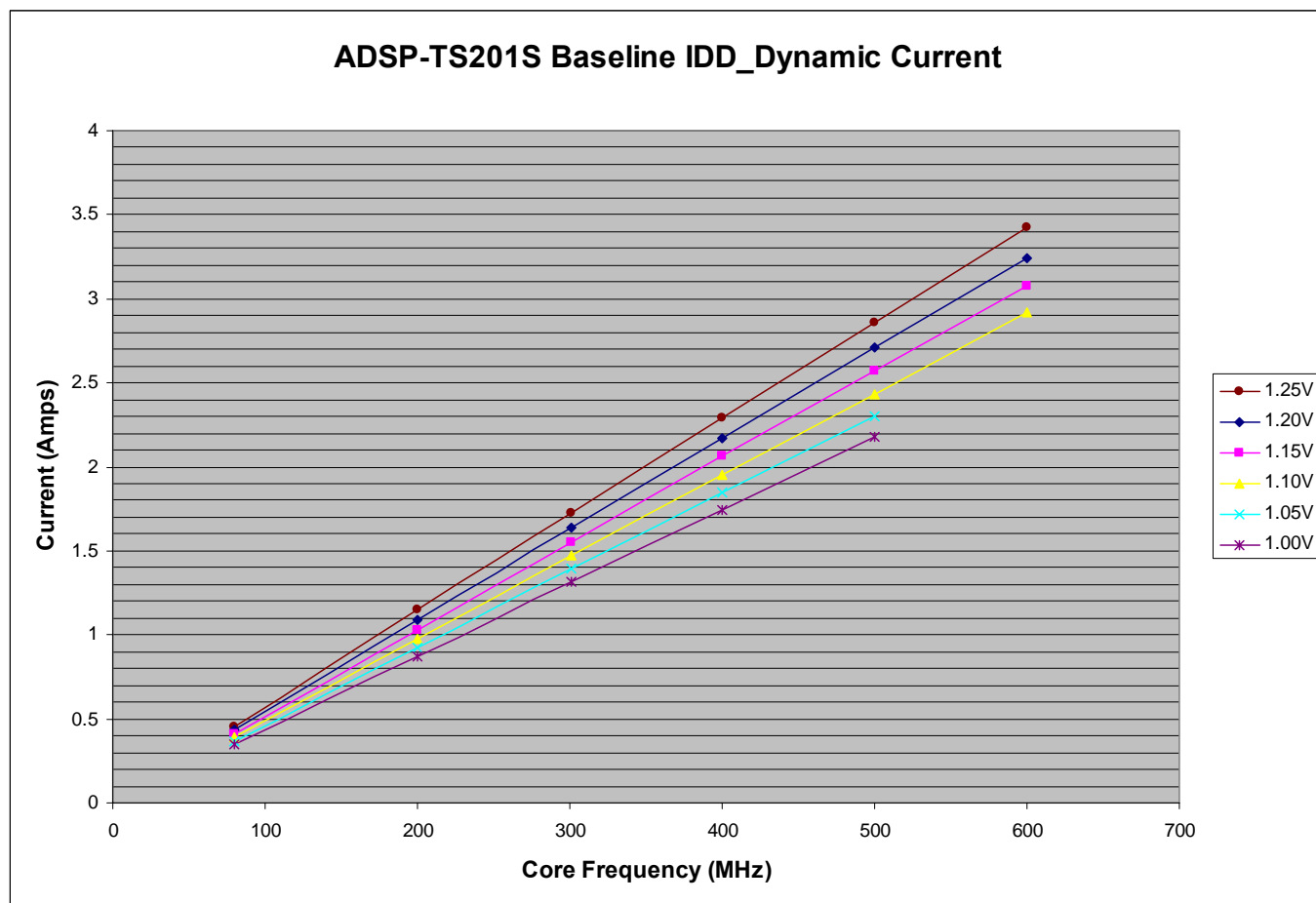


The curves in the “Maximum Baseline Static I_{DD} Current 500 MHz (-050)” graph are used to calculate the *maximum* static current and power consumed by each processor in a system. These curves represent worst-case data for each given voltage, specifically for the 500 MHz (-050) speed-grade only. These curves should be used when estimating the *maximum* static current and power consumption for each 500 MHz processor in a system, when specifying a power supply or thermal relief design.

Note that the value for the maximum static current for 500 MHz devices is greater at higher case temperatures than for 600 MHz devices at the same given temperature. The reason for this is because of the fact that the 600 MHz devices have a lower temperature rating (85°C vs. 105°C). Thus, since the dynamic power of the 600 MHz devices is higher than for the 500 MHz devices (due to their higher V_{DD} voltage and switching frequency), therefore the static power *must* be lower for the 600 MHz at the same given temperature as a 500 MHz device.

Appendix B

Appendix B contains the Maximum Baseline Dynamic Current graph, which represents values for I_{DD_DYN} . This graph appears in [Figure 1](#) on page 3 of this document. The information in this graph pertains to all date codes and revisions of ADSP-TS201S processors.



Appendix C

Appendix C contains a screenshot of the “ADSP-TS20x Power Calculator”. This Excel spreadsheet can be used in conjunction with the information contained within EE-170, and can be used to quickly modify the operating parameters of the ADSP-TS20x processor in a system.

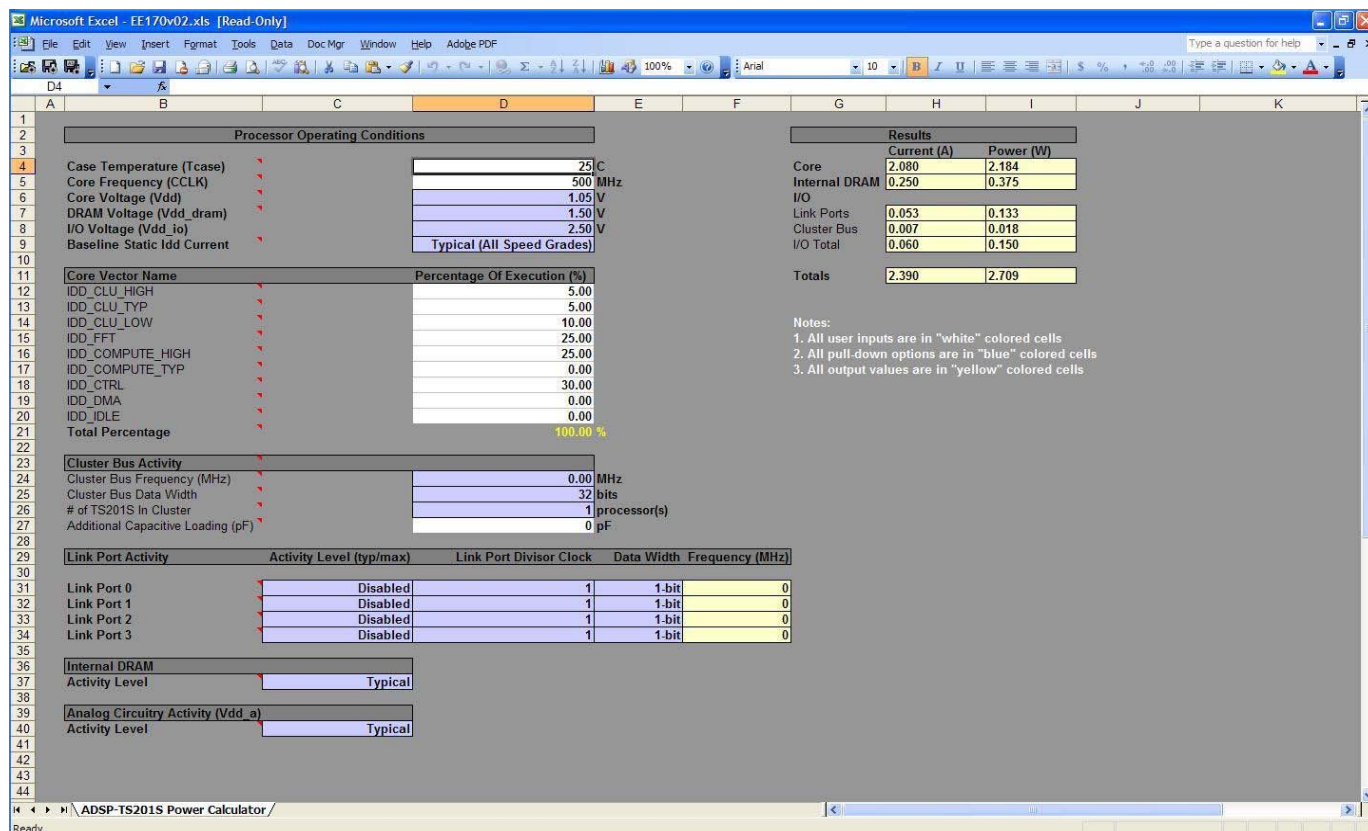


Figure 4. ADSP-TS20x Power Calculator

Figure 4 is a screenshot of the actual calculator spreadsheet. This spreadsheet is broken up into three separate categories. The user data inputs are the “white” cells, where the appropriate data values can be entered as text. An example of a user data input cell is the “Case Temperature” cell or one of the core vector percentage of execution input cells (cells D12 through D20). Warnings are issued whenever an invalid value is entered in any one of the user data input cells.

User selections are pull-down menus in the “blue” cells. Here a list of possible input values that can be chosen when the appropriate cell in the spreadsheet is selected (no text should be entered in the blue cells). An example of a user selection cell is the cluster bus frequency (cell D24). Only the user data input cells and the user selection cells can be selected by the cursor.

All of the output values are displayed in the “yellow” cells. An example of an output value is the Link Port power value, shown in cell I7. The output value cells cannot be selected by the cursor. Lastly, comments for each cell are included. Comments are shown by placing the cursor over the “red” carat symbol in the appropriate cells in column B of the spreadsheet.

Document History

Revision	Description
<i>Rev 2 – October 16, 2006 by Greg F.</i>	Table 2 data and Appendix A graphs updated to reflect changes for silicon revision 2.0. Added Appendix C.
<i>Rev 1 – January 03, 2005 by Greg F.</i>	Initial Public Release