AN-911
APPLICATION NOTE

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A Detailed Guide to Powering the *Tiger*SHARC Processors
by Mark Malaeb

INTRODUCTION

As technology constantly evolves and silicon geometry shrinks, different supply requirements for powering these processors emerge. Typically the core is powered with a lower voltage than the I/Os. The I/Os are generally at a higher voltage to maintain a compatible interface with other system devices. Also, as clock speeds of 600 MHz are reached, these processors become more power hungry. Thus, an efficient power management scheme becomes critical.

This application note, in conjunction with the technical note EE-170, (available from Analog Devices, Inc.), provides a guide that can be used as a reference design for powering those processors. EE-170 provides the detailed equations and derivations for the power needs of the processors. This application note discusses the voltage regulators/switchers that are suitable for those processors running at 600 MHz.

The *Tiger*SHARC® processor requires three different supply voltages, the core voltage of 1.2 V, the internal DRAM voltage at 1.6 V, and the I/O voltage of 2.5 V. These three voltages are discussed in details in the following sections.

TABLE OF CONTENTS

CORE VOLTAGE (V$_{DD}$ = 1.2 V)

The current requirement (I$_{DD}$), on this voltage, consists of three components: dynamic current, static current, and analog current. These currents are defined in Equation 1.

$$I_{DD} = I_{DD\_DYNAMIC} + I_{DD\_STATIC} + I_{DD\_ANALOG} \qquad (1)$$

where:
I_{DD_STATIC} is the static portion of the current that is operating-temperature dependent.
I_{DD_ANALOG} is the current needed to power the on-board PLL and its circuitry.

$$I_{DD\_DYNAMIC} = I_{DD\_CLU} + I_{DD\_FFT} + I_{DD\_COMPUTE} + I_{DD\_CTRL} + I_{DD\_DMA} + I_{DD\_IDLE} \qquad (2)$$

where:
I_{DD_CLU} is the communications logic unit current.
I_{DD_FFT} is the current consumption related to high activity floating-point operations.
$I_{DD\_COMPUTE}$ is the current consumed by the activity operations of the computational units.
I_{DD_CTRL} is the current consumption due to continuous decision-making sequence of instructions and predicted branches.
I_{DD_DMA} is the current consumed by a single DMA channel moving data from external to internal memory.
I_{DD_IDLE} is the current consumption due to idle instructions with no DMA or interrupts.

Using Equation 1 and assuming the worst-case maximum dynamic current consumption; $I_{DD\_DYNAMIC}$ = 4.99 A.

The static current consumption at 55°C, from the static current characteristic curve, is I_{DD_STATIC} = 0.32 A.

The maximum analog current consumption is I_{DD_ANALOG} = 0.055 A.

Summing up all these currents using Equation 1 results in

$$I_{DD} = 4.99\ A + 0.32\ A + 0.055\ A = 5.365\ A \qquad (3)$$

This is the total current needed at 1.2 V for each individual *Tiger*SHARC processor. So a switching regulator, capable of supplying 6 A at 1.2 V does the job. However, since the majority of *Tiger*SHARC applications implement two *Tiger*SHARC processors, a circuit to power such applications, using the ADP1821, is discussed. This means that the current requirements doubled to 12 A at 1.2 V. The circuit is shown in Figure 1. This circuit has been implemented and prototypes built and tested. This circuit is usable with single *Tiger*SHARC processor applications as well.

COMPONENT VALUE DERIVATIONS AND ADP1821 ANALYSIS

The ADP1821 is a versatile, synchronous, step-down PWM controller and is designed to drive all N-type channel power FETs. Its output can be set as low as 0.6 V. It can also supply currents as high as 20 A with the appropriate FET. The IC input voltage range is from 3 V to 5.5 V and the power stage voltage range is from 1 V to 24 V. The IC supply range can be extended to 20 V with a simple Zener network to power the device (as shown in Figure 2). This device can be synchronized at any frequency between 300 kHz and 1.2 MHz by the external frequency or by working at 300 kHz or 600 kHz by setting the FREQ pin to either low or high, respectively. The high frequency operation allows for smaller magnetic components. For this application, the 600 kHz switching frequency is selected. The soft start function allows quick startup while limiting the inrush current. Soft start time can be adjusted by selecting the appropriate C$_{SS}$ capacitor. Its efficiency can be as high as 96% (depending on input/output voltages). The component values for this design were derived using Analog Devices power spreadsheets (contact your local Analog Devices sales representative to access the spreadsheets). The spreadsheet employs more accurate equations that produce better results. However, the data sheet equations put the user within the range of results and provide a better understanding of the results.
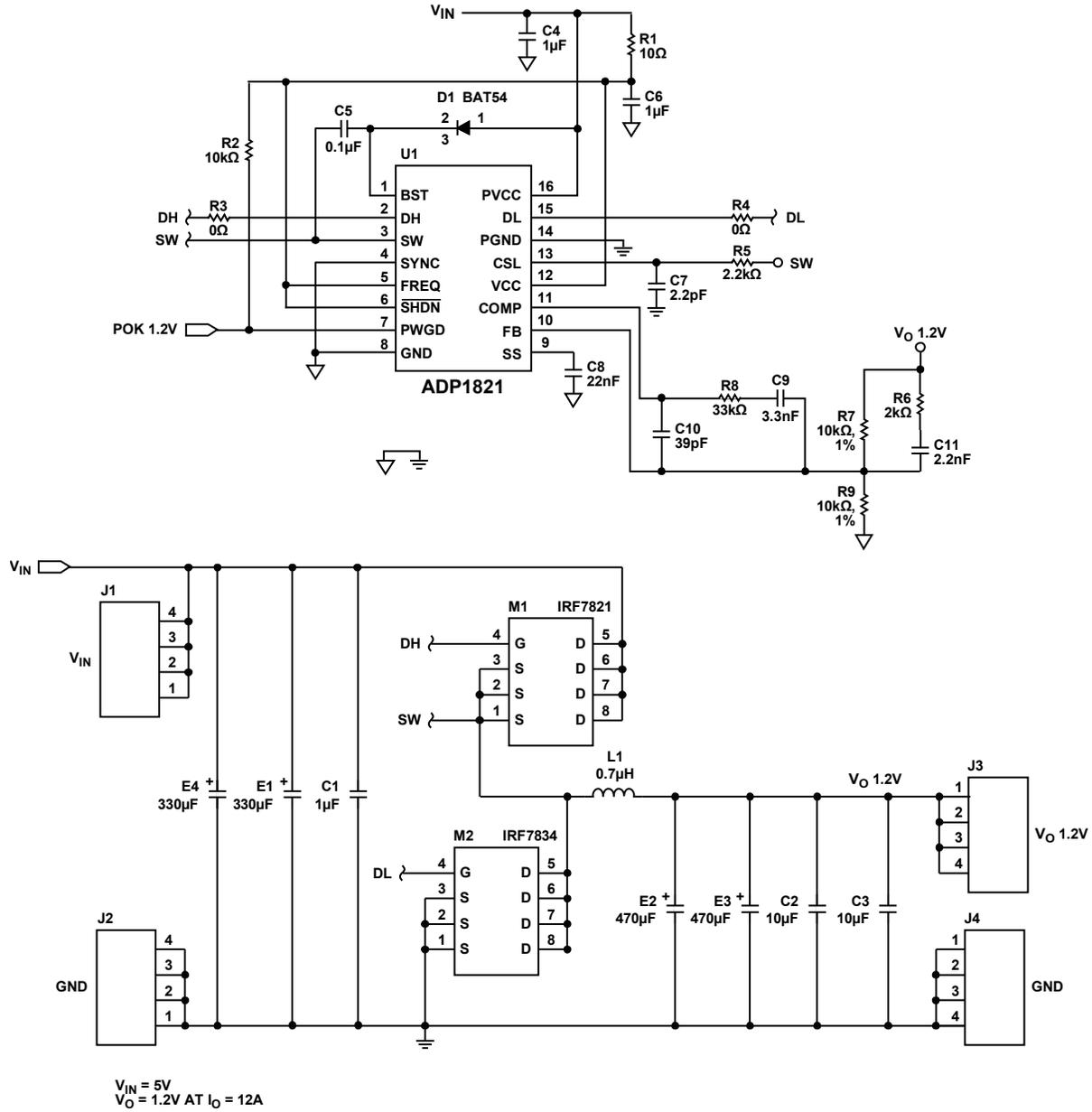
Figure 1. Core Supply Voltage Circuit

Choosing the Input Capacitor Value

The input capacitor is used to ensure a smooth input supply current. It should be chosen such that its impedance, at the switching frequency, is lower than the impedance of the supply upstream. The current rating for the input capacitor should be higher than the rms input ripple current defined in EE-170.

Assuming an input voltage of 5.0 V and an output voltage of 1.2 V at 12 A, the current rating on the capacitors should be at least about 5.125 A. With higher input voltages, the rating requirements on the input capacitor current is lower. Thus, these capacitor values still work at higher input voltages.

Also, a relatively large capacitance is used at the input to keep the ripple voltage on the supply line low. This is especially important where the supply line is high impedance. It is recommended that the supply line be kept at low impedance. Usually, a 100 μF to 1000 μF capacitor is used at the input depending on the output impedance of the upstream supply. In this application, two capacitors are paralleled to meet the ripple current requirement and also provide a larger capacitance (660 μF).

Setting the Output Voltage

The regulation output voltage is set using the following equation:

$$R_{TOP} = R_{BOT}\left(\frac{V_{OUT} - V_{FB}}{V_{FB}}\right) \tag{4}$$

where:
R_{TOP} is R_7 (the high-side voltage divider resistance).
R_{BOT} is R_9 (the low-side voltage divider resistance (10,000 typ)).
V_{OUT} is the desired output voltage (1.2 V).
V_{FB} is the feedback threshold voltage (0.6 V).

Solve for R_{TOP} by

$$R_{TOP} = 10\ \Omega \times (1.2\ \Omega - 0.6\ \Omega)/0.6\ \Omega = 10{,}000\ \Omega \tag{5}$$

Choosing the Compensating Loop Components

The buck converter is a second-order system (the LC output filter generates two poles). To get a stable and good system transient response, the compensation needs to be well designed.

The loop can be compensated using the zero generated by the ESR of the output capacitor (Type II compensator). However, because the ESR of the output capacitor is generally not well characterized, one way of reducing the dependency on ESR is to have multiple capacitors parallel with and lower than the ESR value as was done for this design. A compensating scheme called feedforward compensation (Type III compensator) was used. The compensating loop elements for this circuit are shown in Figure 1, which are R8, C9, C10, C11, and R6. These values were derived from the following equations:

$$R8 = 0.0705 \times R7\ (f_{SW})^2 \times LC/V_{IN} \tag{6}$$

R8 is 34,000 Ω and a 33,000 nF capacitor was used.

$$C9 = 1.6\ \text{nF} \tag{7}$$

A 3.3 nF capacitor was used.

$$C10 = 2/(2\pi \times f_{SW} \times R8) \tag{8}$$

C10 is 16 pF; the spreadsheet value was 39 pF.

$$\begin{aligned} C11 &= 11.14/(R7 \times f_{SW}) \\ &= 11.14/(10{,}000 \times 600\ \text{kHz}) \end{aligned} \tag{9}$$

C11 is 1.86 nF and a 2.2 nF capacitor was chosen.

$$\begin{aligned} R6 &= 0.227/(C11 \times f_{SW}) \\ &= 0.227/(1.86 \times 600\ \text{kHz}) \end{aligned} \tag{10}$$

R6 is 203 Ω; the spreadsheet value was 2000 Ω.

These values are very sensitive to the ESR values of the output capacitor and vary dramatically. Any combination of values will work as long as the loop is stable.

Choosing the Output LC Filter Components

The LC filter is chosen to achieve a desired output voltage ripple. This paragraph shows how the inductor value is derived.

$$L = V_{OUT}\ [1 - V_{OUT}/V_{IN}]/(f_{SW} \times \Delta I_L) \tag{11}$$

where:
V_{OUT} is the desired output voltage (1.2 V).
V_{IN} is the input voltage (5 V).
f_{SW} is the converter switching frequency (600 kHz).
ΔI_L is the inductor ripple current (typically 20% to 30% of the maximum output current, in this design 20% is chosen).

Thus,

$$\begin{aligned} L &= 1.2\ [1 - 1.2/5]/(600\ \text{kHz} \times 12/5) \\ &= 0.63\ \mu\text{H} \end{aligned} \tag{12}$$

A standard inductor with value of 0.7 μH was chosen. Then the inductor ripple current becomes:

$$\begin{aligned} \Delta I_L &= V_{OUT} \times [1 - V_{OUT}/V_{IN}]/(f_{SW} \times L) \\ &= 2.17\ \text{A} \end{aligned} \tag{13}$$

Next, the inductor's current rating needs to be chosen based on the following:

The $I_{SATURATION}$ current should be greater than $I_O + \Delta I_L/2 = 12 + 2.17/2 = 13.08$ A, and the I rms current value should be larger than $(I_O^2 + \Delta I_L^2/12)^{1/2} = 12.02$ A.

For the chosen output capacitor, the most important factor to consider is the ESR. The ESR was chosen to meet the output ripple specification. In this design, the ESR of the output capacitor is chosen to be smaller than $\Delta V_O/\Delta I_L = 5.5$ mΩ (ΔV_O is the output voltage ripple, typically $\Delta V_O = 1\% \times V_O$ is required). Thus, two capacitors, with ESR = 10 mΩ, were used in parallel.

Choosing the MOSFETs

Typically, the MOSFETs must have low on resistance to minimize power dissipation due to I²R and low gate charge to lower gate losses and transition losses. However, the lower the on resistance, the higher the gate charge (and transition losses). Choose a MOSFET to balance those losses. For more details, see the ADP1821 data sheet.

A switcher typically has two field effect transistors (FET): a high-side FET and a low-side FET. For the high-side FET selection, gate charge and on resistance should both be considered. For a lower duty cycle application, the main loss

on the high-side FET is the transition loss, thus gate charge is the first factor to be considered.

Because the low-side FET does not carry transition losses, the main factor in its selection is low on resistance. The following equation governs the behavior of the power loss in the lower FET:

$$P_C \cong (I_{LOAD})^2 \ R_{DSON}\left(\frac{V_{OUT}}{V_{IN}}\right)$$

(14)

Choosing the Soft Start Capacitor, C8

The soft start feature is designed to minimize input inrush current and prevent output voltage overshoot during startup. The ADP1821 charges the external capacitor (C8) to 0.8 V through a 100 kΩ internal resistor and regulates the voltage at the FB pin to the lower value of either SS or the internal 0.6 V. When the voltage at FB is between 0.55 V and 0.75 V, the power-good output (PWGD) is asserted.

In Figure 1, the input voltage range is 3.3 V to 5.5 V. This range can be adjusted to support input voltages up to 20 V by using a simple Zener network circuit (see Figure 2). Choose R_{IN} to correspond to the desired input voltage while maintaining about 5.6 V across the Zener.
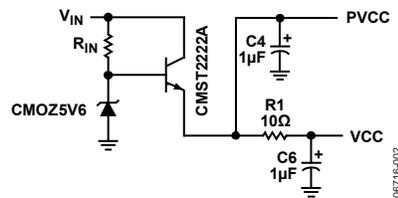

Figure 2. Zener Network Circuit

INTERNAL DRAM VOLTAGE (V_{DD_DRAM} = 1.6 V)

The DRAM on the TS processors requires an external supply. Although the current needed is not as large as the core current, it can go as high as 430 mA. This current is supplied by the ADP2105 (see Figure 3).
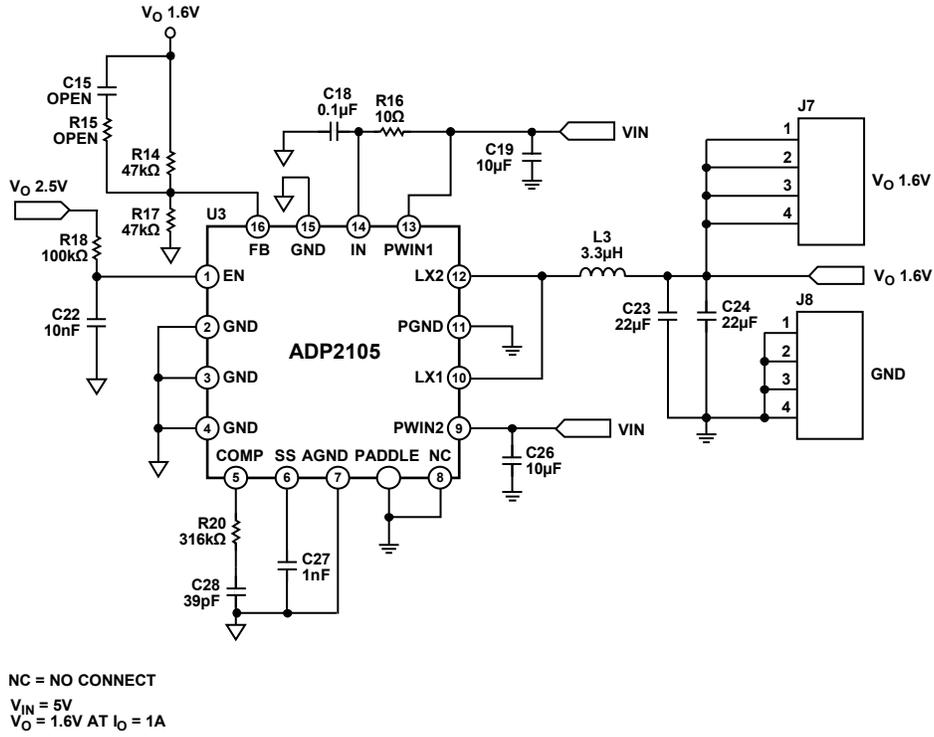

Figure 3. Internal DRAM Supply Voltage Circuit

COMPONENT VALUE DERIVATIONS AND THE ADP2105 ANALYSIS

The ADP2105 is a synchronous step-down converter with peak current mode control. It integrates the high-side switch FET and the low-side synchronous rectifier. The ADP2105 operates at a fixed frequency of 1.2 MHz. It has two modes of operation, full pulse-width modulation mode (PWM) and pulse frequency modulation mode (PFM). At lighter loads the ADP2105 resorts to PFM mode where bursts of energy are delivered to the load as needed (see the ADP2105 for details). The input range for this device is 2.7 V to 5.5 V. Its output voltage can be as low as 0.8 V and its output current as high as 1 A.

Choosing the Input Capacitor Value (Input Filter)

An input filter is needed to make sure that the supply to the device is clean. As described in the ADP1821 the recommended values for the input capacitor, C18, is 0.1 μF and a resistor, R16, is 10 Ω as shown in Figure 3. This combination forms a low-pass filter at about 150 kHz. The recommended values for C19 is 10 μF and C26 is 10 μF (see the ADP1821 for more details).

Setting the Output Voltage

To limit output accuracy degradation, (due to FB bias current), to less than 0.5%, the divider string current should be greater than 15 μA. The bottom resistor, R16, can be determined by:

$$R16 = V_{FB}/I_{STRING}$$
$$= 47 \text{ k}\Omega \tag{15}$$

where:
$V_{FB} = 0.8$ V (internal reference voltage).
$I_{STRING} = 17$ μA.

The top resistor, R14, can be determined by:

$$R14 = R16 \ (V_{OUT} - V_{FB})/V_{FB}$$
$$= 47 \ (1.6 - 0.8)/0.8$$
$$= 47 \text{ K}\omega \tag{16}$$

Choosing the Output LC Filter Components

The minimum inductor value is defined as in the ADP2105 data sheet:

$$L > (1.12 \ \mu\text{H/V}) \times V_{OUT} = 1.12 \times 1.6 = 1.792 \ \mu\text{H} \tag{17}$$

The ideal inductor value is found as:

$$L_{IDEAL} = 2.5 \times V_{OUT} \ (V_{IN} - V_{OUT})/(V_{IN} \times I_{LOAD(MAX)})$$
$$= 2.5 \times 1.6(5 \times 1.6)/5 \times 1$$
$$= 2.72 \ \mu\text{H} \tag{18}$$

Thus, an inductor, L3, of 3.3 μH is chosen.

The output capacitor is chosen based on the transient response requirements. For an overshoot of less than 4%, see Figure 4.
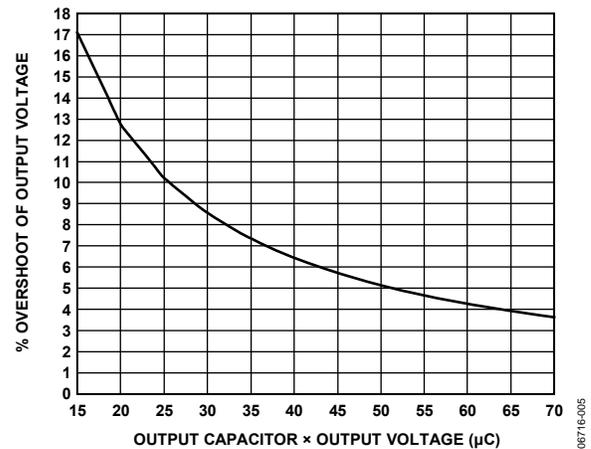

Figure 4. % Overshoot for a 1 A Load Transient Response vs. Output Capacitor × Output Voltage

$$C_{OUT} = 60/1.6 = 37.5 \ \mu\text{F.} \tag{19}$$

To make sure that capacitance is above dc, a total of 44 μF should be used.

Choosing the Compensating Loop Components

These values can be found as

$$R20 = 0.8 \ (2\pi \times F_{CROSS}) \ (C_{OUT} \times V_{OUT})/G_m \ GCS \times V_{REF} \tag{20}$$

$$C28 = 2/(\pi \times F_{CROSS} \times R20) \tag{21}$$

Plug in the values to get

$$R20 = (2\pi \times 80 \text{ kHz}) \ (37.5 \times 1.6)/50 \times 1.875 \times 0.8 = 324 \text{ k}\Omega \tag{22}$$

$$C28 = 2/(\pi \times 80 \text{ kHz} \times 324 \text{ k}\Omega) = 25 \text{ pF} \tag{23}$$

Some adjustments to these components were needed due to layout; R20 is 316 kΩ and C28 is 39 pF were chosen instead.

I/O VOLTAGE ($V_{DD\_I/O}$ = 2.5 V)

This voltage is used to supply power to the external port, and the link ports and the associated circuitry for the external pins, output drivers, and control logic.

The total I/O current is the sum of the external port current and the link port current given by Equation 2.

$$I_{DD\_IO} = I_{DD\_IO\_EP} + I_{DD\_IO\_LP} \tag{24}$$

where:
$$I_{DD\_IO\_EP} = I_{DD\_IO\_EP\_DYN} + I_{DD\_IO\_EP\_STATIC} \tag{25}$$
$$I_{DD\_IO\_LP} = I_{\_LP0} + I_{\_LP1} + I_{\_LP2} + I_{\_LP3} \tag{26}$$

THE EXTERNAL PORT CURRENT

Referring to Equation 3, the external port current has two components: a dynamic current and a static current.

See the EE-170 for an external port current calculation example and assume a maximum SCLK is 500 MHz.

$$I_{DD\_IO\_EP\_DYN} = (170 \text{ mA} + 13.75 \text{ mA} + 0.28 \text{ mA})/4$$
$$= 46 \text{ mA} \tag{27}$$

And according to the EE-170

$$I_{DD\_IO\_EP\_STATIC} = 7 \text{ mA} \tag{28}$$

The total maximum external port current needed (using Equation 3) is:

$$I_{DD\_IO\_EP} = 46 + 7$$
$$= 53 \text{ mA} \tag{29}$$

THE LINK PORT CURRENT

Using Equation 4, the link port current is the sum of the currents from all four links. Each of these links can be one- to four-bits wide. The maximum current required by each link is about 50 mA (see the EE-170 for samples of link port current consumption per link port).

$$I_{DD\_IO\_LP} = 4 \times 50.5$$
$$= 202 \text{ mA} \tag{30}$$

Using Equation 2, the total current required for the I/O is:

$$I_{DD\_IO} = I_{DD\_IO\_EP} + I_{DD\_IO\_LP}$$
$$= 53 + 202$$
$$= 255 \text{ mA} \tag{31}$$

This current is supplied by the ADP2105 as shown in Figure 5.

COMPONENT VALUE DERIVATIONS

The analysis for this circuit (Figure 5) is identical to the derivation used in the Internal DRAM Voltage (V_{DD_DRAM} = 1.6 V) section. The two circuits are identical with this voltage being at 2.5 V instead of the 1.6 V as previously calculated.

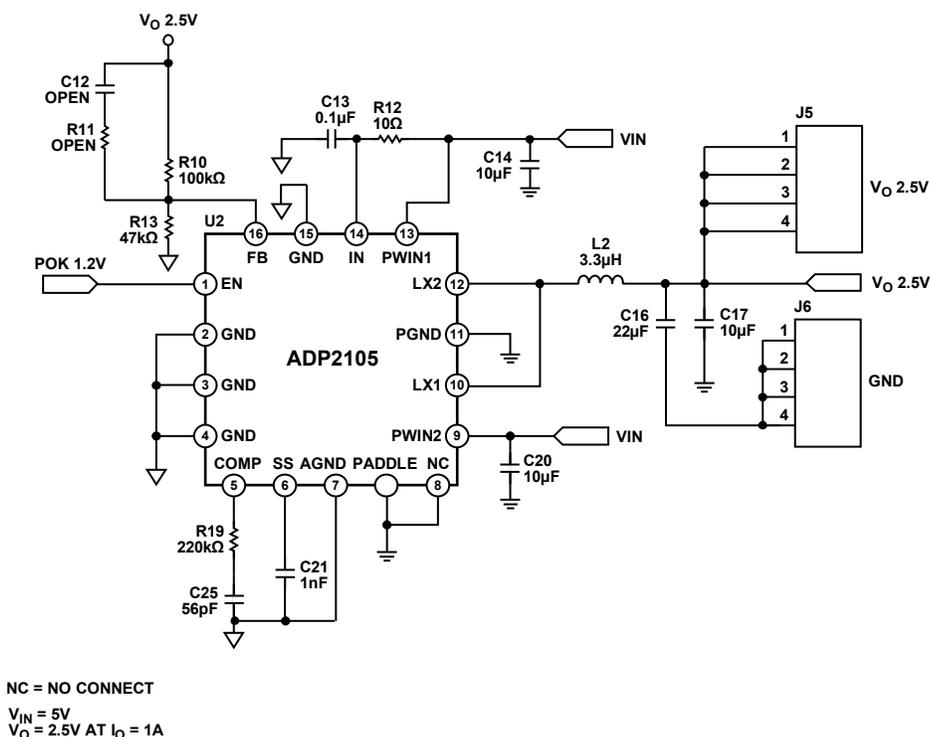*Figure 5. The I/O Supply Voltage Circuit*

BILL OF MATERIALS

Table 1.

Part Reference	Type	Parameter	PCB Footprint	Supplier/Manufacturer No.[1]
C1	Ceramic capacitor	1 µF, 10 V	C0805	*
C2	Ceramic capacitor	10 µF, 6.3 V	C1206	Murata
C3	Ceramic capacitor	10 µF, 6.3 V	C1206	Murata
C4	Ceramic capacitor	1 µF, 10 V	C0603	*
C5	Ceramic capacitor	0.1 µF, 10 V	C0603	*
C6	Ceramic capacitor	1 µF, 10 V	C0603	*
C7	Ceramic capacitor	2.2 pF	C0603	*
C8	Ceramic capacitor	22 nF	C0603	*
C9	Ceramic capacitor	3.3 nF	C0603	*
C10	Ceramic capacitor	39 pF	C0603	*
C11	Ceramic capacitor	2.2 nF	C0603	*
C12	Ceramic capacitor	Open	C0603	*
C13	Ceramic capacitor	0.1 µF, 10 V	C0603	*
C14	Ceramic capacitor	10 µF, 6.3 V	C0805	Murata
C15	Ceramic capacitor	Open	C0603	*
C16	Ceramic capacitor	22 µF, 6.3 V	C0805	Murata
C17	Ceramic capacitor	10 µF, 6.3 V	C0805	Murata
C18	Ceramic capacitor	0.1 µF, 10 V	C0603	*
C19	Ceramic capacitor	10 µF, 6.3 V	C0805	Murata
C20	Ceramic capacitor	10 µF, 6.3 V	C0805	Murata
C21	Ceramic capacitor	1 nF	C0603	*
C22	Ceramic capacitor	10 nF	C0603	*
C23	Ceramic capacitor	22 µF, 6.3 V	C0805	Murata
C24	Ceramic capacitor	22 µF, 6.3 V	C0805	Murata
C25	Ceramic capacitor	56 p	C0603	*
C26	Ceramic capacitor	10 µF, 6.3 V	C0805	Murata
C27	Ceramic capacitor	1 nF	C0603	*
C28	Ceramic capacitor	39 p	C0603	*
D1	Diode	30 V, 200 mA	SOT-23	FairChild BAT54
E1	POSCAP™	10 V, 330 µF, 35 mΩ	Sanyo_TPB_D4	Sanyo 10TPB330M
E2	POSCAP	2.5 V, 470 µF, 10 mΩ	Sanyo_TPD_D4D	Sanyo 2R5TPD470M
E3	POSCAP	2.5 V, 470 µF, 10 mΩ	Sanyo_TPD_D4D	Sanyo 2R5TPD470M
E4	POSCAP	10 V, 330 µF, 35 mΩ	Sanyo_TPB_D4	Sanyo 10TPB330M
J1			sip4_dual	
J2			sip4_dual	
J3			sip4_dual	
J4			sip4_dual	
J5			sip4_dual	
J6			sip4_dual	
J7			sip4_dual	
J8			sip4_dual	
L1	Inductor	0.7 µH, I_{SAT} = 26 A, I rms = 17.3 A	Cooper_HC7	CoilCraft MLC1265-701ML
L2	Inductor	L = 3.3 µH, I_{SAT} = 2.2 A	CoilCraft_LPS4012	CoilCraft LPS4018-332ML
L3	Inductor	L = 3.3 µH, I_{SAT} = 2.2 A	CoilCraft_LPS4012	CoilCraft LPS4018-332ML
M1	MOSFET	*	SO8	International Rectifier IRF7821
M2	Mosfet	*	SO8	International Rectifier IRF7834
R1	Resistor	10 Ω	R0603	*
R2	Resistor	10 kΩ	R0603	*
R3	Resistor	0 Ω	R0603	*

Part Reference	Type	Parameter	PCB Footprint	Supplier/Manufacturer No.[1]
R4	Resistor	0 Ω	R0603	*
R5	Resistor	2.2 kΩ	R0603	*
R6	Resistor	2 kΩ	R0603	*
R7	Resistor	10 kΩ,1%	R0603	*
R8	Resistor	33 kΩ	R0603	*
R9	Resistor	10 kΩ,1%	R0603	*
R10	Resistor	100 kΩ	R0603	*
R11	Resistor	Open	R0603	*
R12	Resistor	10 Ω	R0603	*
R13	Resistor	47 kΩ	R0603	*
R14	Resistor	47 kΩ	R0603	*
R15	Resistor	Open	R0603	*
R16	Resistor	10 Ω	R0603	*
R17	Resistor	47 kΩ	R0603	*
R18	Resistor	100 kΩ	R0603	*
R19	Resistor	220 kΩ	R0603	*
R20	Resistor	316 kΩ	R0603	*
U1	Controller	*	16-Lead QSOP	Analog Devices, Inc. ADP1821
U2	IC	*	16-Lead, 4 × 4 LFCSP	Analog Devices, Inc. ADP2105
U3	IC	*	16-Lead, 4 × 4 LFCSP	Analog Devices, Inc. ADP2105

[1] * = parts that are available from most manufacturers.

NOTES

**ANALOG
DEVICES**

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