External Bus Arbitration with ADSP-TS20x TigerSHARC® Processors

Contributed by Stephen Francis *Rev 1 – February 10, 2006*

1 Introduction

The following Engineer-to-Engineer note discusses external port bus arbitration on ADSP-TS20x TigerSHARC® processors. The intention of this EE-Note is to complement the Multiprocessing Interface and Bus Arbitration Protocol sections of the External Port chapter of the *ADSP-TS201 TigerSHARC Processor Hardware Reference* manual[1]. Example code, in which each TigerSHARC processor in a three-processor system uses the shared external bus to transfer data from its internal memory to the internal memory of another TigerSHARC processor and the resulting captured waveforms highlight the ADSP-TS20x external bus arbitration scheme.

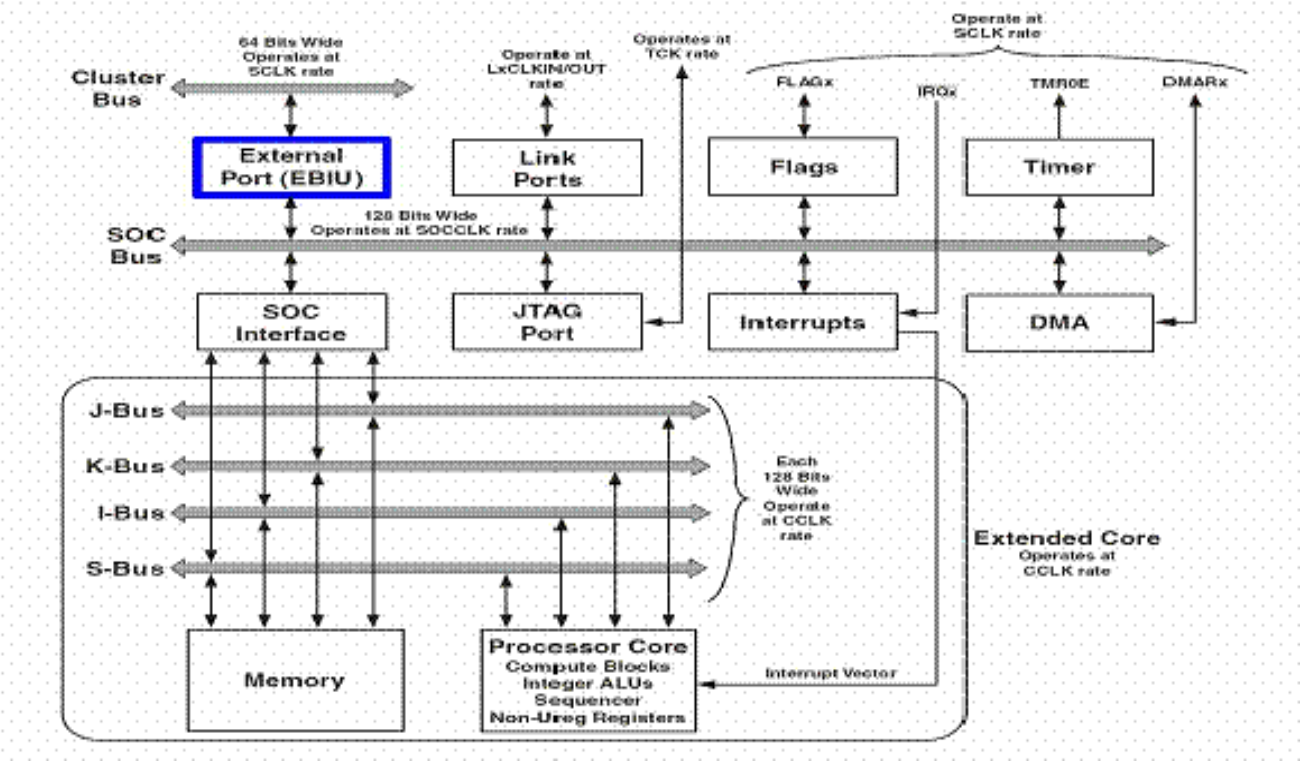

Figure 1. ADSP-TS201 Processor Block Diagram

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3 Bus Arbitration Protocol

The rotating bus arbitration protocol implemented on TigerSHARC processors ensures bus fairness among TigerSHARC processors in a cluster. After reset, the TigerSHARC processor with ID0 becomes the bus master and the external bus priority rotates in a round-robin fashion, going up from the present master. The bus arbitration is determined by the current external bus master and the state of the /BRx pins of each TigerSHARC processor in the multiprocessing system.

A host or a TigerSHARC processor with a higher priority request than the current bus master can gain control of the external bus from the current bus master. A host will assert its /HBR signal to request the external bus. A processor requesting the external bus with a core access will assert its /CPA signal in addition to its /BR signal to signify the high-priority external bus request. A processor requesting the external bus with a DMA access configured for high priority will assert its /DPA signal (but only if /CPA is not asserted) in addition to its /BR signal to signify the high-priority external bus request. The external bus priority in descending order is:

1. Host
2. TigerSHARC processor (/BR and /CPA asserted)
3. TigerSHARC processor (/BR and /DPA asserted)
4. TigerSHARC processor (/BR asserted)

The following sections discuss the effects of normal-priority external bus accesses and high-priority external bus accesses on the external bus arbitration protocol. Example code and resulting waveforms captured from a three-processor system highlight the bus arbitration protocol implemented on the TigerSHARC processor. For more information on the multiprocessing interface and bus arbitration protocol implemented on the TigerSHARC, refer to the External Port and SDRAM Interface chapter in the *ADSP-TS201 TigerSHARC Processor Hardware Reference.*

4 Normal Priority Accesses

4.1 Normal-Priority External Bus Arbitration Sequence: /CPA, /DPA Inactive (no Host Present) (Example 1)

Table 1 shows the external bus settings and the data transfer details for each TigerSHARC processor in Example 1. The captured signals for this example appear in Figure 2.

External Bus Settings	Processor	Data Transfer
Bus width: 64 bits Bus speed: 60 MHz.	A (ID0)	64 normal word external port DMA transfer Quad-word transfer, normal priority
	B (ID1)	64 normal word external port DMA transfer Quad-word transfer, normal priority
	C (ID2)	64 normal word external port DMA transfer Quad-word transfer, normal priority

Table 1. Bus Settings and Data Transfer Details

As shown in Figure 2, processor A (ID0) gains control of the external bus first and completes its DMA transfer. Processor B (ID1) is next to gain control of the external bus and completes its DMA transfer. Processor C (ID2) is next to gain control of the external bus and completes its DMA transfer. Because each of the transfers is an external port DMA transfer with normal priority (and not a core access or host access), the /CPA, /DPA, and /HBR signals (Channel 4) are inactive in this example; thus, the external bus mastership is determined by the Processor IDs (ID0-ID2 in this example).

Example 1 Captured Signals:

Channel	Signal
Channel 1 (Yellow)	Processor A (ID0) /BR0
Channel 2 (Blue)	Processor B (ID1) /BR1
Channel 3 (Pink)	Processor C (ID2) /BR2
Channel 4 (Green)	/CPA, /DPA Inactive

Figure 2. Normal-Priority External Bus Arbitration Sequence: /CPA, /DPA Inactive (no Host present) (Example 1)

5 High-Priority Accesses

The bus arbitration scheme on the TigerSHARC processor allows a host processor to gain temporary priority over the current external bus master. Any TigerSHARC processor in the cluster can also gain temporary access over the current external bus master with a high-priority DMA external port access, or a core access over the external bus, using its corresponding /BR and /DPA or /CPA pins.

5.1 DMA Priority Access (/DPA)

The DMA priority access (/DPA) pin is asserted when a TigerSHARC processor's DMA channel is configured for high priority and accesses the external bus. This allows a DMA channel configured for high priority (belonging to a slave TigerSHARC processor) to interrupt background transfers of a normal-priority DMA channel belonging to a master TigerSHARC processor and gain control of the external bus. In this case, the current external bus master in this case completes its current transaction (normal, long, or quad-word transfer) and passes the external bus mastership to the requesting TigerSHARC processor by de-asserting its /BR.

In a multiprocessing system, when one of the TigerSHARC processors assert the /DPA signal, all TigerSHARC processors with normal-priority DMA transactions de-assert their /BR signals. When more

than one TigerSHARC processor requests the bus by asserting their /BR signals along with /DPA, the TigerSHARC processor with the highest priority gains the bus mastership.

The following two examples highlight the external bus arbitration scheme on the TigerSHARC processor for high-priority DMA accesses over the external port.

5.1.1 High-Priority External Bus DMA Transfer by a TigerSHARC Processor (Processor B) in a Three-Processor Multiprocessing System (Example 2)

Table 2 shows the external bus settings and the data transfer details for each processor in Example 4. In this example, the DMA transfers of processor B and processor C are intentionally delayed by a few cycles to allow processor A's DMA transfer to start. The captured signals for this example appear in Figure 3.

External Bus Settings	Processor	Data Transfer
Bus width: 64 bits Bus speed: 60 MHz.	A (ID0)	External port DMA transfer: 64 words Quad-word transfer, normal priority
	B (ID1)	64 normal word external port DMA transfer Quad-word transfer, high priority
	C (ID2)	64 normal word external port DMA transfer Quad-word transfer, normal priority

Table 2. Bus Settings and Data Transfer Details

As shown in Figure 3, processor A (ID0) gains control of the external bus first and starts its normal-priority DMA transfer. Processor B (ID1) and processor C (ID2) assert their /BR signals after the intentional delay. By means of a high-priority DMA transfer, processor B (ID1) breaks in and gains control of the external bus from processor A and completes its high-priority DMA transfer. Processor B's /DPA (Channel 4 (green)) signal is also asserted, which signifies the high-priority DMA transfer.

Processor A (after completing its current external bus transaction) and processor C de-assert their /BR signals when processor B's /BR and /DPA signals are asserted. When processor B has completed its high-priority DMA transfer, it de-asserts its /BR and /DPA signals. Processor A and processor C then re-assert their /BR signals.

The bus arbitration protocol on the ADSP-TS201 dictates that processor C is next to receive control of the external bus (Figure 3). So, processor C (ID2) gains control of the external bus and completes its normal-priority DMA transfer. Figure 4 shows captured signals from the same example but with Channel 4 (green) set to processor C's /BM signal, showing that processor C has gained control of the external bus. Processor A (ID0), which had not completed its normal-priority DMA transfer when processor B's high-priority DMA transfer occurred gains control of the external bus after processor C and completes its normal-priority DMA transfer.

Example 2 Captured Signals:

Channel	Signal
Channel 1 (Yellow)	Processor A (ID0) /BR0
Channel 2 (Blue)	Processor B (ID1) /BR1
Channel 3 (Pink)	Processor C (ID2) /BR2
Channel 4 (Green)	/DPA

Figure 3. High-Priority External Bus DMA Transfer by a TigerSHARC Processor (Processor B) in a Three-Processor Multiprocessing System (Example 2)

Example 2 Captured Signals:

Channel	Signal
Channel 1 (Yellow)	Processor A (ID0) /BR0
Channel 2 (Blue)	Processor B (ID1) /BR1
Channel 3 (Pink)	Processor C (ID2) /BR2
Channel 4 (Green)	Processor C (ID2) /BM

Figure 4. High-Priority External Bus DMA Transfer by a TigerSHARC Processor (Processor B) in a Three-Processor Multiprocessing System, Showing Processor C's /BM signal (Example 2)

5.1.2 High Priority External Bus DMA Transfer by a TigerSHARC Processor (Processor C) in a Three-Processor Multiprocessing System (Example 3)

Table 3 shows the external bus settings and the data transfer details for each processor in Example 3. In this example, the DMA transfers of processor B and processor C are intentionally delayed by a few

cycles to allow processor A's DMA transfer to start. The captured signals for this example appear in Figure 5.

External Bus Settings	Processor	Data Transfer
Bus width: 64 bits Bus Speed: 60 MHz	A (ID0)	64 normal word external port DMA transfer Quad-word transfer, normal priority
	B (ID1)	64 normal word external port DMA transfer Quad-word transfer, normal priority
	C (ID2)	64 normal word external port DMA transfer Quad-word transfer, high priority

Table 3. Bus Settings and Data Transfer Details

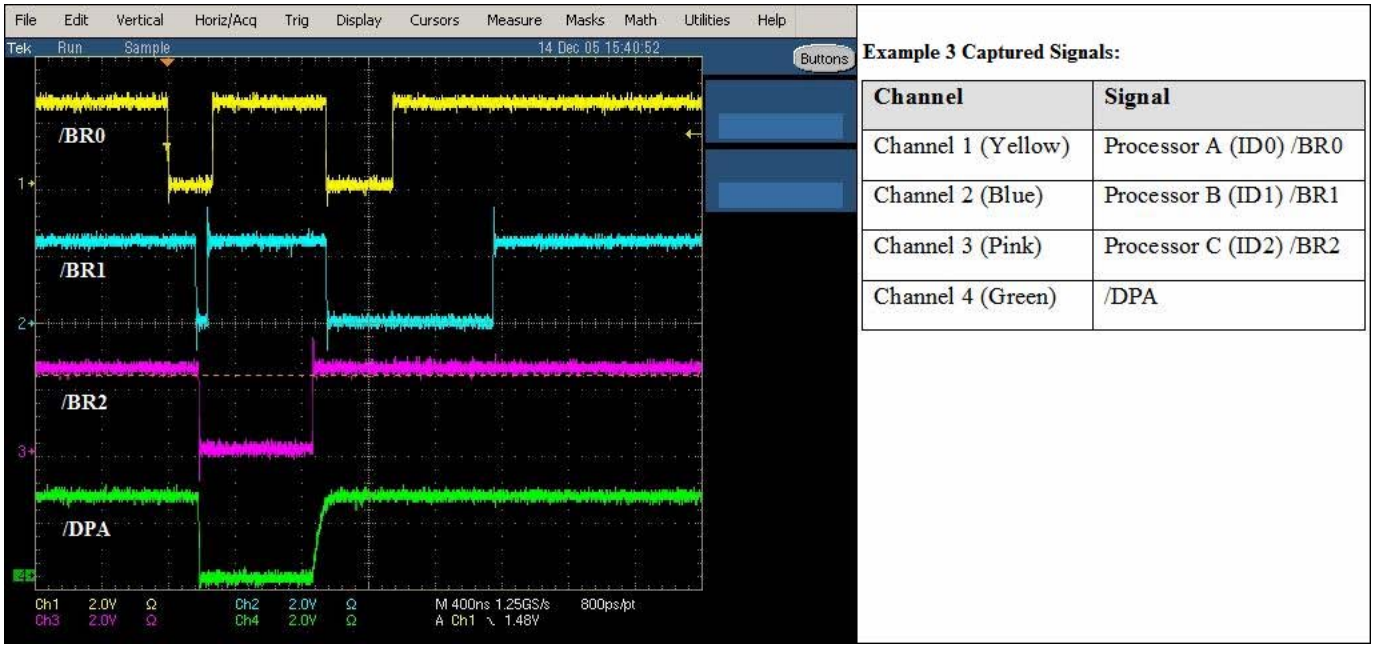


Figure 5. High-Priority External Bus DMA Transfer by a TigerSHARC Processor (Processor C) in a Three-Processor Multiprocessing System (Example 3)

As shown in Figure 5, processor A (ID0) gains control of the external bus first and starts its normal-priority DMA transfer. Processor B (ID1) and processor C (ID2) assert their `/BR` signals after the intentional delay. By means of a high-priority DMA transfer, processor C (ID2) breaks in and gains control of the external bus from processor A and completes its high-priority DMA transfer. Processor C's `/DPA` (Channel 4 (green)) signal is also asserted, which signifies the high-priority DMA transfer.

Processor A (after completing its current external bus transaction) and processor B de-assert their `/BR` signals when processor C's `/BR` and `/DPA` signals are asserted. When processor C has completed its DMA transfer, it de-asserts its `/BR` and `/DPA` signals. Processor A and processor B then re-assert their `/BR` signals. The bus arbitration scheme on the ADSP-TS201 dictates that processor A is next to receive control of the external bus after processor C (ID2) has completed its DMA transfer in this three-processor system as shown in Figure 5. Processor A (ID0) gains control of the external bus and completes its normal-priority DMA transfer. Processor B (ID1), which is next in the arbitration scheme and still waiting

to complete its normal-priority DMA transfer, then gains control of the external bus after processor A and completes the DMA transfer.

5.2 Core Priority Access (/CPA)

The core priority access (/CPA) pin is asserted when the TigerSHARC processor core accesses the external bus. This allows a slave TigerSHARC processor to interrupt background transfers of a DMA channel belonging to a master TigerSHARC processor and gain control of the external bus.

After completing the current transaction (a normal, long, or quad-word transfer), the current TigerSHARC external bus master passes the external bus mastership to the requesting TigerSHARC processor by de-asserting its /BR. In a multiprocessing system, when one TigerSHARC processor asserts the /CPA signal, TigerSHARC processors with DMA transactions de-assert their /BR signals (and /DPA signals in high-priority DMA transactions). When more than one TigerSHARC processor requests the bus by asserting its /BR and /CPA, the TigerSHARC processor with the highest priority gains bus mastership.

The following two examples highlight the external bus arbitration scheme on the TigerSHARC processor for core priority accesses over the external port.

5.2.1 Core Access Over the External Bus by a TigerSHARC Processor in a Three-Processor Multiprocessing System (Example 4)

Table 4 shows the external bus settings and the data transfer details for each processor in Example 4. The data transfers of processor B and processor C are intentionally delayed by a few cycles to allow processor A's DMA transfer to start. The captured signals for this example appear in Figure 1.

External Bus Settings	Processor	Data Transfer
Bus width: 64 bits Bus speed: 60 MHz.	A (ID0)	64 normal word external port DMA transfer Quad-word transfer, normal priority
	B (ID1)	Core data transfer to another processor's internal memory over the external bus
	C (ID2)	64 normal word external port DMA transfer Quad-word transfer, normal priority

Table 4. Example 4—Bus Settings and Data Transfer Details

As shown in Figure 6, processor A (ID0) gains control of the external bus first and starts its normal-priority DMA transfer. Processor B (ID1) is attempting to acquire the external bus for a core access and will therefore assert both of its corresponding /BR and /CPA signals. Processor C (ID2) asserts its /BR signal to signify its DMA data transfer. The assertion of /CPA causes processor C to de-assert its /BR because it is not attempting a core access over the cluster bus. For the same reason, processor A also de-asserts its /BR (after completing its current external bus transaction) thus relinquishing the bus to processor B. When processor B has completed its core access over the external bus, it de-asserts its /BR and /CPA signals. Processor A and processor C then re-assert their corresponding /BR signals.

The bus arbitration scheme on the ADSP-TS201 dictates that processor C is next to receive control of the external bus (Figure 6). So, processor C (ID2) gains control of the external bus and completes its normal-priority DMA transfer. Figure 7 shows captured signals from the same example but with Channel 4 (green) set to processor C's /BM signal, showing that processor C has gained control of the external bus. Processor A (ID0), which had not completed its normal-priority DMA transfer when processor B's high-

priority DMA transfer occurred, gains control of the external bus after processor C and completes its normal-priority DMA transfer.

Example 4 Captured Signals:

Channel	Signal
Channel 1 (Yellow)	Processor A (ID0) /BR0
Channel 2 (Blue)	Processor B (ID1) /BR1
Channel 3 (Pink)	Processor C (ID2) /BR2
Channel 4 (Green)	/CPA

Figure 6. Core Access Over the External Bus by a TigerSHARC Processor in a Three-Processor Multiprocessing System (Example 4)

Example 4 Captured Signals:

Channel	Signal
Channel 1 (Yellow)	Processor A (ID0) /BR0
Channel 2 (Blue)	Processor B (ID1) /BR1
Channel 3 (Pink)	Processor C (ID2) /BR2
Channel 4 (Green)	Processor C (ID2) /BM

Figure 7. Core Access Over the External Bus by a TigerSHARC Processor in a Three-Processor Multiprocessing System, Showing Processor C's /BM signal (Example 4)

5.2.2 Core Accesses over External Bus by two TigerSHARC processors in a three TigerSHARC Processor Multiprocessing System (Example 5)

Table 5 shows the external bus settings and the data transfer details for each processor in Example 3. Processor B and processor C core accesses to another processor over the external bus are intentionally delayed by a few cycles to allow processor A's DMA transfer to start. The captured signals for this example appear in Figure 8.

External Bus Settings	Processor	Data Transfer
Bus width: 64 bits Bus speed: 60 MHz.	A (ID0)	64 normal word external port DMA transfer Quad-word transfer, normal priority
	B (ID1)	Core data transfer to another processor's internal memory over the external bus
	C (ID2)	Core data transfer to another processor's internal memory over the external bus

Table 5. Example 5 Bus Settings and Data Transfer Details

As shown in Figure 8, processor A (ID0) gains control of the external bus first and starts its normal-priority DMA transfer. Processor B (ID1) and processor C (ID2) assert their `/BR` and `/CPA` signals after the intentional delay to signify their core accesses to other processors in the cluster over the external bus. Because the core accesses over the external bus have a higher priority than processor A's normal-priority DMA transfer, processor B (ID1), which has the highest ID priority, gains control of the external bus and performs its core access over the external bus. Processor A de-asserts its `/BR` signal (after completing its current external bus transaction).

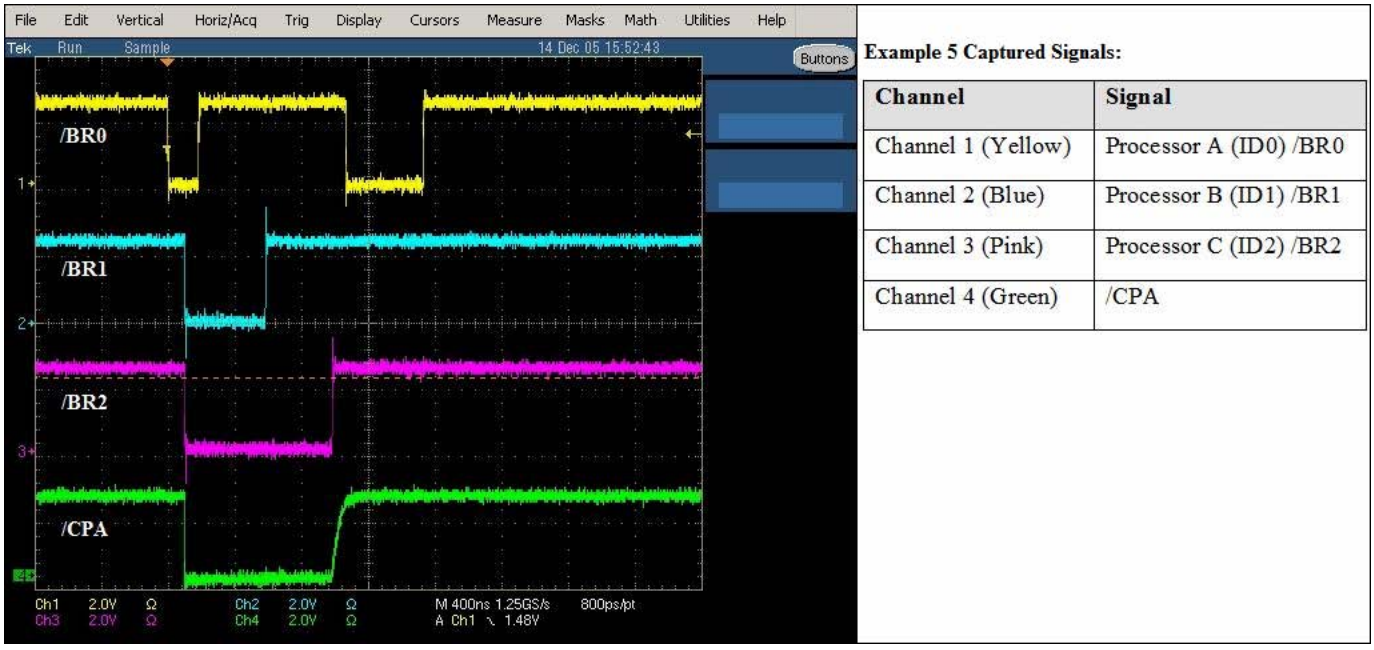


Figure 8. Core Accesses Over External Bus by Two TigerSHARC Processors in a Three-Processor Multiprocessing System (Example 5)

When processor B (ID1) completes its core access over the external bus, it de-asserts its `/BR` and processor C (ID2) gains control of the external bus and performs its core access. The `/CPA` signal

(Channel 4 (green)) remains asserted. When processor C completes its core access over the external bus, it de-asserts its /BR and the /CPA signal is also de-asserted. Processor A (ID0), which had not completed its normal-priority DMA transfer, then regains control of the external bus after processor C (ID2) and completes its normal-priority DMA transfer.

5.3 /DPA and /CPA Accesses in a TigerSHARC Multiprocessing System

In a TigerSHARC processor cluster system, the requesting bus agents with an active /CPA have higher priority over requesting the bus agents with an active /DPA. So, requesting bus agents with an active /DPA de-assert their /BR signals (and /DPA signals) upon sensing that a /CPA is asserted by other bus agents.

The following three examples highlight how the external bus arbitration scheme on the TigerSHARC processor functions when there are both /CPA and /DPA accesses in a TigerSHARC processor cluster system.

5.3.1 High-Priority DMA Transfer, Core Access Over the External Bus in a TigerSHARC Processor Multiprocessing System (Example 6)

Table 6 shows the external bus settings and the data transfer details for each processor in Example 6. In this example, processor B's core accesses are intentionally delayed by a few cycles to allow processor A's DMA transfer to start. The captured signals for this example appear in Figure 9.

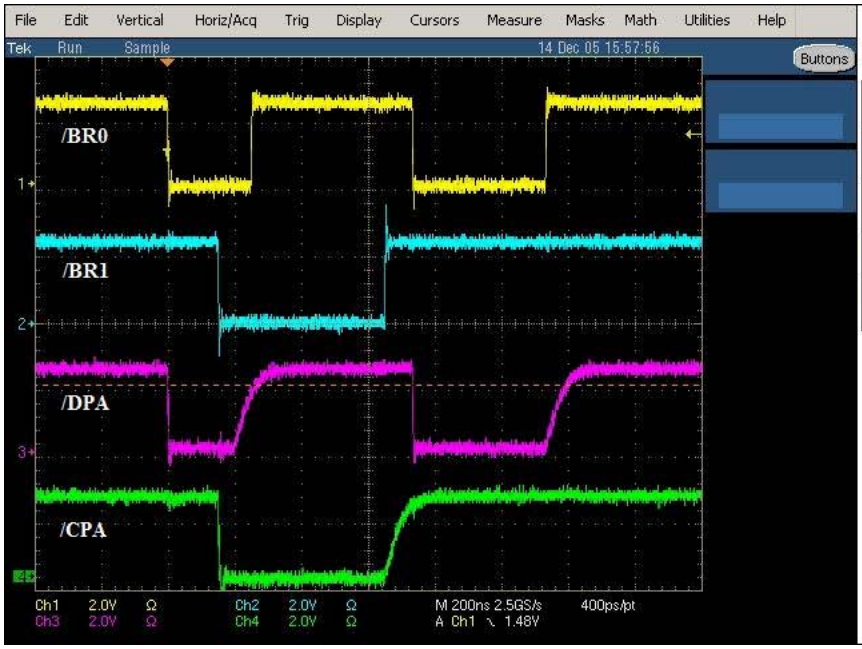
External Bus Settings	Processor	Data Transfer
Bus width: 64 bits Bus speed: 60 MHz.	A (ID0)	64 normal word external port DMA transfer Quad-word transfer, high priority
	B (ID1)	Core data transfer to another processor's internal memory over the external bus
	C (ID2)	Idle

Table 6. Example 6—Bus Settings and Data Transfer Details

As shown in Figure 9, processor A (ID0) gains control of the external bus first and starts its high-priority DMA transfer. Processor A's /DPA signal is also asserted to signify the high-priority DMA transfer. Processor B (ID1) asserts its /BR signal after the intentional delay to signify its core accesses to processor A over the external bus. Processor B's /CPA signal is also asserted, which signifies the core access over the external bus.

Processor A recognizes the higher priority core access over the external bus from processor B and relinquishes control of the external bus by de-asserting its /BR and /DPA signals (after completing its current external bus transaction). Processor B completes its core accesses to processor A over the external bus and de-asserts its /BR and /CPA signals.

Processor A, which had not completed its high-priority DMA transfer, then re-asserts its /BR and /DPA signals and completes its transfer. Figure 10 shows another screen capture of the same signals for the same example.



Example 6 Captured Signals:

Channel	Signal
Channel 1 (Yellow)	Processor A (ID0) /BR0
Channel 2 (Blue)	Processor B (ID1) /BR1
Channel 3 (Pink)	/DPA
Channel 4 (Green)	/CPA

Figure 9. High-Priority DMA Transfer, Core Access Over the External Bus in a TigerSHARC Processor Multiprocessing System (Example 6)

Example 6 Captured Signals:

Channel	Signal
Channel 1 (Yellow)	Processor A (ID0) /BR0
Channel 2 (Blue)	Processor B (ID1) /BR1
Channel 3 (Pink)	/DPA
Channel 4 (Green)	/CPA

Figure 10. High-Priority DMA Transfer, Core Access Over the External Bus in a TigerSHARC Processor Multiprocessing System (Example 6)

5.3.2 High-Priority DMA Transfer, Core Access, Normal-Priority DMA Transfer Over the External Bus in a Three-Processor Multiprocessing System (Example 7)

Table 7 shows the external bus settings and the data transfer details for each processor in Example 7. In this example, processor B's core accesses and processor C's normal DMA transfer are intentionally

delayed by a few cycles to allow processor A's DMA transfer to start. The captured signals for this example appear in Figure 11.

External Bus Settings	Processor	Data Transfer
Bus width: 64 bits Bus speed: 60 MHz.	A (ID0)	64 normal word external port DMA transfer Quad-word transfer, high priority
	B (ID1)	Core data transfer to another processor's internal memory over the external bus
	C (ID2)	64 normal word external port DMA transfer Quad-word transfer, normal priority

Table 7. Example 7—Bus Settings and Data Transfer Details

As shown in Figure 11, processor A (ID0) gains control of the external bus first and starts its high-priority DMA transfer. Processor A's /DPA signal is also asserted to signify the high-priority DMA transfer.

Processor B (ID1) asserts its /BR signal after the intentional delay to signify its core accesses to processor A over the external bus. Processor B's /CPA signal (not shown in Figure 11) is also asserted, which signifies the core access over the external bus. Processor A recognizes the higher priority core access from processor B and relinquishes control of the external bus by de-asserting its /BR and /DPA signals (after completing its current external bus transaction). Processor B completes its core accesses to processor A over the external bus and de-asserts its /BR and /CPA signals.

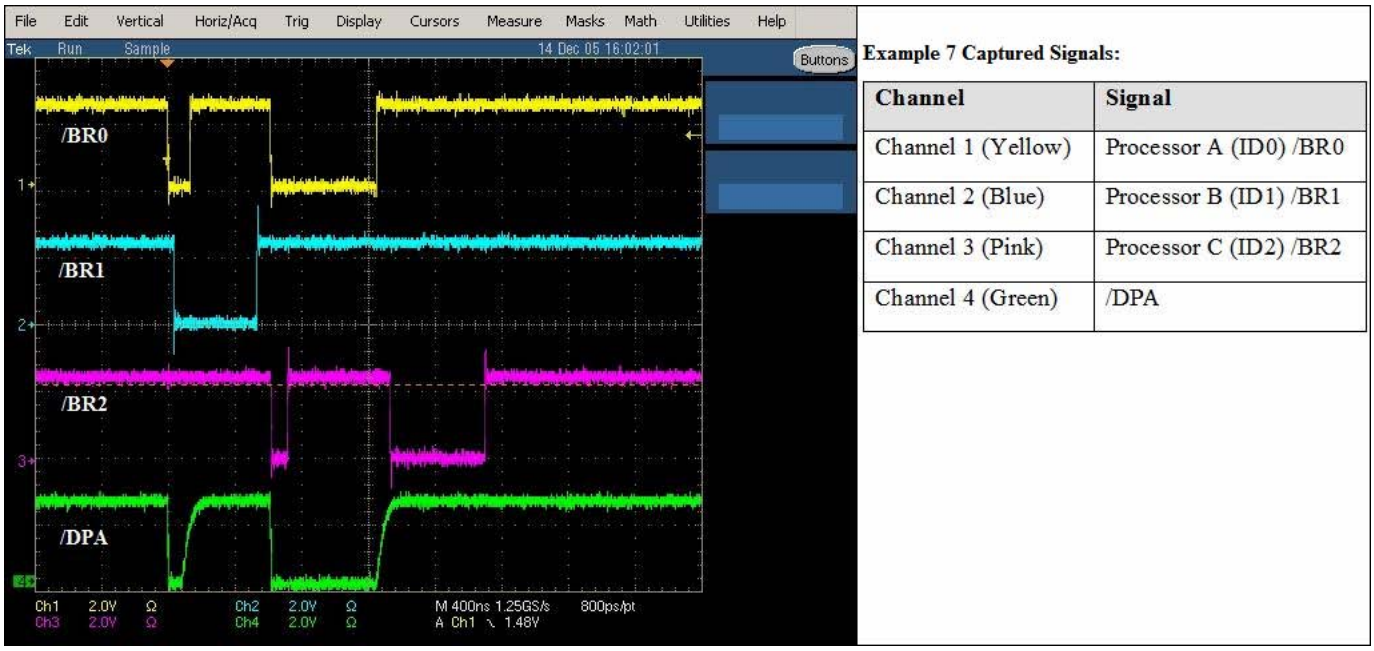


Figure 11. High-Priority DMA Transfer, Core Access, Normal-Priority DMA Transfer Over the External Bus in a Three-Processor Multiprocessing System (Example 7)

Processor A and processor C assert their /BR signals, and processor A also asserts its /DPA signal. Processor C is next after processor B in the ADSP-TS201 arbitration scheme but recognizes that processor A has a high-priority DMA transfer and de-asserts its /BR signal. Processor A completes its high-priority DMA transfer and de-asserts its /BR and /DPA signals. Processor B is not requesting the bus

at this time and so processor C gains control of the external bus and completes its normal-priority DMA transfer.

Figure 12 shows the captured signals for the same example, but shows processor C's /BM signal.

Example 7 Captured Signals:

Channel	Signal
Channel 1 (Yellow)	Processor A (ID0) /BR0
Channel 2 (Blue)	Processor B (ID1) /BR1
Channel 3 (Pink)	Processor C (ID2) /BR2
Channel 4 (Green)	Processor C (ID2) /BM

Figure 12. High-Priority DMA Transfer, Core Access, Normal-Priority DMA Transfer Over the External Bus in a Three-Processor Multiprocessing System, Showing Processor C's /BM signal (Example 7)

5.3.3 High-Priority DMA Transfer, Core Access, High-Priority DMA Transfer Over the External Bus in a Three-Processor Multiprocessing System (Example 8)

Table 8 shows the external bus settings and the data transfer details for each processor in Example 9. In this example, processor B's core accesses and processor C's normal DMA transfer are intentionally delayed by a few cycles to allow processor A's DMA transfer to start. The captured signals for this example appear in Figure 13.

External Bus Settings	Processor	Data Transfer
Bus width: 64 bits Bus speed: 60 MHz.	A (ID0)	64 normal word external port DMA transfer Quad-word transfer, high priority
	B (ID1)	Core data transfer to another processor's internal memory over the external bus
	C (ID2)	64 normal word external port DMA transfer Quad-word transfer, high priority

Table 8. Example 8—Bus Settings and Data Transfer Details

As shown in Figure 13, processor A (ID0) gains control of the external bus first and starts its high-priority DMA transfer. Processor A's /DPA signal is also asserted to signify the high-priority DMA transfer. Processor B (ID1) asserts its /BR signal after the intentional delay to signify its core accesses to processor A over the external bus. Processor B's /CPA signal (not shown) is also asserted, which signifies the core access over the external bus. Processor A recognizes the higher priority core access from

processor B and relinquishes control of the external bus by de-asserting its /BR and /DPA signals (after completing its current external bus transaction). Processor B completes its core accesses to processor A over the external bus and de-asserts its /BR and /CPA signals.

Processor A and processor C assert their /BR and /DPA signals. Processor C, which is next after processor B in the ADSP-TS201 arbitration scheme, completes its high-priority DMA transfer and de-asserts its /BR and /DPA signal. Processor A completes its high-priority DMA transfer and de-asserts its /BR and /DPA signals. The /DPA signal (Channel 4 (green)) remains asserted for the high-priority DMA transfers of both processor C and processor A because the /DPA signals are tied together on this board. Figure 14 shows the captured signals for the same example, but shows processor C's /BM signal.

Example 8 Captured Signals:

Channel	Signal
Channel 1 (Yellow)	Processor A (ID0) /BR0
Channel 2 (Blue)	Processor B (ID1) /BR1
Channel 3 (Pink)	Processor C (ID2) /BR2
Channel 4 (Green)	/DPA

Figure 13. High-Priority DMA Transfer, Core Access, High-Priority DMA Transfer Over the External Bus in a Three-Processor Multiprocessing System (Example 8)

5.4 Host Accesses

The host can be a bus master on the TigerSHARC processor's external bus—it uses /HBR and /HBG to gain control of the bus. In order for the host to become bus master, the host must assert /HBR and wait until /HBG is asserted by the current TigerSHARC processor master. The TigerSHARC processor relinquishes the external bus and indicates this by asserting /HBG.

After completing all outstanding transactions, the host keeps /HBR asserted for as long as it needs the bus. The master that last relinquished the bus keeps its /BR line asserted, so that when the host de-asserts /HBR, it becomes the master again.

Example 8 Captured Signals:

Channel	Signal
Channel 1 (Yellow)	Processor A (ID0) /BR0
Channel 2 (Blue)	Processor B (ID1) /BR1
Channel 3 (Pink)	Processor C (ID2) /BR2
Channel 4 (Green)	Processor C (ID2) /BM

Figure 14. High-Priority DMA Transfer, Core Access, High-Priority DMA Transfer Over the External Bus in a Three-Processor Multiprocessing System, Showing Processor C's /BM signal (Example 8)

6 Conclusion

This EE-Note discusses the TigerSHARC multiprocessing interface and how each TigerSHARC processor and host in a TigerSHARC multiprocessing system arbitrates for the use of the shared external bus in the multiprocessing system. Accompanying example code and resulting waveforms captured from a three-processor system highlight the bus arbitration scheme.

7 References

[1] *ADSP-TS201 TigerSHARC Processor Hardware Reference.* Rev.1.1, December 2004. Analog Devices, Inc.

[2] *ADSP-TS201 TigerSHARC Processor Programming Reference.* Rev.1.1, April 2004. Analog Devices, Inc.

8 Document History

Revision	Description
Rev 1 – February 10, 2006 *by S. Francis*	Initial Release