SFP Reference Design Kit

Preliminary Technical Data

FEATURES

Small Form-factor Pluggable (SFP) MSA compliant
SFF-8472 Digital Diagnostic Monitoring
Multi-Rate from 155Mbps to 4.25Gbps
Internal Calibration
Closed-Loop control of extinction ratio(ADN2870)
Build-in LOS/RSSI detectors (ADN2891/2)
Embedded MCU, MicroConverter®(ADuC7020):
- 16/32-bit RISC ARM7TDMI core, 45MIPS peak
- 5 channels 12-bit ADC
- 4 x 12-bit DACs
- On-chip Power Supply Monitor
- On-chip Temperature Monitor
- Programmable Logic Array
- 62K Bytes EEPROM, 8K Bytes SRAM
- Four I^2C Device Addressing

APPLICATONS

Multi-rate OC-3 to OC-48FEC SFP/SFF Modules
1x/2x/4x Fibre Channel Modules
Gigabit Ethernet Modules

DESCRIPTION

The SFP Reference Design Kit(SFP-RDK) provides a complete optical transceiver chipset and system-level solution for designers. The SFP-RDK includes:
- SFP Transceiver Module Board
- SFP Host Board
- JTAG Adapter board
- PCB Schematics
- PCB Layout , Gerber Files, CAD Files
- Bill of Materials
- SFP Firmware Source Code in ANSI C
- Evaluation GUI software
- Applications Note(AN-706), User Manuals

The SFP-RDK consists of Analog Devices' optical transceiver chip set: the ADN2870 dual loop laser driver, the ADN2880/2 Transimpedance amplifier, the ADN2891/2 Limiting amplifier and the ADuC7020 MicroConverter®. Use of the micro-controller allows flexible module designs support user definable functions.

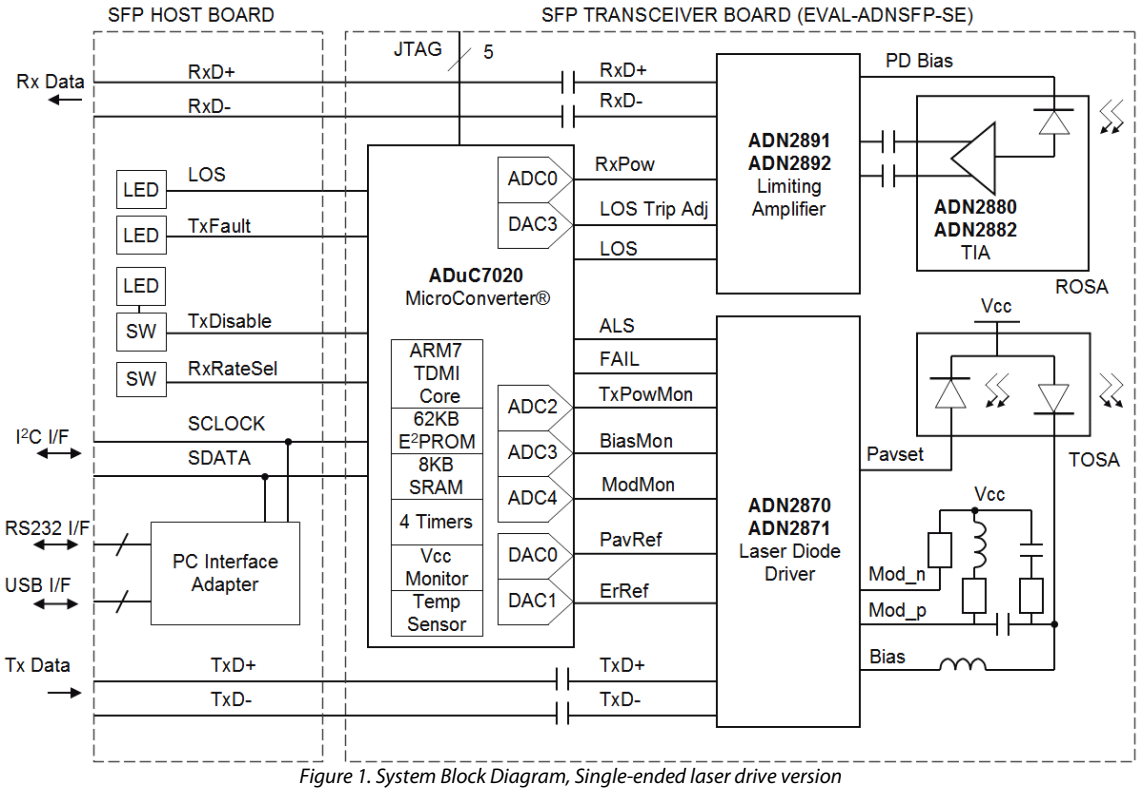

Figure 1. System Block Diagram, Single-ended laser drive version

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ELECTRICAL CHARACTERISTICS

(T_A= T_{MAX} to T_{MIN}, V_{CC}= 3.1V to 3.5V, unless otherwise noted, refer to individual datasheets)

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
POWER SUPPLY					
Supply Voltage	3.10		3.50	V	
Power Dissipation					2.488Gbps, PRBS2^23-1
MicroConverter (ADuC7020)		3		mA	Normal Mode, 1MHz Clock
		TBD		mA	Average power
Laser Driver (ADN2870)		30		mA	TX_Disable asserted
Limiting Amplifier (ADN2871)		TBD		mA	TX_Disable asserted
Limiting Amplifier (ADN2891)		44	60	mA	
Limiting Amplifier (ADN2892)		50		mA	
Transimpedance Amplifier (ADN2880)	50	75	120	mA	I_{INAVE} = 0 mA
Transimpedance Amplifier (ADN2882)		TBD		mA	I_{INAVE} = 0 mA
TRANSMITTER					
Laser Bias Current	2		100	mA	
Laser Modulation Current	5		90	mA	
Differential Input Data Voltage	0.4		2.4	Vp-p	
TX Fault Output Low Voltage			0.8	V	
TX Fault Output High Voltage	2.4			V	
TX Disable Input Low Voltage			0.8	V	
TX Disable Input High Voltage	2.4			V	
RECEIVER					
Differential Output Data Voltage	650	700	800	mVp-p	
LOS Output Low Voltage			0.8	V	
LOS Output High Voltage	2.4			V	
Random Jitter		2	5	ps RMS	Input>10mVp-p, OC-48, PRBS2^{23}-
Deterministic Jitter		13.7	19	ps p-p	Input>10mVp-p, OC-48, PRBS2^{23}-

TIMING CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Serial ID Clock Range			100	KHz	
Tx Disable Assert Time			10	µs	
Tx Disable Negate Time			1	ms	
Time to Initialize, including Reset of TX_FAULT			300	ms	
Tx Fault Assert Time			100	µs	
TX Disale to Reset	10				
LOS Assert Time		600		µs	
LOS Deassert Time		100		µs	
RX Data Output Rise Time		65		ps	20%-80%
RX Data Output Fall Time		65		ps	20%-80%

Ordering Guide

Model	Description	Supported Data Rates	Supported Lasers	PC Board	IC's
EVAL-ADNSFP-SE	Single-ended laser drive	OC-3 to OC-48FEC 100/1000 Ethernet	FP/DFB/VCSEL	V1.3	ADN2891 ADN2880 ADN2870 ADuC7020
EVAL-ADNSFP-Diff	Differential laser drive	OC-3 to OC-48FEC Rate to 3.3Gbps	FP/DFB/VCSEL	V1.4	ADN2891 ADN2880 ADN2870 ADuC7020
EVAL-ADNSFP-FC	Differential laser driver	100/1000 Ethernet 1x/2x/4x Fiber Channel	FP/DFB/VCSEL	V1.4	ADN2892 ADN2882 ADN2870 ADuC7020

Note: The EVAL-ADNSFP-FC will support the ADN2891 Limiting Amp pinout and functionality allowing this board to handle SONET data.

Selection Guide

Model	EVAL-ADNSFP-SE	EVAL-ADNSFP-Diff	EVAL-ADNSFP-FC
Receive Section			
Max Data Rate	3.3G	3.3G	4.25G
ROSA TIA	ADN2880ACPZ	ADN2880ACPZ	ADN2882ACPZ
Limiting Amp	ADN2891ACPZ	ADN2891ACPZ	ADN2892ACPZ
LOS Range	3mV to 50mV	3mV to 50mV	3mV to 50mV
Protocols Supported	SONET, 8B/10B	SONET, 8B/10B	8B/10B
Transmit Section			
Max Data Rate	4.25G	4.25G	4.25G
Laser Control	Dual Loop	Dual Loop	Dual Loop
Laser Drive Circuit	Single Ended	Single Ended	Differential
LDD	ADN2870ACPZ	ADN2870ACPZ	ADN2870ACPZ
Supported Lasers	FP/DFB/VCSEL	FP/DFB/VCSEL	FP/DFB/VCSEL
Protocols Supported	SONET, 8B/10B	SONET, 8B/10B	SONET, 8B/10B
Laser	TBD	TBD	AOC 5962-581
Supervisor			
Supervisor	ADuC7020ACPZ	ADuC7020ACPZ	ADuC7020ACPZ
Recommended Usage			
OC-3 to OC-48 Single Rate Modules	√	√	
OC-3 to OC-48 Multi Rate Modules	√	√	
1GE Modules	√	√	√
1X/2X/4X Fiber Channel Modules			√
LX4 Modules	√*	√*	
DWDM SFP	√*	√*	

√* The SFP Reference Design can provide a performance benchmark for these types of modules.

The Analog Devices SFP Reference Design is available in several configuration depending on the end application. The primary differences are related to the speed of the receive section, and the configuration of the laser driver interface circuit.

Receive Section:
–SE and –Diff versions are design to work with SONET data at rates less than 3.3G; they will also support 8B/10B encoded data.
–FC version features a limiting amp and TIA that support rates up to 4.25G and 8B/10B encoded data. The limiting amplifier in the –FC version (ADN2892) has a BW select feature to improve sensitivity for 1X FC and 1GE data rates, and can filter relaxation oscillations from legacy CD lasers used in older fiber channel modules.

Transmit Section
The –SE version has a typical single ended drive circuit. The differential driver circuit in the –Diff and –FC versions can produce superior transmit eye quality by improving fall times to increase eye margin. This is particularly important when driving VCSELs that can have slow fall time performance. All three boards will support FP/DFP or VCSEL lasers.

Module Board Optical Edge Pad Dimensions and Placement

Viewed from ROSA/TOSA to board edge.
All dimensions are in millimeters

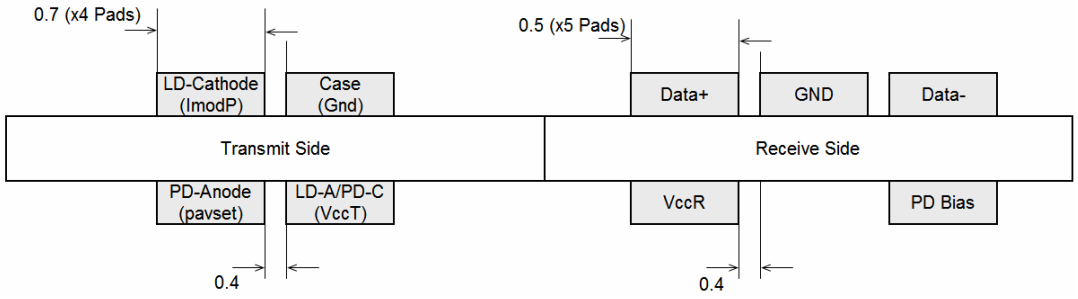


Figure 2. Edge pin configuration PC Board V1.3 (EVAL-ADNSFP-SE)

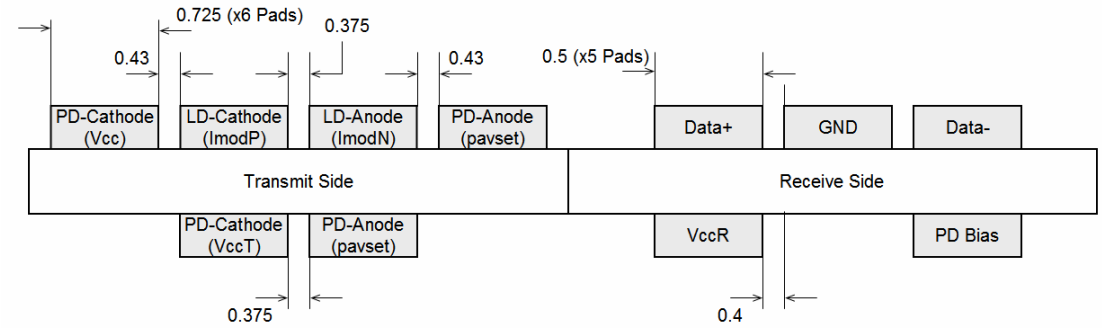


Figure 3. Edge pin configuration PC Board V1.4 (EVAL-ADNSFP-Diff/-FC)

Board Outlines

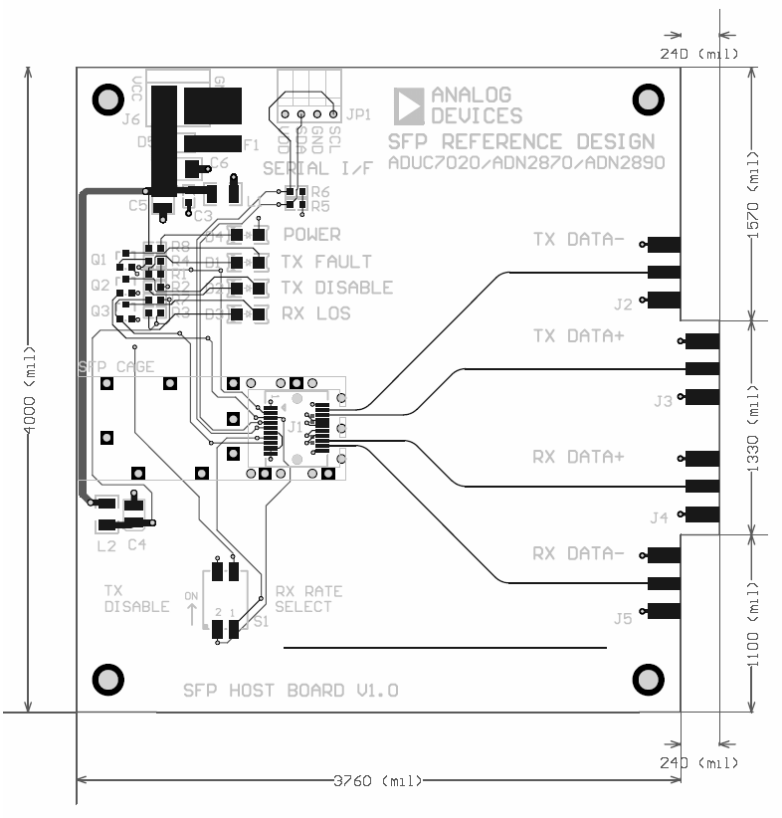


Figure 4. SFP Host Board

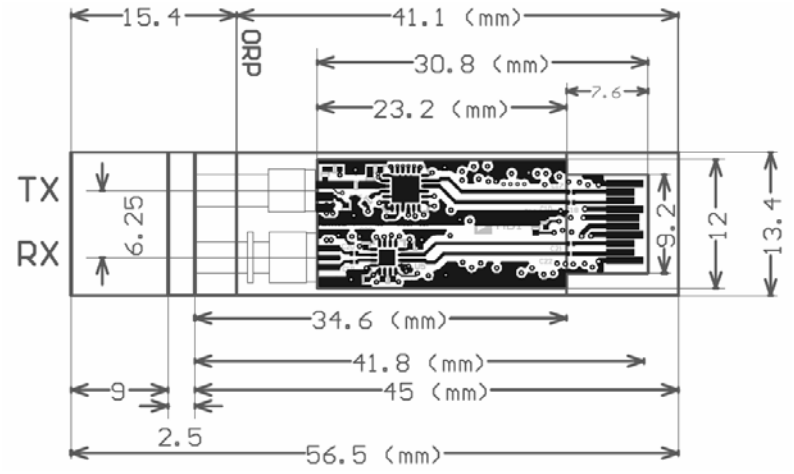


Figure 5. SFP Module Board V1.3 (Top side)

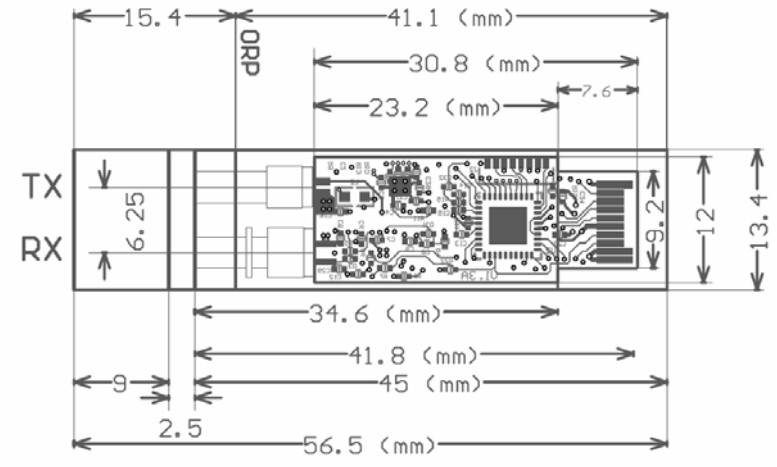


Figure 6. SFP Module Board V1.3 (Bottom side)

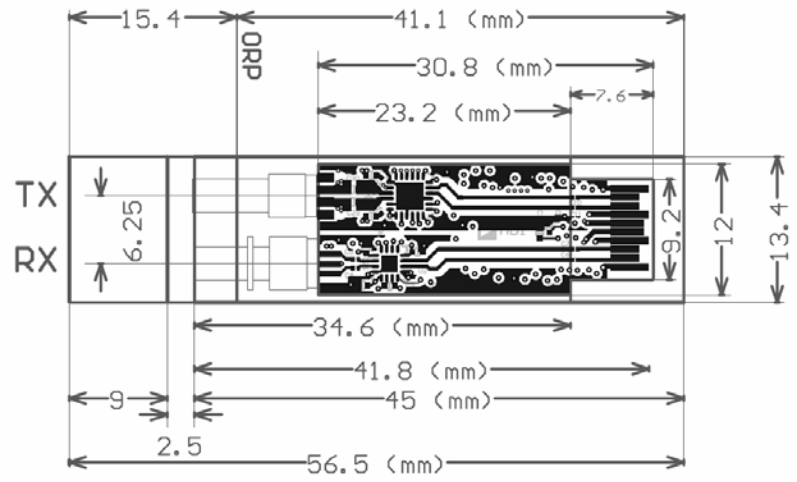


Figure 7. SFP Module Board V1.4 (Top side)

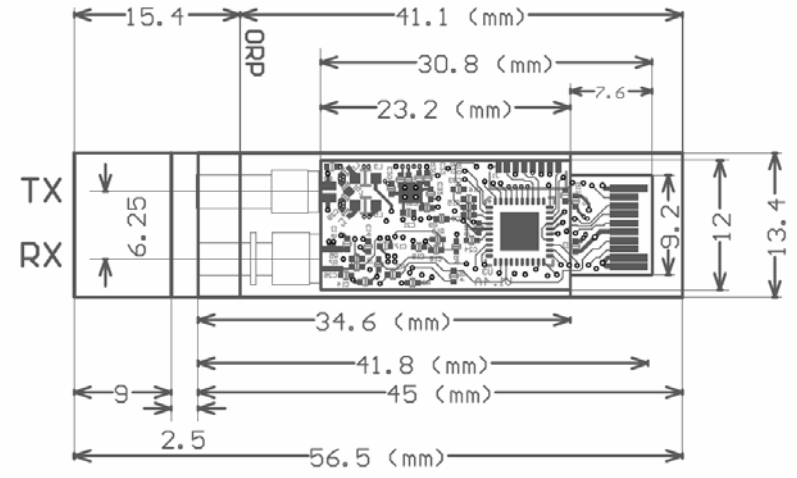
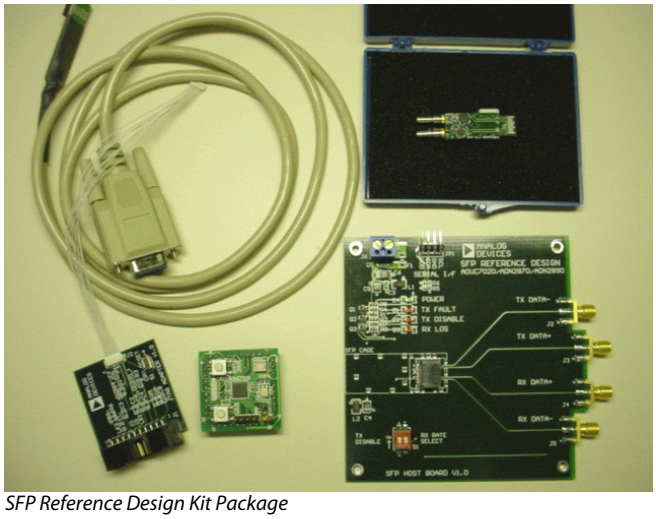


Figure 8. SFP Module Board V1.4 (Bottom side)

Contents of SFP Reference Design Kit Package

The SFP-RDK package contains the following items.

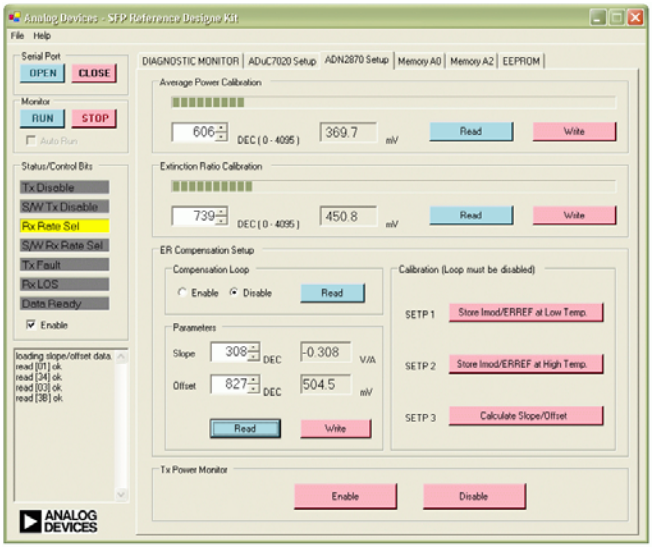
- SFP Module Board with TOSA and ROSA
- SFP Host Board
- GUI Adapter Board (RS232-to-I2C, ADuC7020-MiniEval)
- JTAG Adapter Board
- RS-232 Cable (MicroConverter Dongle Cable)
- Test Report
- CD containing:
  - Firmware source files
  - GUI software files
  - GUI driver files



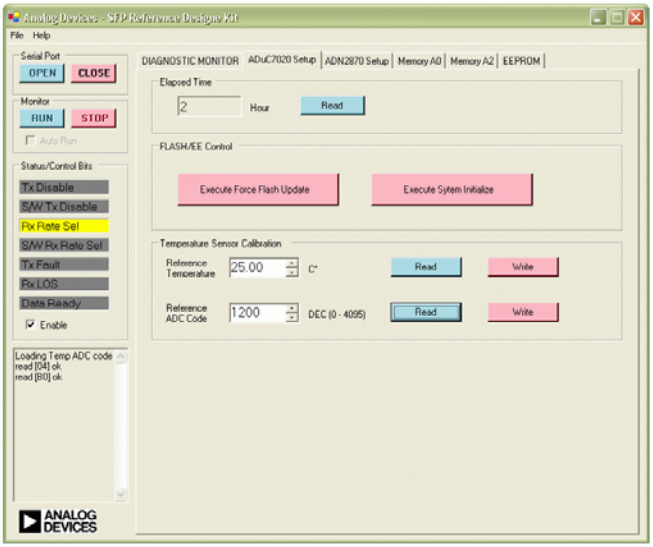
SFP Reference Design Kit Package

GUI

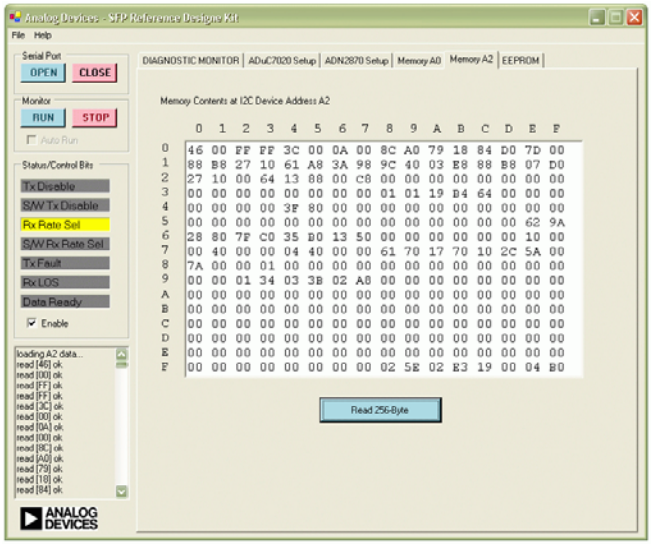
SFF-8472 Diagnostic Window



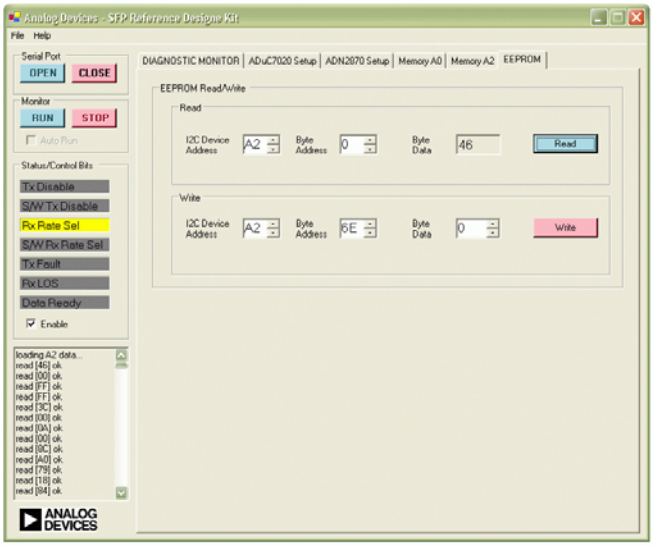
ADN2870 Setup Window



ADuC7020 Setup Window



A0h and A2h Memory Windows



EEPROM Read and Write Window

PR05288-0-11/04(PrA)