ANALOG DEVICES

AN-831
APPLICATION NOTE

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Implementing a Counter with the ADuC702x Family

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INTRODUCTION

The ADuC702x family has an on-chip programmable logic array that consists of 16 gates with flip-flops on the output. This glue logic can be used for different functions. This application note describes how to implement a 3-bit counter but it can also apply to a simple sequence generation.

THE PLA

The programmable logic array (PLA) can be described as glue logic and its function is to remove the requirement for simple external logic. It consists of two independent blocks of eight elements. The two blocks can have different clocks, however, each element within a block uses the same block clock.

Each of the 16 elements contains a two-input look-up table and a flip-flop. The look-up table can be configured to generate any logic function based on one or two inputs. The flip-flop can be clocked with the block clock or it can be bypassed.

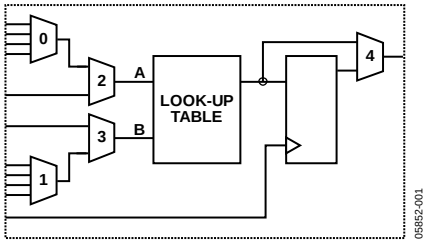

Figure 1. PLA Element

SYNCHRONOUS COUNTER

The flip-flops in a synchronous counter all receive the same clock signal. To implement a three-bit counter, three flip-flops and three outputs are required, as well as some logic to determine the next state (see Table 1 and Table 2).

Table 1. Transition Table

	Actual Outputs			Next Outputs		
State	Q_2	Q_1	Q_0	D_2	D_1	D_0
0	0	0	0	0	0	1
1	0	0	1	0	1	0
2	0	1	0	0	1	1
3	0	1	1	1	0	0
4	1	0	0	1	0	1
5	1	0	1	1	1	0
6	1	1	0	1	1	1
7	1	1	1	0	0	0

Table 2. Functions

		Q_1, Q_0			
D_2		00	01	11	10
Q_2	0	0	0	1	0
	1	1	1	0	1

$$D_2 = \overline{Q_2}Q_1Q_0 + Q_2\overline{Q_1} + Q_2\overline{Q_0}$$

		Q_1, Q_0			
D_1		00	01	11	10
Q_2	0	0	1	0	1
	1	0	1	0	1

$$D_1 = Q_1\overline{Q_0} + \overline{Q_1}Q_0 = Q_1 \oplus Q_0$$

$$D_0 = \overline{Q_0}$$

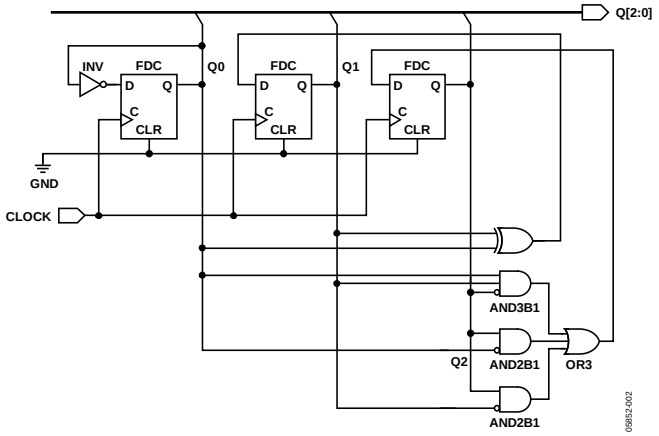

Figure 2. Schematic

IMPLEMENTATION ON THE ADUC702x

To implement a three-bit counter, three flip-flops and three general-purpose outputs are required.

Because each PLA element contains only a two input gate, the three input gates need to be replaced with two input gates.

D_2 can also be written as

$$D_2 = \overline{Q_2}Q_1Q_0 + Q_2\overline{Q_1} + Q_2\overline{Q_0} = \overline{Q_2}Q_1Q_0 + Q_2\overline{Q_1Q_0}$$

This can easily be implemented with two input gates.

Note that the clock used for the flip-flops is fully programmable. It can be one of three GPIOs: the HCLK, internal oscillator, or Timer 1 overflow. The Timer 1 overflow offers a great deal of flexibility with four clock sources, a prescaler, and a 32-bit counter.

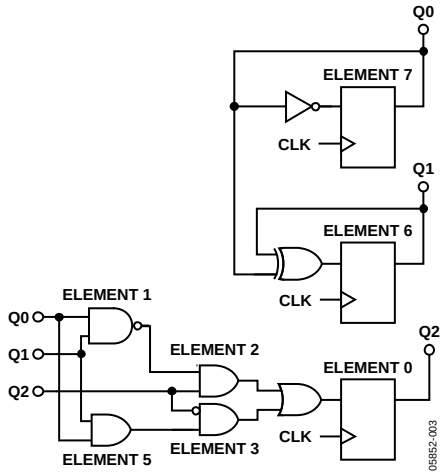

Figure 3. Implementation Using the PLA Tool

CONCLUSION

There are three main advantages to implementing a 3-bit counter using the PLA:

- There is no requirement for an external component.
- As an integrated solution, no processing power is required.
- The clock is fully programmable, with no requirement for an external clock signal.

This application note only discusses the case of a 3-bit counter. However, any simple sequence generation can be easily implemented using the same technique.

The main disadvantage of this technique is due to the limited number of gates and outputs available on the part.

The graphical PLA configuration tool is available to download on Analog Devices' website, www.analog.com.

Table 3. Relevant Extract from Companion Code PLAinit.c

```
//Code Generated By the ADuC 702X PLA Tool
//FileType:        C PLA Configuration File
//Source:          C Source Code
//Date:                  24/10/2005 22:20:13
//================================================================
#include "ADuC7026.h"
void   plaInitialize( )
{
      // Configure Port Pins for PLA mode

//          In order for the PLA Tool to configure the required GPIO pins
//          you must make the necessary selections on the outputs tab!!!
GP1CON = 0x30000000;
GP2CON = 0x00000330;

      // Configure individual elements

      PLAELM0 = 0x02DC;
      PLAELM1 = 0x07CF;
      PLAELM2 = 0x0051;
      PLAELM3 = 0x0145;
      PLAELM5 = 0x07D1;
      PLAELM6 = 0x07CC;
      PLAELM7 = 0x018A;

      // Clk Source configuration

      PLACLK = 0x0004;

}
```

NOTES

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