EVAL-ADuC7026 User Guide
UG-669

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Evaluating the ADuC7026 MicroConverter

FEATURES

- Full featured evaluation system for the ADuC7026
- 2-layer PCB (4" × 5" form factor)
- 9 V power supply regulated to 3.3 V on board
- 4-pin UART header to connect to RS-232 interface cable
- 20-pin standard JTAG connector
- Demonstration circuit
- 32.768 kHz watch crystal to drive the PLL clock
- ADR291 2.5 V external reference chip
- Reset/download/IRQ0 push-buttons
- Power indicator/general-purpose LEDs
- Access to all ADC inputs and DAC output from external header. All device ports are brought out to external header pins.
- Surface-mount and through-hole general-purpose prototype area
- External memory and latch footprint

QUICKSTART DEVELOPMENT SYSTEM KIT CONTENTS

- ADuC7026 evaluation board
- Serial download cable
- International power supply
- CD containing
  - evaluation software
  - ADuC7026 data sheet
  - example code

QUICKSTART PLUS DEVELOPMENT SYSTEM KIT CONTENTS

- ADuC7026 evaluation board
- mIDAS-Link JTAG emulator
- USB cable
- Serial download cable
- International power supply
- CD containing
  - evaluation software
  - ADuC7026 data sheet
  - example code

GENERAL DESCRIPTION

This user guide, which replaces AN-744, refers to revision B2 of the ADuC7026 MicroConverter® evaluation boards. Two models of the development kit are available: EVAL-ADuC7026QSZ is the QuickStart™ Development System; EVAL-ADuC7026QSPZ is the QuickStart Plus Development System. All references in this user guide to the physical orientation of components on the evaluation board are made with respect to a component-side view of the board with the prototype area appearing at the bottom of the board. The evaluation board is laid out to minimize coupling between the analog and digital sections of the board. To this end, the ground plane is split with the analog section on the left side and a digital plane on the right side of the board. The regulated 3.3 V power supply is routed directly to the digital section and is filtered before being routed into the analog section of the board.

EVALUATION BOARD

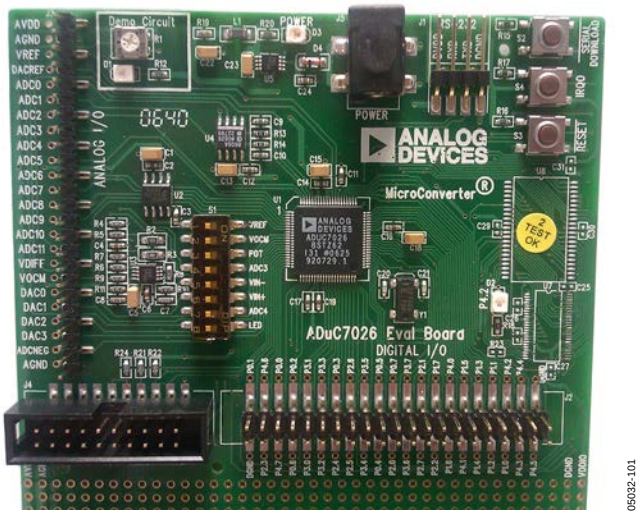

Figure 1. Typical Evaluation Board

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REVISION HISTORY

2/14—Rev. A to Rev. B

Reorganized Layout (from AN-744 to UG-669) ... Universal
Added Figure 1; Renumbered Sequentially and Changes to General Description Section ... 1
Change to Figure 6 ... 12
Changes to Table 5 ... 13

2/07—Rev. 0 to Rev. A

Reorganized Layout ... Universal
Added Table 4 and changes to Figure 2 ... 9
Changes to Figure 4 ... 11
Changes to Table 5 ... 13

2004—Revision 0: Initial Version

GETTING STARTED WITH THE EVALUATION HARDWARE

POWER SUPPLY

Connect the 9 V power supply via the 2.1 mm input power socket (J5). The input connector is configured as a center negative, that is, as GND on the center pin and +9 V on the outer shield.

The 9 V supply is regulated via the Linear Voltage Regulator U5. The 3.3 V regulator output is used to drive the digital side of the board directly. The 3.3 V supply is also filtered and then used to supply the analog side of the board.

When on, the LED (D3) indicates that a valid 3.3 V supply is being driven from the regulator circuit. All active components are decoupled with 0.1 µF at device supply pins to ground.

RS-232 INTERFACE

The ADuC7026 (U1) P1.1 and P1.0 lines are connected to the RS-232 interface cable via Connector J1. The interface cable generates the required level shifting to allow direct connection to a PC serial port. Ensure that the cable supplied is connected to the board correctly, that is, DVDD is connected to DVDD and DGND is connected to DGND.

EMULATION INTERFACE

Nonintrusive emulation and download are possible on the ADuC7026, via JTAG, by connecting a JTAG emulator to the J4 connector.

CRYSTAL CIRCUIT

The board is fitted with a 32.768 kHz crystal, from which the on-chip PLL circuit can generate a 41.78 MHz clock.

EXTERNAL REFERENCE (ADR291)

The external 2.5 V Reference Chip U2 has two functions. It is provided on the evaluation board to demonstrate the external reference option of the ADuC7026, but its main purpose is to generate the V_{OCM} voltage of the differential amplifier if required.

RESET/DOWNLOAD/IRQ0 PUSH-BUTTONS

A reset push-button is provided to allow the user to reset the part manually. When the button is pushed, the reset pin of the ADuC7026 is pulled to DGND. Because the reset pin on the ADuC7026 is Schmidt triggered internally, there is no need to use an external Schmidt trigger on this pin.

When pushed, the IRQ0 push-button switch drives P0.4/IRQ0 high. This can be used to initiate an external interrupt 0.

To enter serial download mode, the user must pull the P0.0/BM pin low while reset is toggled. On the evaluation board, serial download mode can easily be initiated by holding down the serial download push-button (S2) while inserting and releasing the reset button (S3) as shown in Figure 2.

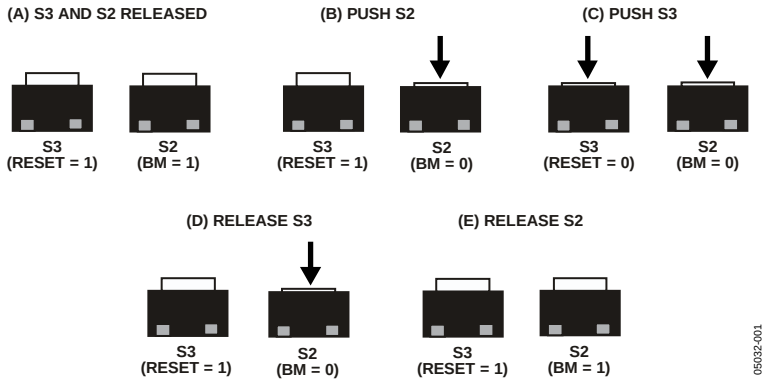

Figure 2. Entering Serial Download Mode on the Evaluation Board

POWER INDICATOR/GENERAL-PURPOSE LEDS

A power LED (D3) is used to indicate that a sufficient supply is available on the board. A general-purpose LED (D2) is directly connected to P4.2 of the ADuC7026. When P4.2 is cleared, the LED is turned on, and when P4.2 is set, the LED is turned off.

ANALOG I/O CONNECTIONS

All analog I/O connections are brought out on Header J3.

ADC0 and ADC1 are buffered using an AD8606 to evaluate single-ended and pseudo differential mode. A potentiometer can be connected to ADC0 (buffered).

ADC3 and ADC4 can be buffered with a single-ended to differential op amp on-board, with the AD8132 used to evaluate the ADC in fully differential mode.

ADC2 and ADC5 to ADC11 are not buffered. Be sure to follow the data sheet recommendations when connecting signals to these inputs.

DAC1 can be used to control the brightness of the LED D1, when connected via the S1 switch.

GENERAL-PURPOSE PROTOTYPE AREA

General-purpose prototype areas are provided at the bottom of the evaluation board for adding external components as required in the user's application. AV_{DD}, AGND, V_{DDIO}, and DGND tracks are provided in the prototype area.

EXTERNAL MEMORY AND LATCH FOOTPRINT

Footprints for a 32 k × 16 static RAM (CY7C1020CV33), a 64 k × 16 flash (AT29LV1024), and a16-bit latch are also on board. See the External Memory Interface section.

DIP SWITCH LINK OPTIONS

S1-1 V_{REF}

Function

Connects the output of the 2.5 V external reference (ADR291) to the V_{REF} pin (Pin 68) of the ADuC7026.

Use

Slide S1-1 to the on position to connect the external reference to the ADuC7026.

Slide S1-1 to the off position to use the internal 2.5 V reference or a different external reference on the V_{REF} pin of Header J3.

S1-2 V_{OCM}

Function

Connects 1.67 V to the V_{OCM} pin of the AD8132. No extra dc voltage is required on the board to use the ADC in differential mode.

Use

Slide S1-2 to the on position to connect V_{OCM} of the differential amplifier to the 1.67 V divided output of the ADR291 reference.

Slide S1-2 to the off position to use a different voltage for V_{OCM} by connecting a dc voltage to the V_{OCM} pin of Header J3. Note that the V_{OCM} value is dependent on the reference value, as shown in Table 1.

Table 1. V_{OCM} Range

V_{REF}	V_{OCM} Minimum	V_{OCM} Maximum
2.5 V	1.25 V	2.05 V
2.048 V	1.024 V	2.276 V
1.25 V	0.75 V	2.55 V

S1-3 POT

Function

Connects the potentiometer output to ADC0. This input is buffered by an AD8606. This is for demonstration purposes.

Use

Slide S1-3 to the on position to connect the potentiometer to the op amp of the ADC0 input channel.

Slide S1-3 to the off position to use the ADC0 input on Header J3.

S1-4 ADC3

Function

Brings out ADC3 (Pin 80) on Header J3.

Use

Slide S1-4 to the on position to connect ADC3 of Header J3 directly to the ADC3 pin (Pin 80) of the ADuC7026.

Slide S1-4 to the off position to disconnect ADC3 of Header J3 from the ADC3 pin (Pin 80) of the ADuC7026.

S1-5 VIN–

Function

Connects the –OUT pin of the single-ended to differential op amp (AD8132) to ADC3. S1-5 and S1-6 must be used together. When VIN– is in the on position, VIN+ must also be in the on position to use the differential op amp on Channel ADC3 and Channel ADC4.

Use

Slide S1-5 to the on position to connect –OUT of the AD8132 to ADC3.

Slide S1-5 to the off position to use ADC3 without the AD8132.

S1-6 VIN+

Function

Connects the +OUT pin of the single-ended to differential op amp (AD8132) to ADC4. When VIN+ is in the on position, VIN– must also be in the on position to use the differential op amp on Channel ADC3 and Channel ADC4.

Use

Slide S1-6 to the on position to connect +OUT of the AD8132 to ADC4.

Slide S1-6 to the off position to use ADC4 without the AD8132.

S1-7 ADC4

Use

Slide S1-7 to the on position to connect ADC4 of Header J3 directly to the ADC4 pin (Pin 1) of the ADuC7026.

Slide S1-7 to the off position to disconnect ADC4 of Header J3 from the ADC4 pin (Pin 1) of the ADuC7026.

S1-8 LED

Function

Connects the DAC1 output to the green LED of the demonstration circuit, D1.

Use

Slide S1-8 to the on position to connect the DAC1 output to D1.

Slide S1-8 to the off position to use the DAC1 output on Header J3.

EXTERNAL CONNECTORS

ANALOG I/O CONNECTOR J3

Connector J3 provides external connections for all ADC inputs, reference inputs and DAC outputs. The pinout of the connector is shown in Table 2.

POWER SUPPLY CONNECTOR J5

Connector J5 allows for the connection between the evaluation board and the 9 V power supply provided in the ADuC7026 development system.

EMULATION CONNECTOR J4

Connector J4 provides a connection of the evaluation board to the PC via a USB cable and mIDAS link provided in the ADuC7026 QuickStart Plus development system only.

SERIAL INTERFACE CONNECTOR J1

Connector J1 provides a simple connection of the evaluation board to the PC via a PC serial port cable provided with the ADuC7026 development system.

DIGITAL I/O CONNECTOR J2

Connector J2 provides external connections for all GPIOs. The pinout of the connector is shown in Table 3.

Table 2. Pin Functions for Analog I/O Connector J3

Pin No.	Pin Description
J3-1	AV_{DD}
J3-2	AGND
J3-3	V_{REF}
J3-4	DAC_{REF}
J3-5	ADC0
J3-6	ADC1
J3-7	ADC2
J3-8	ADC3
J3-9	ADC4
J3-10	ADC5
J3-11	ADC6
J3-12	ADC7
J3-13	ADC8
J3-14	ADC9
J3-15	ADC10
J3-16	ADC11
J3-17	V_{DIFF}
J3-18	V_{OCM}
J3-19	DAC0
J3-20	DAC1
J3-21	DAC2
J3-22	DAC3
J3-23	ADC_{NEG}
J3-24	AGND

Table 3. Pin Functions for Digital I/O Connector J2

Pin No.	Pin Description
J2-1	DGND
J2-2	P4.5 AD13/PLAO[13]
J2-3	P4.4 AD12/PLAO[12]
J2-4	P4.3 AD/11PLAO[11]
J2-5	P4.2 AD10/PLAO[10]
J2-6	P1.0 T1/SIN/SCL0/PLAI[0]
J2-7	P1.1 SOUT/SDA0/PLAI[1]
J2-8	P1.2 RTS/SCL1/PLAI[2]
J2-9	P1.3 CTS/SDA1/PLAI[3]
J2-10	P1.4 IRQ2/RI/CLK/PLAI[4]
J2-11	P1.5 IRQ3/DCD/MISO/PLAI[5]
J2-12	P4.1 AD9/PLAO[9]
J2-13	P4.0 AD8/PLAO[8]
J2-14	P1.6 DSR/MOSI/PLAI[6]
J2-15	P1.7 DTR/CSL/PLAO[0]
J2-16	P2.2 $PWM0_L$/RS/PLAO[7]
J2-17	P2.1 $PWM0_H$/WS/PLAO[6]
J2-18	P2.7 $PWM1_L/\overline{MS3}$
J2-19	P3.7 PWM_{SYNC}/AD7/PLAI[15]
J2-20	P3.6 PWM_{TRIP}/AD6/PLAI[14]
J2-21	P0.7 ECLK/XCLK/SIN/PLAO[4]
J2-22	P2.0 $\overline{CONV_{START}}$/SOUT/PLAO[5]
J2-23	P0.5 $IRQ1/ADC_{BUSY}/\overline{MS0}$/PLAO[2]
J2-24	P0.4 $IRQ0/PWM_{TRIP}/\overline{MS1}$/PLAO[1]
J2-25	P3.5 $PWM2_L$/AD5/PLAI[13]
J2-26	P3.4 $PWM2_H$/AD4/PLAI[12]
J2-27	P2.6 $PWM1_H/\overline{MS2}$
J2-28	P2.5 $PWM0_L/\overline{MS1}$
J2-29	P0.3 $TRST/A16/ADC_{BUSY}$
J2-30	P2.4 $PWM0_H/\overline{MS0}$
J2-31	P3.3 $PWM1_L$/AD3/PLAI[11]
J2-32	P3.2 $PWM1_H$/AD2/PLAI[10]
J2-33	P3.1 $PWM0_L$/AD1/PLAI[9]
J2-34	P3.0 $PWM0_H$/AD0/PLAI[8]
J2-35	P0.2 $PWM2_L/\overline{BHE}$
J2-36	P0.6 T1/MRST/AE/PLAO[3]
J2-37	P0.0 $CMP/\overline{MS2}$/PLAI[7]
J2-38	P4.7 AD15/PLAO[15]
J2-39	P4.6 AD14/PLAO[14]
J2-40	P2.3 AE
J2-41	P0.1 $PWM2_H/\overline{BLE}$
J2-42	DGND

EXTERNAL MEMORY INTERFACE

A footprint for a 32 k × 16 SRAM, a 64 k × 16 flash, and a 16-bit D-latch are provided on board because address and data are multiplexed on the external bus.

The memory footprints are for a CY7C1020CV33 and AT29LV1024. The latch footprint is for a 74LVT16373AGG.

Note that you can use different versions of the CY7C1020CV33 memory, with different access times. Wait states can be added in the XMxPAR register to allow for interfacing to slower memory, if required.

CONNECTIONS

Table 4.

Connection	Description
Controls	$\overline{RS}$, $\overline{WS}$, and AE are the minimum control signals of any memory interface. $\overline{MS0}$ and $\overline{MS1}$, memory select signals, are connected to the $\overline{CE}$ of the SRAM and the flash, respectively, to enable the memory when necessary. $\overline{BHE}$ and $\overline{BLE}$ allows the high or low byte of the 16-bit SRAM to be selected.
Data	16 bits of address data, (AD[15:0]), are directly connected from the ADuC7026 to the memory circuitry.
Addresses	16 bits of address IO[16:1] are connected from the ADuC7026 to AD[15:0] of the memory devices. AD[0] addresses a byte. To address the 32 k of the SRAM only, 14-bit addresses are required. 15-bit addresses are required for the 64 k flash.

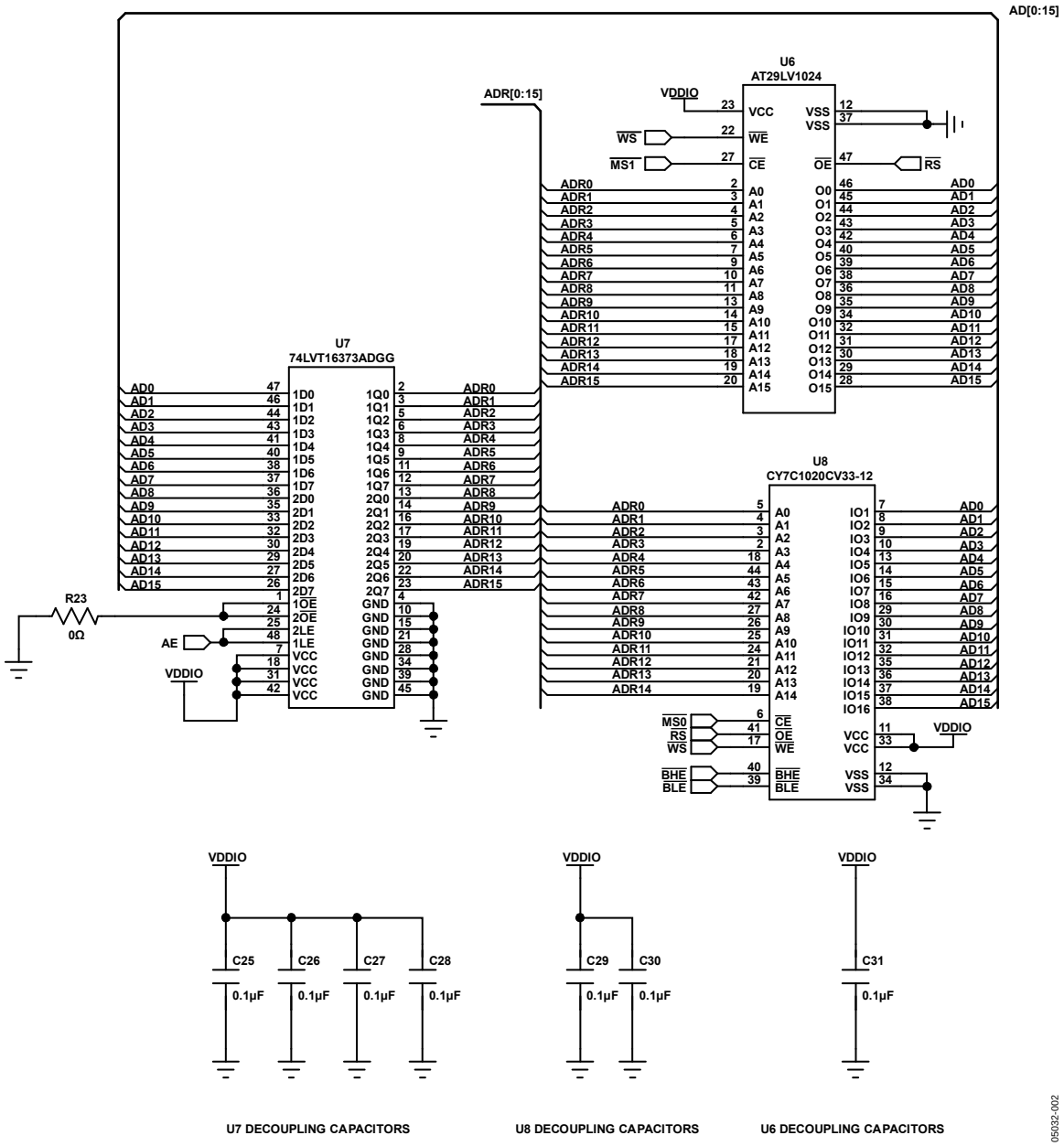

Figure 3. External Memory Connections

POTENTIOMETER DEMONSTRATION CIRCUIT

By using the sample code in pot.c located in the code example folder on the accompanying CD, the variation in the potentiometer resistance can be seen on the output LED.

Note that the internal and external reference are 2.5 V, which gives an ADC input range of 0 V to 2.5 V in single-ended mode. The potentiometer can give a voltage between 0 V and AV_{DD} = 3.3 V.

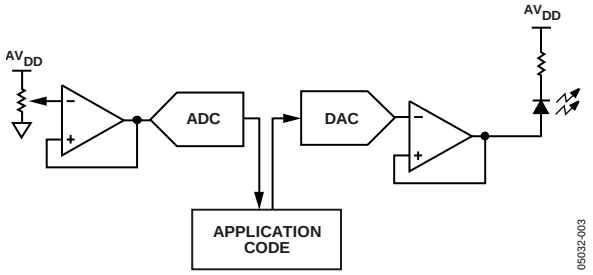

Figure 4. Circuit Diagram of the RTD Circuit

SCHEMATIC AND ARTWORK

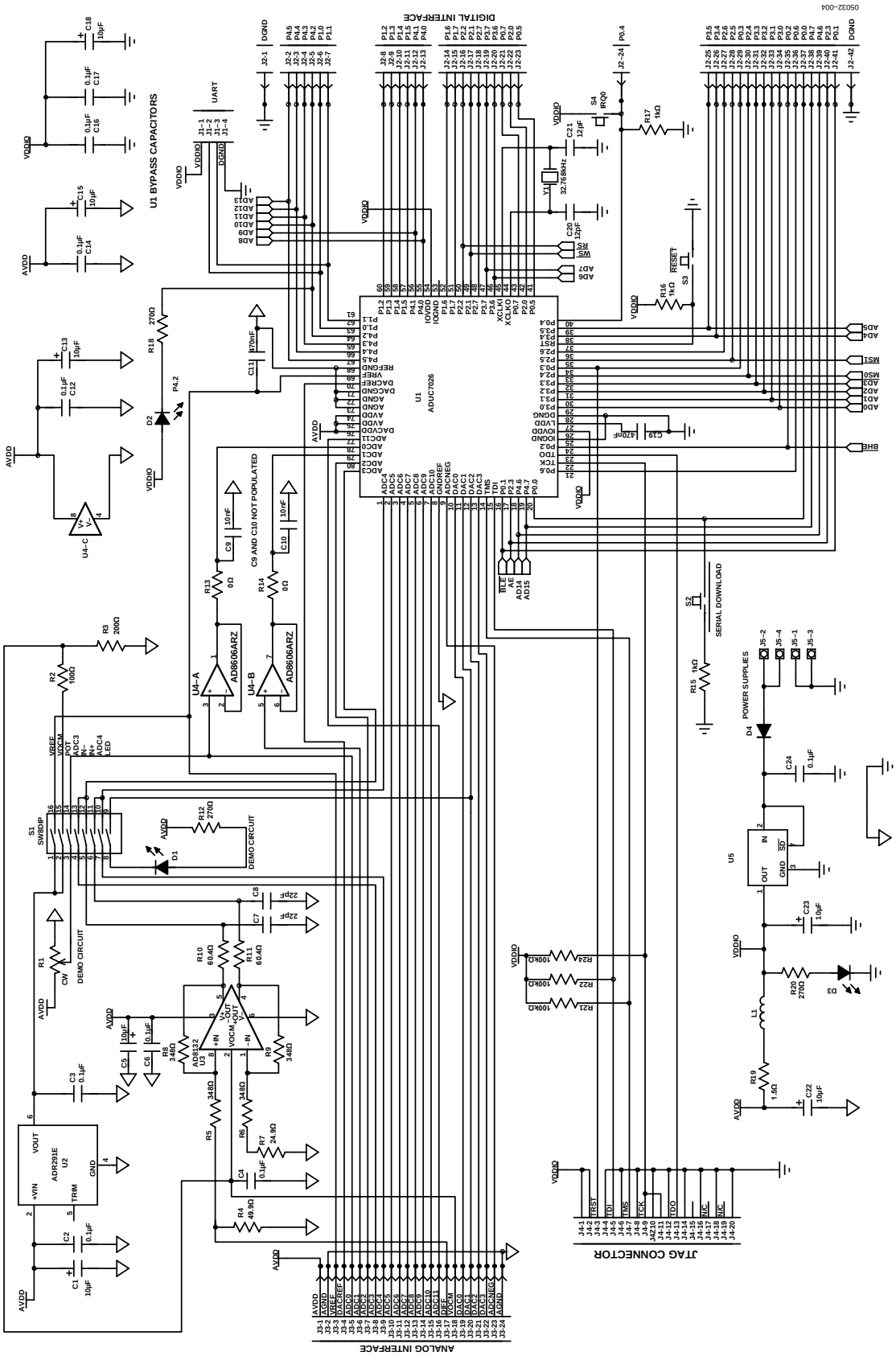

Figure 5. Evaluation Board Schematic

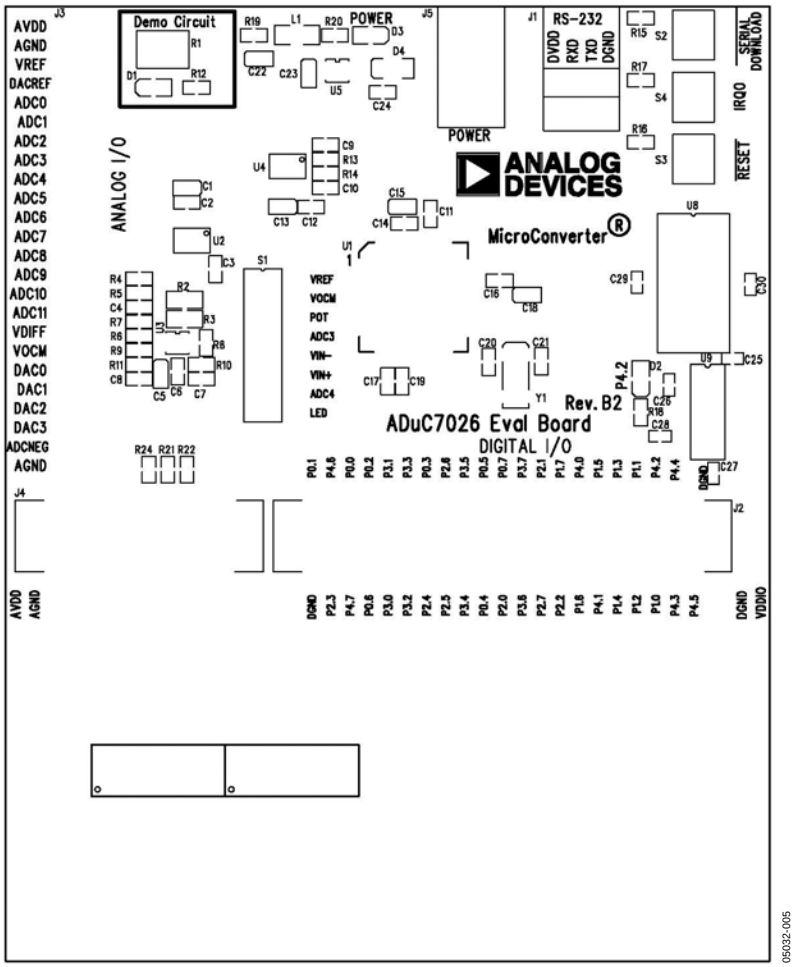

Figure 6. Evaluation Board Silkscreen

BILL OF MATERIALS

Table 5.

Component	Qty	Part	Description	Order No.	Mfg.
ADuC7026 Evaluation Board, Revision B2	1	PCB-1	2-sided, surface-mount PCB		Analog Devices
PCB Standoff	4	Standoff	Stick-on mounting feet	148-922	Farnell
U1	1	ADuC7026	MicroConverter (80-lead LQFP)	ADuC7026CP	Analog Devices
U2	1	ADR291	Band gap reference	ADR291ER	Analog Devices
U3	1	AD8132	Differential op amp	AD8132ARM	Analog Devices
U4	1	AD8606	Dual op amp, (8-pin SOIC)	AD8606AR	Analog Devices
U5	1	ADP3333	Fixed 3.3 V linear voltage regulator	ADP3333ARM3.3	Analog Devices
U6	0	AT29LV1024	64 k × 16 flash	AT29LV1024	Not populated
U7	0	74LVT16373ADGG	16-bit D-latch	74LVT16373ADGG	Not populated
U8	0	CY7C1020CV33-12	32 k × 16 static RAM	CY7C1020CV33-12	Not populated
Y1	1	32.768 kHz	Watch crystal	971-3220	Farnell
S1	1	SW\8DIP	8-way DIP switch	GH7242-ND	DigiKey
S2, S3, S4	3	Push-button switch	PCB-mounted push-button switch	177-807	Farnell
D1, D2, D3	3	LED	1.8 mm miniature LED	359-9954	Farnell
D4	1	PRLL4002	Diode	BAV103TPMSCT-ND	DigiKey
C1, C5, C13, C15, C18, C22, C23	7	10 µF	Surface-mount tantalum capacitor, Taj-B case	197-130	Farnell
C2 to C4, C6, C12, C14, C16, C17, C24	10	0.1 µF	Surface-mount ceramic capacitor, 0603 case	317-287	Farnell
C7, C8	2	22 pF	Surface-mount ceramic capacitor, 0603 case	722-005	Farnell
C9, C10	2	10 nF	Surface-mount ceramic capacitor, 0603 case	301-9561	Farnell
C11, C19	2	470 nF	Surface-mount ceramic capacitor, 0603 case	318-8851	Farnell
C20, C21	2	12 pF	Surface-mount ceramic capacitor, 0603 case	721-979	Farnell
R1	1	10 kΩ potentiometer	0.25W, 4 series, (4 mm × 4 mm square)	TS53YJ 10K 20% TR (lead free)	Vishay
R2	1	100 Ω	Surface-mount resistor, 0603 case	933-2375	Farnell
R3	1	200 Ω	Surface-mount resistor, 0603 case	933-2758	Farnell
R4	1	49.9 Ω	Surface-mount resistor, 0805 case	311-49.9HRCT-ND	DigiKey
R5, R6, R8, R9	4	348 Ω	Surface-mount resistor, 0603 case	311-348HRCT-ND	DigiKey
R7	1	24.9 Ω	Surface-mount resistor, 0805 case	311-24.9HRCT-ND	DigiKey
R10, R11	2	60.4 Ω	Surface-mount resistor, 0805 case	311-60.4HRCT-ND	DigiKey
R12, R18, R20	3	270 Ω	Surface-mount resistor, 0603 case	933-0917	Farnell
R13, R14, R23	3	0 Ω	Surface-mount resistor, 0603 case	933-1662	Farnell
R15, R16, R17	3	1 kΩ	Surface-mount resistor, 0603 case	933-0380	Farnell
R19	1	1.5 Ω	Surface-mount resistor, 0603 case	9331832	Farnell
R21, R22, R24	3	100 kΩ	Surface-mount resistor, 0603 case	933-0402	Farnell
L1	1	Ferrite bead	Surface-mount inductor, 1206 case	952-6862	Farnell
J1	1	4-pin header	4-pin, 90° single-row header	TSM-104-02-T-SH	Samtec
J2	1	42-pin header	42-pin, straight single-row header	TSM-121-01-T-DV	Samtec
J3	1	42-pin header	24-pin, straight single-row header	TSM-124-01-T-SV	Samtec
J4	1	20-pin header	20-pin, connector	HTST-110-01-L-DV	Samtec
J5	1	Power socket	PCB mounted socket (2 mm pin diameter)	KLD-SMT2-0202-A	Kycon

NOTES

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ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG05032-0-2/14(B)