



Integrated Precision Battery Sensor for Automotive System

Silicon Anomaly

ADuC7032-8L

This anomaly list describes the known bugs, anomalies, and workarounds for the ADuC7032-8L/ADuC7032-88 integrated precision battery sensor. The anomalies listed apply to all ADuC7032-8L/ADuC7032-88 packaged material branded as follows:

First Line ADuC7032
Second Line BSTZ-8L BSTZ-88

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ADuC7032-8L FUNCTIONALITY ISSUES

| Silicon Revision Identifier | Kernel Revision Identifier | Chip Marking | Silicon Status | Anomaly Sheet | No. of Reported Anomalies |
|-----------------------------|----------------------------|--------------------------------|----------------|---------------|---------------------------|
| 8L/88 | A60 | ADuC7032 BSTZ-8L or BSTZ-88 | Release | Rev. B | 4 |

ADuC7032-8L PERFORMANCE ISSUES

| Silicon Revision Identifier | Kernel Revision Identifier | Chip Marking | Silicon Status | Anomaly Sheet | No. of Reported Anomalies |
|-----------------------------|----------------------------|--------------------------------|----------------|---------------|---------------------------|
| 8L/88 | A60 | ADuC7032 BSTZ-8L or BSTZ-88 | Release | Rev. B | 2 |

Rev. B

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
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ANOMALIES**ADuC7032-8L/-88 Functionality Issues****1. LIN Communication with VDD > 31 V [er001]:**

| | |
|------------------------|--|
| Background: | The ADuC7032-8L/ADuC7032-88 is specified for operation up to 40 V. |
| Issue: | If the LIN communication occurs with VDD > 31 V, the ADuC7032-8L/ADuC7032-88 resets. |
| Workaround: | Pending. |
| Related Issues: | None. |

2. LIN Short-Circuit Recognition [er002]:

| | |
|------------------------|--|
| Background: | The ADuC7032-8L/ADuC7032-88 features LIN short-circuit protection. In the event of a short circuit on the LIN bus, an interrupt is generated. HVCFG1[2] allows users to enable/disable this interrupt. It is enabled by default. |
| Issue: | If the LIN is shorted to VDD with a resistance lower than 120 Ω , LIN can oscillate over temperature and supply and a short may not be detected. |
| Workaround: | Pending. |
| Related Issues: | None. |

3. Power-On Reset [er003]:

| | |
|--------------------|---|
| Background: | The ADuC7032-8L/ADuC7032-88 integrates a power-on reset (POR) circuit holding the ASIC in reset for 20 ms typically after VDD reaches 3 V typically. |
| Issue: | Under particular conditions, the POR does not release the reset signal, that is, the ASIC remains in reset until a power cycle occurs. This POR issue only occurs under three specific and coincident power-on conditions: <ul style="list-style-type: none"> • Fast ramp on VDD, nominally faster than 100 μs from V_{init} to 12 V • Initial value of VDD (V_{init}) \sim1.2 V • Voltage on REG_DVDD at time the VDD ramp is reapplied \sim175 mV |
| Workaround: | A fast VDD ramp (that is, ramping from \sim 1.2 V to 12 V in $<$ 100 μ s) is required as one of the conditions to initiate the reported POR issue. Analog Devices recommends careful selection of external power supply decoupling components to ensure that the VDD supply ramp rate can always be guaranteed to be $>$ 100 μ s under all VBAT power-on conditions. Specifically, in modules that already incorporate a series resistor and decoupling capacitor to ground on the VDD line between the reverse protection diode and the VDD pin (see Figure 1), choose the series resistor/decoupling capacitor combination to give an RC time constant of at least 100 μ s, such as 10 Ω and 10 μ F. |

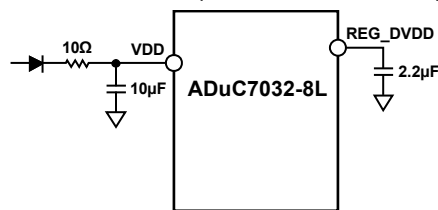


Figure 1.

07055-002

Related Issues: None.

4. ADC Overrange [er004]:

| | |
|------------------------|--|
| Background: | The ADuC7032-8L/ADuC7032-88 integrates a number of flags or status bits (ADCSTA[14:12]) to monitor overrange and underrange conditions in the ADC interface. These bits, automatically set by the hardware, are set to 1 to indicate an underrange or overrange has occurred in the ADC conversion. When this occurs, the data in the data register (ADCxDAT) is invalid. The conversion result in the data register (ADCxDAT) is clamped to negative full scale (underrange) or positive full scale (overrange). |
| Issue: | Under certain limited operating conditions a large negative overrange does not produce the expected clamp to negative full scale. Two situations may occur: <ul style="list-style-type: none">• Issue 1: A clamp to positive full scale can occur with the error bits (ADCSTA[14:12]) set correctly.• Issue 2: The error bits are not set correctly, and the ADC data register is not clamped to positive full scale or negative full scale. This occurs when the ADCFLT register has the following settings: ADCFLT[15] = 1 and ADCFLT[6:0] = 0x7E or 0x7F. |
| Workaround: | Workarounds for these two issues, when using the I-ADC, are as follows: <ul style="list-style-type: none">• Issue 1: The error bits (ADCSTA[14:12]) can be monitored to identify an overrange or underrange condition in the ADC conversion.• Issue 2: It is recommended not to use these two ADC filter configurations (ADCFLT[6:0] = 0x7E or 0x7F, when ADCFLT[15] = 1). If it is necessary to use these configurations, a workaround for the I-ADC is available by using the overrange (ADCSTA[3]) bit in the ADCSTA register. Two configurations are available: <ul style="list-style-type: none">• This can be configured to produce an interrupt whenever the I-ADC input becomes grossly (133% of full scale) in the positive or negative direction. Therefore, this interrupt, or status bit, can be monitored to indicate that the input has overranged, allowing the PGA gain to be changed without having to wait until the full ADC conversion is complete.• If an interrupt is not required, this bit can be used as an additional validation of the data register. The I-ADC data register (ADC0DAT) is valid if the ADCSTA[0] is 1, and the ADCSTA[3] is 0. |
| Related Issues: | None. |

ANOMALIES**ADuC7032-8L Performance Issues****1. ESD [pr001]:**

| | |
|------------------------|---|
| Background: | The ADuC7032-8L/ADuC7032-88 is intended to be classified for HBM ESD rating of 2 kV and FICDM ESD rating of 500 V. |
| Issue: | For silicon branded 8L and 88, HBM ESD is specified to 800 V and FICDM ESD is specified to 400 V and 750 V for the corner pins. |
| Workaround: | Pending. |
| Related Issues: | None. |

2. WU Pin Latch-Up [pr002]:

| | |
|--------------------|--|
| Background: | The latch-up condition on the WU pin should follow the AECQ100 specification and should be able to sink up to -100 mA at 125°C . |
| Issue: | The WU pin fails the AECQ100 specification. |
| Workaround: | It is recommended to use a protection diode such as BAS52, as shown in Figure 2, to avoid destructive damage to the part. |

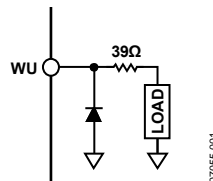


Figure 2. Protection Diode on WU Pin

Related Issues: None.**SECTION 1. ADuC7032-8L/ADuC7032-88 FUNCTIONALITY ISSUES**

| Reference Number | Description | Status |
|------------------|-----------------------------------|--------|
| er001 | LIN communication with VDD > 31 V | Open |
| er002 | LIN short-circuit recognition | Open |
| er003 | Power-on reset | Open |
| er004 | ADC overrange | Open |

SECTION 2. ADuC7032-8L/ADuC7032-88 PERFORMANCE ISSUES

| Reference Number | Description | Status |
|------------------|-----------------|--------|
| pr001 | ESD | Open |
| pr002 | WU pin latch-up | Open |