Integrated Precision Battery Sensor for Automotive Systems

Silicon Anomaly Sheet

ADuC7039

This anomaly list describes the known bugs, anomalies, and workarounds for the ADuC7039 integrated precision battery sensor. The anomalies listed apply to all ADuC7039 packaged material branded as follows:

First Line ADuC7039
Second Line WBCPZ or BCP6Z

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ADuC7039 FUNCTIONALITY ISSUES

Silicon Revision Identifier	Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
D60 B60	0	ADuC7039 WBCPZ ADuC7039 BCP6Z	Release	Rev. B	4

Rev. B
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ANOMALIES

ADuC7039 Functionality Issues

1. SPI Communication in Slave Mode [er001]:

Background:	The ADuC7039 features an integrated SPI peripheral. The SPICON[2] configures the phase of the SPI clock relative to each data bit. When SPICON[2] = 0, the SPI clock is expected to transition at the end of each bit. When SPICON[2] = ,1 the SPI clock is expected to transition at the start of each bit transfer. This bit needs to be configured in both master and slave mode. In slave mode this bit should be configured to match the master device set up. If the master clock toggles at the start of a bit transfer, then this bit must be set = 1.
Issue:	When the ADuC7039 SPI interface is configured in slave mode and SPICON[2] = 0, the SPI may transmit incorrect data not reflecting data written to the Tx FIFO.
Workaround:	If SPICON[2] = 1, then the SPI transmits data correctly. The SPI master, however, must be configured to transition its clock at the start of bit transfers. If the ADuC7039 is the only device connected to the SPI master, this issue does not arise as long as the SPI clock does not transition when the SPI chip select to the ADuc7039 is de-asserted (that is, when $\overline{SS}$ = 1).
Related Issues:	None.

2. GPIO Interface [er002]:

Background:	The ADuC7039 features six GPIOs configured via the GPCON and GPDAT MMRs. These two MMRs have read/write access. GPCON controls the mode of operation of the pin. GPCON = 0 configures all pins as GPIOs. GPDAT configures the direction and level of the GPIOs: The direction of each GPIO is configured by writing Bit 24 to Bit 29. The output level of each GPIO is controlled by Bit 16 to Bit 21. The input level of each GPIO is reflected in Bit 0 to Bit 5.
Issue 1:	When writing to the GPDAT MMR, the direction bits are Bit 29 to Bit 24, but when reading back from the GPDAT MMR, the direction bits are Bit 27 to Bit 22.
Workaround 1:	User code should read the direction bits in GPDAT Bit 27 to Bit 22.
Issue 2:	After configuring the GPIOs as inputs, Bit 0 to Bit 5 do not reflect the correct level on the pins.
Workaround 2:	Add a dummy instruction between configuring the GPIO and reading back GPDAT to ensure correct reading of the GPIO levels.
Related Issues:	None.

3. ADC Overrange [er003]:

Background:	The ADuC7039 integrates a number of flags or status bits (ADCSTA[13:12]) to monitor overrange and underrange in the ADC interface. These bits, set automatically by hardware, are set to 1 to indicate an underrange or overrange has occurred in the ADC conversion. When this occurs, the data in the data register (ADCxDAT) is invalid. The conversion result in the data register (ADCxDAT) is clamped to negative full scale (underrange) or positive full scale(overrange).
Issue :	Under certain limited operating conditions a large negative overrange does not produce the expected clamp to negative full scale. A clamp to positive full scale can occur, with the error bits ADCSTA[13:12] being set correctly.
Workaround:	A workaround for this issue when using the I-ADC is to monitor the the error bits, ADCSTA[13:12], to identify an overrange or underrange condition in the ADC conversion.
Related Issues:	None.

4. Operation of SPI in Slave Mode [er004]:

Background:	When in SPI slave mode, the ADuC7039 expects the number of clock pulses from the master to be divisible by 8 when the slave select pin (Pin 21) is active. The internal bit shift counter does not reset when the chip select pin is de-asserted.
Issue:	If the number of clocks from the master is not divisible by 8 when the chip select is active, this can result in incorrect data being received or transmitted by the ADuC7039 as the bit shift counter will not be at 0 for later transfers. The internal bit shift counter for the transmit or receive buffers can only be reset by hardware, software, or watchdog reset condition.
Workaround:	Always ensure that the number of SPI clocks are divisible by 8 when the ADuC7039 chip select is active.
Related Issues:	None.

SECTION 1. ADuC7039 FUNCTIONALITY ISSUES

Reference Number	Description	Status
er001	SPI communication in slave mode	Open
er002	GPIO interface	Open
er003	ADC overrange	Open
er004	Operation of SPI in slave mode	Open

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