INSTRUCTION SET

Arithmetic Operations

			bytes	OSC periods
ADD	A,source	add source to A	1,2	12
ADD	A,#data		2	12
ADDC	A,source	add with carry	1,2	12
ADDC	A,#data		2	12
SUBB	A,source	subtract from A with borrow	1,2	12
SUBB	A,#data		2	12
INC	A	increment	1	12
INC	source		1,2	12
INC	DPTR *		1	24
DEC	A	decrement	1	12
DEC	source		1,2	12
MUL	AB	multiply A by B	1	48
DIV	AB	divide A by B	1	48
DA	A	decimal adjust	1	12

Legend

Rn	register addressing using R0-R7
direct	8bit internal address (00h-FFh)
@Ri	indirect addressing using R0 or R1
source	any of [Rn, direct, @Ri]
dest	any of [Rn, direct, @Ri]
#data	8bit constant included in instruction
#data16	16bit constant included in instruction
bit	8bit direct address of bit
rel	signed 8bit offset
addr11	11bit address in current 2K page
addr16	16bit address

* INC DPTR increments the 24bit value DPP/DPH/DPL

Data Transfer Operations

			bytes	OSC periods
MOV	A,source	move source to destination	1,2	12
MOV	A,#data		2	12
MOV	dest,A		1,2	12
MOV	dest,source		1,2,3	24
MOV	dest,#data		2,3	12,24
MOV	DPTR,#data16		3	24
MOVC	A,@A+DPTR	move from code memory	1	24
MOVC	A,@A+PC		1	24
MOVX	A,@Ri	move to/from data memory	1	24
MOVX	A,@DPTR		1	24
MOVX	@Ri,A		1	24
MOVX	@DPTR,A		1	24
PUSH	direct	push onto stack	2	24
POP	direct	pop from stack	2	24
XCH	A,source	exchange bytes	1,2	12
XCHD	A,@Ri	exchg low digits	1	12

Program Branching

			bytes	OSC periods
ACALL	addr11	call subroutine	2	24
LCALL	addr16		3	24
RET		return from sub.	1	24
RETI		return from int.	1	24
AJMP	addr11	jump	2	24
LJMP	addr16		3	24
SJMP	rel		2	24
JMP	@A+DPTR		1	24
JZ	rel	jump if A = 0	2	24
JNZ	rel	jump if A not 0	2	24
CJNE	A,direct,rel	compare and jump if not equal	3	24
CJNE	A,#data,rel		3	24
CJNE	Rn,#data,rel		3	24
CJNE	@Ri,#data,rel		3	24
DJNZ	Rn,rel	decrement and jump if not zero	2	24
DJNZ	direct, rel		3	24
NOP		no operation	1	12

Logical Operations

			bytes	OSC periods
ANL	A,source	logical AND	1,2	12
ANL	A,#data		2	12
ANL	direct,A		2	12
ANL	direct,#data		3	24
ORL	A,source	logical OR	1,2	12
ORL	A,#data		2	12
ORL	direct,A		2	12
ORL	direct,#data		3	24
XRL	A,source	logical XOR	1,2	12
XRL	A,#data		2	12
XRL	direct,A		2	12
XRL	direct,#data		3	24
CLR	A	clear A to zero	1	12
CPL	A	complement A	1	12
RL	A	rotate A left	1	12
RLC	A	...through C	1	12
RR	A	rotate A right	1	12
RRC	A	...through C	1	12
SWAP	A	swap nibbles	1	12

Boolean Variable Manipulation

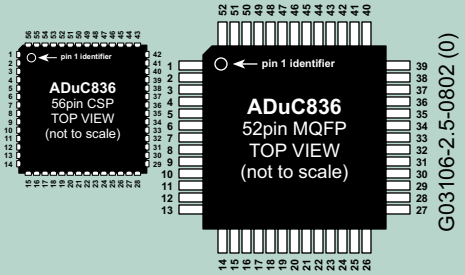
			bytes	OSC periods
CLR	C	clear bit to zero	1	12
CLR	bit		2	12
SETB	C	set bit to one	1	12
SETB	bit		2	12
CPL	C	complement bit	1	12
CPL	bit		2	12
ANL	C,bit	AND bit with C	2	24
ANL	C,/bit	...NOTbit with C	2	24
ORL	C,bit	OR bit with C	2	24
ORL	C,/bit	...NOTbit with C	2	24
MOV	C,bit	move bit to bit	2	12
MOV	bit,C		2	24
JC	rel	jump if C set	2	24
JNC	rel	jmp if C not set	2	24
JB	bit,rel	jump if bit set	3	24
JNB	bit,rel	jmp if bit not set	3	24
JBC	bit, rel	jmp&clear if set	3	24

ASSEMBLER DIRECTIVES

EQU	define symbol	DW	store word values in program memory
DATA	define internal memory symbol	ORG	set segment location counter
IDATA	define indirect addressing symbol	END	end of assembly source file
XDATA	define external memory symbol	CSEG	select program memory space
BIT	define internal bit memory symbol	XSEG	select external data memory space
CODE	define program memory symbol	DSEG	select internal data memory space
DS	reserve bytes of data memory	ISEG	select indirectly addressed internal data memory space
DBIT	reserve bits of bit memory		
DB	store byte values in program memory	BSEG	select bit addressable memory space

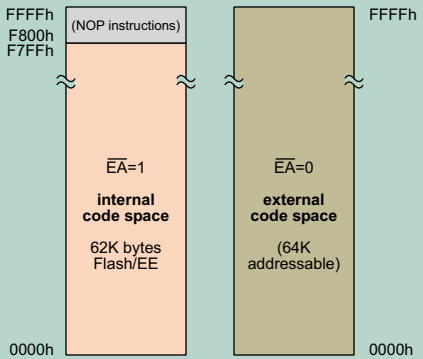
PIN FUNCTIONS

MQFP	CSP		MQFP	CSP		MQFP	CSP	
1	56	P1.0 / T2 / PWM0	14	16	MISO	27	29	SDATA / MOSI	40	43	$\overline{EA}$
2	1	P1.1 / T2EX / PWM1	15	17	RESET	28	30	P2.0 / A8 / A16	41	44	$\overline{PSEN}$
3	2	P1.2 / I_{EXC}1 / DAC	16	18	P3.0 / RxD	29	31	P2.1 / A9 / A17	42	45	ALE
4	3	P1.3 / I_{EXC}2 / AIN5	17	19	P3.1 / TxD	30	32	P2.2 / A10 / A18	43	46	P0.0 / AD0
5	4,5	AV_{DD}	18	20	P3.2 / $\overline{INT0}$	31	33	P2.3 / A11 / A19	44	47	P0.1 / AD1
6	6,7,8	AGND	19	21	P3.3 / $\overline{INT1}$	32	34	XTAL1 (in)	45	48	P0.2 / AD2
7	9	REFIN-	20	22	DV_{DD}	33	35	XTAL2 (out)	46	49	P0.3 / AD3
8	10	REFIN+	21	23	DGND	34	36	DV_{DD}	47	50	DGND
9	11	P1.4 / AIN1	22	24	P3.4 / T0 / PWMclk	35	37,38	DGND	48	51	DV_{DD}
10	12	P1.5 / AIN2	23	25	P3.5 / T1	36	39	P2.4 / A12 / A20	49	52	P0.4 / AD4
11	13	P1.6 / AIN3	24	26	P3.6 / $\overline{WR}$	37	40	P2.5 / A13 / A21	50	53	P0.5 / AD5
12	14	P1.7 / AIN4 / DAC	25	27	P3.7 / $\overline{RD}$	38	41	P2.6 / A14 / A22	51	54	P0.6 / AD6
13	15	$\overline{SS}$	26	28	SCLOCK	39	42	P2.7 / A15 / A23	52	55	P0.7 / AD7



G03106-2.5-0802 (0)

CODE MEMORY SPACE



INTERRUPT VECTOR ADDRESSES

Interrupt Bit	Interrupt Name	Vector Address	Priority within Level
PSMCON.5	Power Supply Monitor Interrupt	43h	1
WDS	WatchDog Timer Interrupt	5Bh	2
IE0	External Interrupt 0	03h	3
RDY0/RDY1	End of ADC Conversion Interrupt	33h	4
TF0	Timer0 Overflow Interrupt	0Bh	5
IE1	External Interrupt 1	13h	6
TF1	Timer1 Overflow Interrupt	1Bh	7
ISPI/I2CI	SPI/I2C Interrupt	3Bh	8
RI/TI	UART Interrupt	23h	9
TF2/EXF2	Timer2 Interrupt	2Bh	10
TIMECON.2	Time Interval Counter Interrupt	53h	11

PRINTED IN U.S.A.

ANALOG DEVICES

ADuC836

MicroConverter® Quick Reference Guide

a "Data Acquisition System on a Chip"

the ADuC836 is:

ADC: 16bit ΣΔ with programmable gain, plus 16bit ΣΔ auxiliary ADC

DAC: 12bit, 15µs, voltage output, rail-to-rail <1LSB DNL

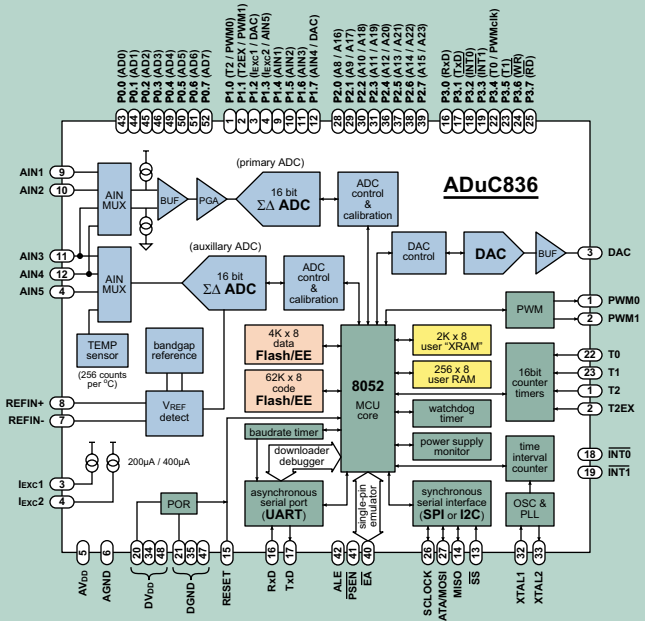
EEPROM: 62K bytes Flash/EE code memory
4K bytes Flash/EE data memory

microcontroller: industry standard 8052
32 I/O lines, programmable PLL clock (98KHz to 12.58MHz from 32KHz crystal)

other on-chip features: calibrated temperature sensor, power supply monitor, watchdog timer, flexible serial interface ports, voltage reference, time interval counter, dual 8/16bit PWM, power-on-reset

FUNCTIONAL BLOCK DIAGRAM

* pin numbers below refer to MQFP package



www.analog.com/microconverter

REV. 0

BIG MEMORY BIG MEMORY BIG MEMORY BIG MEMORY BIG MEMORY BIG MEMORY BIG MEMORY BIG MEMORY BIG MEMORY BIG MEMORY BIG MEMORY

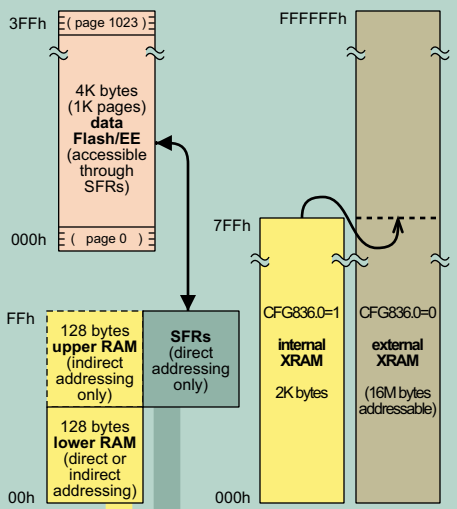
DATA MEMORY: RAM, SFRs, user Flash/EE (all read/write)

LOWER RAM

decimal address	HEX address		MSB address			(bit addresses)			LSB address
127	7Fh	General Purpose Area							
...	...								
48	30h								
47	2Fh	Bit Addressable Area	7Fh	7Eh	7Dh	7Ch	7Bh	7Ah	79h	78h
46	2Eh		77h	76h	75h	74h	73h	72h	71h	70h
45	2Dh		6Fh	6Eh	6Dh	6Ch	6Bh	6Ah	69h	68h
44	2Ch		67h	66h	65h	64h	63h	62h	61h	60h
43	2Bh		5Fh	5Eh	5Dh	5Ch	5Bh	5Ah	59h	58h
42	2Ah		57h	56h	55h	54h	53h	52h	51h	50h
41	29h		4Fh	4Eh	4Dh	4Ch	4Bh	4Ah	49h	48h
40	28h		47h	46h	45h	44h	43h	42h	41h	40h
39	27h		3Fh	3Eh	3Dh	3Ch	3Bh	3Ah	39h	38h
38	26h		37h	36h	35h	34h	33h	32h	31h	30h
37	25h		2Fh	2Eh	2Dh	2Ch	2Bh	2Ah	29h	28h
36	24h		27h	26h	25h	24h	23h	22g	21h	20h
35	23h		1Fh	1Eh	1Dh	1Ch	1Bh	1Ah	19h	18h
34	22h		17h	16h	15h	14h	13h	12h	11g	10h
33	21h		0Fh	0Eh	0Dh	0Ch	0Bh	0Ah	09h	08h
32	20h		07h	06h	05h	04h	03h	02h	01h	00h

31	1Fh	R7	Register Bank 3
30	1Eh	R6	
29	1Dh	R5	
28	1Ch	R4	
27	1Bh	R3	
26	1Ah	R2	Register Bank 2
25	19h	R1	
24	18h	R0	
23	17h	R7	
22	16h	R6	
21	15h	R5	
20	14h	R4	
19	13h	R3	
18	12h	R2	Register Bank 1
17	11h	R1	
16	10h	R0	
15	0Fh	R7	
14	0Eh	R6	
13	0Dh	R5	
12	0Ch	R4	
11	0Bh	R3	
10	0Ah	R2	Register Bank 0
9	09h	R1	
8	08h	R0	
7	07h	R7	
6	06h	R6	
5	05h	R5	
4	04h	R4	
3	03h	R3	
2	02h	R2	
1	01h	R1	
0	00h	R0	

DATA MEMORY SPACE
(read/write area)



lower RAM details

SFR details

SFR MAP & RESET VALUES

(reserved)	SPIDAT 00h	(reserved)	(reserved)	PSMCON DFh	PLLCON D7h	(reserved)	EADRH C6h	EDATA4 00h	SPH B7h	CFG836 00h	DPCON A7h	(reserved)	(reserved)	(reserved)	PCON 87h
(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	EADRL C6h	EDATA3 00h	(reserved)	PWMCON 00h	INTVAL A6h	T3CON 00h	(reserved)	(reserved)	(reserved)
DACCON FDh	(reserved)	GN1H* EDh	OF1H E5h	ADC1H DDh	ICON D5h	TH2 CDh	(reserved)	EDATA2 BDh	(reserved)	HOUR A5h	T3FD 9Dh	TH1 8Dh	(reserved)		
DACH FCh	(reserved)	GN1L* ECh	OF1L E4h	ADC1L DCh	SF D4h	TL2 CCh	(reserved)	EDATA1 BCh	PWM1H B4h	MIN A4h	(not used)	TH0 8Ch	DPP 84h		
DACL FBh	(not used)	GN0H* EBh	OF0H E3h	ADC0H DBh	ADC1CON D3h	RCAP2H CBh	(reserved)	PWM1L B3h	SEC A3h	I2CADD 9Bh	TL1 8Bh	DPH 83h			
(reserved)	(reserved)	GN0M* EAh	OF0M E2h	ADC0M DAh	ADC0CON D2h	RCAP2L CAh	CHIPID C2h	PWM0H B2h	HTHSEC A2h	I2CDAT 9Ah	TL0 8Ah	DPL 82h			
(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	ADCMODE D1h	(reserved)	ECON B9h	PWM0L B1h	TIMECON A1h	SBUF 99h	TMOD 89h	SP 81h			
SPICON F8h	B F0h	I2CCON E8h	ACC E0h	ADCSTAT D8h	PSW D0h	T2CON C8h	WDCON C0h	IP B8h	P3 B0h	IE A8h	P2 A0h	SCON 98h	P1 90h	TCON 88h	P0 80h

SPR0 F9h 0	SPR1 F9h 0	CPHA FAh 1	CPOL F8h 0	SPIM FCh 0	WCOL FEh 0	ISPI FFh 0										
I2CI E8h 0	I2CTX E9h 0	I2CRS EAh 0	I2CM EBh 0	MDI ECh 0	MCO EDh 0	MDE EEh 0	RDY0 DFh 0									
P D0h 0	F1 D1h 0	OV D2h 0	RS0 D3h 0	RS1 D4h 0	F0 D5h 0	AC D6h 0	CY D7h 0									
CAP2 C8h 0	CNT2 C9h 0	TR2 CAh 0	EXEN2 CBh 0	TCLK CCh 0	RCLK CDh 0	EXF2 CEh 0	TF2 CFh 0									
WDWR C0h 0	WDE C1h 0	WDS C2h 0	WDIR C3h 0	PRE0 C4h 1	PRE1 C5h 1	PRE2 C6h 1	PRE3 C7h 1									
PX0 B8h 0	PT0 B9h 0	PX1 BAh 0	PT1 BBh 0	PS BCh 0	PT2 BDh 0	PADC BEh 0	RD B7h 1									
RXD B0h 1	TXD B1h 1	INT0 B2h 1	INT1 B3h 1	T0 B4h 1	T1 B5h 1	WR B6h 1	EADC AEh 0									
EX0 A8h 0	ET0 A9h 0	EX1 AAh 0	ET1 ABh 0	ES ACh 0	ET2 ADh 0	EA AFh 0										
A0h 1	A1h 1	A2h 1	A3h 1	A4h 1	A5h 1	A6h 1	A7h 1									
RI 98h 0	TI 99h 0	RB8 9Ah 0	TB8 9Bh 0	REN 9Ch 0	SM2 9Dh 0	SM1 9Eh 0	SM0 9Fh 0									
T2 90h 1	T2EX 91h 1	IE0 89h 0	IT0 88h 0	IE1 8Bh 0	IT1 8Ah 0	TR0 8Ch 0	TF0 8Dh 0	TR1 8Eh 0	TF1 8Fh 0							
80h 1	81h 1	82h 1	83h 1	84h 1	85h 1	86h 1	87h 1									

MAP KEY

* calibration coefficients are preconfigured at power-up to factory calibrated values

SFR DESCRIPTIONS

ADCSTAT ADC Status Register
RDY0 primary ADC ready flag
RDY1 auxiliary ADC ready flag
CAL calibration flag
NOXREF no external reference flag
ERR0 primary ADC error flag
ERR1 auxiliary ADC error flag

ADCMODE ADC Mode Register
ADMODE.5 primary ADC enable bit
ADMODE.4 auxiliary ADC enable bit
ADMODE.2 mode bits
ADMODE.1 [powerdown, idle, sngl-conv, cont-conv, zero-selfcal, fs-selfcal, zero-syscal, fs-syscal]
ADMODE.0

ADC0CON Primary ADC Control Register
AD0CON.7 (this bit must contain zero)
AD0CON.6 external reference select bit (0=internal ref)
AD0CON.5 channel selection bits:
AD0CON.4 [AIN1-AIN2,AIN3-AIN4,AIN2-AIN2,AIN3-AIN2]
AD0CON.3 unipolar select bit (0=bipolar)
AD0CON.2 range select bits:
AD0CON.1 [±20mV, ±40mV, ±80mV, ±160mV, ±320mV,
AD0CON.0 ±640mV, ±1.28V, ±2.56V]

ADC1CON Auxiliary ADC Control Register
AD1CON.6 external reference select bit (0=internal ref)
AD1CON.5 channel selection bits:
AD1CON.4 [AIN3, AIN4, TEMP, AIN5]
AD1CON.3 unipolar select bit (0 = bipolar)

SF Sync Filter Register: $f_{ADC} = 4{,}096Hz / (3 \cdot SF)$

OF0H,OF0M ADC0 offset coefficient

OF1H,OF1L ADC1 offset coefficient

GN0H,GN0M ADC0 gain coefficient

GN1H,GN1L ADC1 gain coefficient

ADC0H,ADC0M ADC0 data

ADC1H,ADC1L ADC1 data

ICON Current Source Control Register
ICON.6 burnout current enable bit
ICON.5 ADC1 current correction bit (0=correction off)
ICON.4 ADC0 current correction bit (0=correction off)
ICON.3 I2 pin select bit [0=pin4 / 1=pin3]
ICON.2 I1 pin select bit [0=pin3 / 1=pin4]
ICON.1 I2 enable bit (0=disable)
ICON.0 I1 enable bit (0=disable)

DACCON DAC Control register
DACCON.4 DAC pin select bit [0=pin3 / 1=pin12]
DACCON.3 ModeSelect (0=12bit, 1=8bit)
DACCON.2 RangeSelect (0=2.5V, 1=AV_{DD})
DACCON.1 Clear DAC (0=ON, 1=normal operation)
DACCON.0 PowerDown DAC (0=off, 1=on)

DACH,DACL DAC data registers

PLLCON PLL Control Register
PLLCON.7 oscillator powerdown control bit (0=XTAL on)
PLLCON.6 PLL lock indicator flag (0=out of lock)
PLLCON.5 (this bit must contain zero)
PLLCON.4 EA detect status bit (reflects state of EA pin)
PLLCON.3 "fast interrupt" control bit (0=normal)
PLLCON.2 3-bit clock divider value, "CD" (default=3):
PLLCON.1 $f_{CORE} = 12{,}582{,}912Hz / 2^{CD}$
PLLCON.0

TIMECON Time Interval Counter Control Register
TIMECON.6 (this bit must contain 1)
TIMECON.5 interval timebase select bits
TIMECON.4 [128th sec, seconds, minutes, hours]
TIMECON.3 single time interval control bit (0=reload&restart)
TIMECON.2 time interval interrupt bit, "TII"
TIMECON.1 time interval enable bit (0=disable&clear)
TIMECON.0 time clock enable bit (0=disable)

INTVAL TIC Interval Register

HTHSEC TIC Elapsed 128th Second Register

SEC TIC Elapsed Seconds Register

MIN TIC Elapsed Minutes Register

HOUR TIC Elapsed Hours Register

ECON Data Flash/EE comand register
01h READ page
02h PROGRAM page
03h VERIFY page
05h ERASE page
06h ERASE ALL
82h PROGRAM byte
0Fh EXIT ULOAD mode
F0h ENTER ULOAD mode
(all others reserved)

EADRH,EADRL Data Flash/EE address registers

EDATA1,EDATA2,EDATA3,EDATA4 Data Flash/EE data registers

SPICON SPI Control register
ISPI SPI interrupt (set at end of SPI transfer)
WCOL write collision error flag
SPE SPI enable (0=I2C enable, 1=SPI enable)
SPIM master mode select (0=slave)
CPOL clock polarity select (0=SCLK idles low)
CPHA clock phase select (0=leading edge latch)
SPR1 SPI bitrate select bits
SPR0 bitrate = F_{CORE} / [2, 4, 8, 16]

SPIDAT SPI Data register

I2CCON I2C Control register
MDO master mode SDATA output bit
MDE master mode SDATA output enable (0=disable)
MCO master mode SCLK output bit
MDI master mode SDATA input bit
I2CM master mode select bit (0=slave mode)
I2CRS serial port reset
I2CTX transmission direction status (0=RX,1=TX)
I2CI serial interface interrupt

I2CADD I2C Address register

I2CDAT I2C Data register

PWMCON PWM Control register
PWMCON.6 PWM mode bits [0=disabled, 1=single/var.res.,
PWMCON.5 2=twin/8bit, 3=twin/16bit, 4=dual/16bitNRZ,
PWMCON.4 5=dual/8bit, 6=dual/16bitRZ, 7=(reserved)]
PWMCON.3 PWM clock divide bits
PWMCON.2 PWM counter = clock / [1,4,16,64]
PWMCON.1 PWM clock source bits [1=F_{XTAL}/15, 2=F_{XTAL},
PWMCON.0 3=external input, 4=F_{VCO}(12.58MHz)]

PWM0H,PWM0L PWM0 data registers

PWM1H,PWM1L PWM1 data registers

T3CON Timer 3 Control register
T3CON.7 Timer 3 baud rate enable (0=disable)
T3CON.2 binary divide factor (DIV)
T3CON.1 DIV = log[F_{CORE}/(32·baudrate)] / log2
T3CON.0 (rounded down)

T3FD Timer 3 Fractional Divider register
T3FD = $(2 \cdot F_{CORE}) / (baudrate \cdot 2^{DIV}) - 64$

CFG836 ADuC836 Configuration register
CFG836.7 extended stack pointer enable (0=disable)
CFG836.0 internal XRAM enable (0=external XRAM only)
all others (reserved)

CHIPID Chip ID Register (3X hex = ADuC836)

DPCON Data Pointer Control register
DPCON.6 data pointer auto-toggle enable (0=disable)
DPCON.5 shadow data pointer mode control bits
DPCON.4 [1=8052, 2=post-inc, 3=post-dec, 4=LSBtgl]
DPCON.3 main data pointer mode control bits
DPCON.2 [1=8052, 2=post-inc, 3=post-dec, 4=LSBtgl]
DPCON.1 (not implemented to allow INC DPCON toggling)
DPCON.0 data pointer select [0=main, 1=shadow]

WDCON Watchdog Timer control register
PRE3 watchdog timeout selection bits
PRE2 0000-0111 = timeout=[15.6, 31.2, 62.5, 125, 500
PRE1 1000 = immediate reset 1000, 2000] ms
PRE0 all others codes = reserved
WDIR watchdog interrupt response enable
WDS watchdog status flag
WDE watchdog enable
WDWR watchdog write enable

PSMCON Power Supply Monitor control register
PSMCON.7 DV_{DD} compare bit (0=fault)
PSMCON.6 AV_{DD} compare bit (0=fault)
PSMCON.5 PSM interrupt bit
PSMCON.4 DV_{DD} trip point select bits
PSMCON.3 [4.63V, 3.08V, 2.93V, 2.63V]
PSMCON.2 AV_{DD} trip point select bits
PSMCON.1 [4.63V, 3.08V, 2.93V, 2.63V]
PSMCON.0 PSM powerdown control (1=on / 0=off)

SP Stack Pointer

SPH Stack Pointer High byte

IE Interrupt Enable register #1
EA enable interrupts (0=all intrrupts disabled)
EADC enable RDY0/RDY1 (ADC interrupt)
ET2 enable TF2/EXF2 (Timer2 overflow interrupt)
ES enable RI/TI (serial port interrupt)
ET1 enable TF1 (Timer1 overflow interrupt)
EX1 enable IE1 (external interrupt 1)
ET0 enable TF0 (Timer0 overflow interrupt)
EX0 enable IE0 (external interrupt 0)

IEIP2 Interrupt Enable/Priority register #2
IEIP2.6 priority of TII interrupt (timer interval)
IEIP2.5 priority of PSMI interrupt (power supply monitor)
IEIP2.4 priority of ISPI/I2CI interrupt (serial interface)
IEIP2.3 (this bit must contain zero)
IEIP2.2 enable TII interrupt (timer interval)
IEIP2.1 enable PSMI interrupt (power supply monitor)
IEIP2.0 enable ISPI/I2CI interrupt (serial interface)

IP Interrupt Priority register
PADC priority of RDY0/RDY1 (ADC interrupt)
PT2 priority of TF2/EXF2 (Timer2 overflow interrupt)
PS priority of RI/TI (serial port interrupt)
PT1 priority of TF1 (Timer1 overflow interrupt)
PX1 priority of IE1 (external interrupt 1)
PT0 priority of TF0 (Timer0 overflow interrupt)
PX0 priority of IE0 (external interrupt 0)

TMOD Timer Mode register
TMOD.3/.7 gate control bit (0=ignore INTx)
TMOD.2/.6 counter/timer select bit (0=timer)
TMOD.1/.5 timer mode selecton bits
TMOD.0/.4 [13bitT, 16bitT/C, 8bitT/Creload, 2x8bitT]
(upper nibble = Timer1, lower nibble = Timer0)

TCON Timer Control register
TF1 Timer1 overflow flag
TR1 Timer1 run control (0=off, 1=run)
TF0 Timer0 overflow flag
TR0 Timer0 run control (0=off, 1=run)
IE1 external INT1 flag
IT1 IE1 type (0=level trig, 1=edge trig)
IE0 external INT0 flag
IT0 IE0 type (0=level trig, 1=edge trig)

TH0,TL0 Timer0 registers

TH1,TL1 Timer1 registers

T2CON Timer2 Control register
TF2 overflow flag
EXF2 external flag
RCLK receive clock enable (0=Timer1 used for RxD clk)
TCLK transmit clock enable (0=Timer1 used for TxD clk)
EXEN2 external enable (0=ignore T2EX, 1=capt/rld on T2EX)
TR2 run control (0=stop, 1=run)
CNT2 timer/counter select (0=timer, 1=counter)
CAP2 capture/reload select (0=reload, 1=capture)

TH2,TL2 Timer2 register

RCAP2H,RCAP2L Timer2 Reload/Capture

P0 Port0 register (also A0-A7 & D0-D7)

P1 Port1 register
P1.2-1.7 analog/digital pins (1=analog function, 0=digital input)
T2EX timer/counter 2 capture/reload trigger (or digital I/O)
T2 timer/counter 2 external input (or digital I/O)

P2 Port2 register (also A8-A15 & A16-A23)

P3 Port3 register
RD external data memory read strobe
WR external data memory write strobe
T1 timer/counter 1 external input
T0 timer/counter 0 external input
INT1 external interrupt 1
INT0 external interrupt 0
TxD serial port transmit data line
RxD serial port receive data line

SCON Serial communications Control register
SM0 UART mode control bits baud rate:
SM1 00 - 8bit shift register - F_{CORE}/12
01 - 8bit UART - variable
10 - 9bit UART - F_{CORE}/64(x2)
11 - 9bit UART - variable
SM2 in modes 2&3, enables multiprocessor communication
REN receive enable control bit
TB8 in modes 2&3, 9th bit transmitted
RB8 in modes 2&3, 9th bit received
TI transmit interrupt flag
RI receive interrupt flag

SBUF Serial port Buffer register

PCON Power Control register
PCON.7 double baud rate control
PCON.6 enable serial interrupt (ISI) from power-down mode
PCON.5 enable interrupt (INT0) from power-down mode
PCON.4 ALE disable (0=normal, 1=forces ALE high)
PCON.3 general purpose flag
PCON.2 general purpose flag
PCON.1 power-down control bit (0=normal)
PCON.0 idle-mode control (0=normal)

PSW Program Status Word
CY carry flag
AC auxiliary carry flag
F0 general purpose flag 0
RS1 register bank select control bits
RS0 active register bank = [0,1,2,3]
OV overflow flag
F1 general purpose flag 1
P parity of ACC

DPP Data Pointer Page

DPH,DPL (DPTR) Data Pointer

ACC Accumulator

B auxiliary math register

BIG MEMORY BIG MEMORY BIG MEMORY BIG MEMORY BIG MEMORY BIG MEMORY BIG MEMORY BIG MEMORY BIG MEMORY BIG MEMORY BIG MEMORY