ANALOG DEVICES

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ADuCM350 Analog Front End Accuracy in a Noisy Digital Environment

INTRODUCTION

The ADuCM350 is a complete, coin cell powered, high precision, meter-on-chip for portable device applications, such as point-of-care diagnostics and body-worn vital signs monitoring devices.

The ADuCM350 analog front end (AFE) features a 16-bit precision, 160 kSPS ADC, 0.2% precision voltage reference, 12-bit no missing codes DAC, and a reconfigurable ultralow leakage switch matrix. The ADuCM350 also includes a Cortex™-M3 based processor, memory, and all I/O connectivity

to support portable meters with display, USB communication and active sensors. The ADuCM350 is available in a 120-pin, 8 mm × 8 mm CSP_BGA, and operates from −40 °C to +85°C.

The ADuCM350 is specifically designed for high precision analysis of electrochemical reactions.

This application note documents the robustness of the analog front end of the ADuCM350 in the presence of four separate intensive digital noise environments.

FUNCTIONAL BLOCK DIAGRAM

Figure 1.

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REVISION HISTORY

3/14—Revision 0: Initial Version

SEQUENCER/AFE CONTROLLER

The ADuCM350 utilizes an autonomous sequencer to control the analog front end of the device. This allows the AFE to perform cycle accurate operations in an asynchronous manner to the Cortex-M3 processor. The sequencer handles the precision and timing critical operations without being subjected to system load.

The Cortex-M3 processor runs a sequence using the **RunSequence** command. There are two independent DMA

channels for transferring data to and from the sequencer. There are two fail safe operations for operational integrity; a sequence counter which tallies the number of commands executed by the sequencer and a CRC-8 applied on all commands executed. Once the sequence begins, it operates independently of the core and can only be aborted using specific commands.

This functionality allows the ADuCM350 to perform high precision robust measurements in a digitally noisy environment

Figure 2. ADuCM350 Example of Amperometric Type Sequence in Software Development Kit
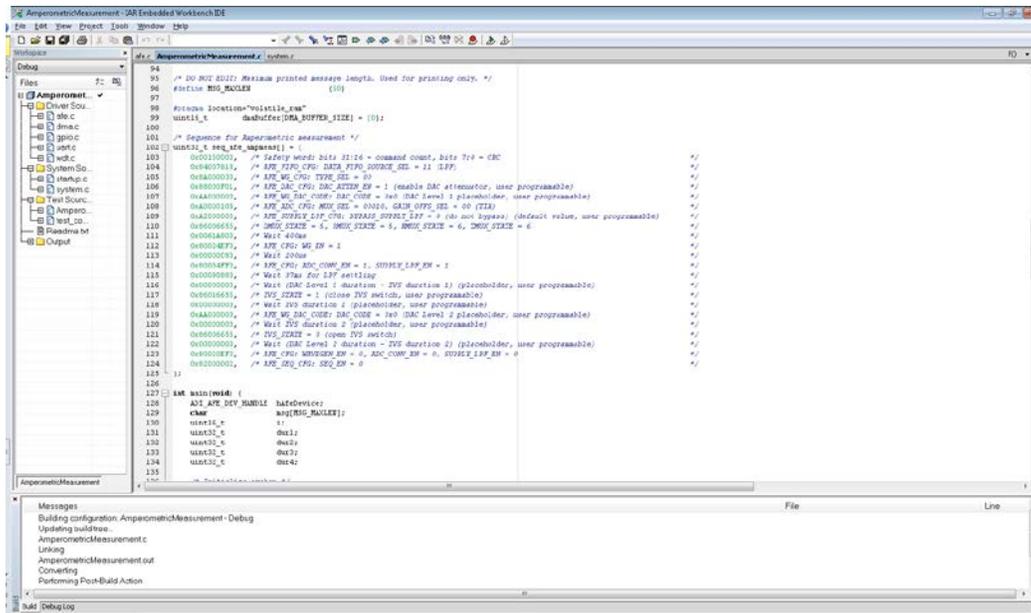
DIGITAL FILTERING

This block implements a low-pass supply rejection filter for output data rates of 900 SPS. The requirement is to reject 50 Hz/60 Hz tones in the dc amperometric phase.

The filter block consists of two cascaded sinc2 filters. The first filter (sinc2hf) decimates the input data (ADC data sampled at 160 kHz) down to ~900 Hz. The second filter (sinc2lf) adds notches at 50 Hz and 60 Hz for supply rejection. Typically, the filtered data (sinc2lf) is supplied to the Cortex-M3, but the option exists to read back the unfiltered data (sinc2hf output).

The filter settling time is 1/50 + 1/60 = 36.667 ms.

The block diagram is shown in Figure 3.

The sinc2hf filter decimates the 160 kSPS input data by 178 for a target output data rate of 900 Hz. The reason behind choosing 900 Hz was to allow the optimal placement of the 50 Hz and 60 Hz notches.

The selectivity achieved with this configuration makes it very robust for high precision measurement in a digitally noisy environment. See Figure 4 for plot of signal-to-noise ratio of TIA measurement channel.
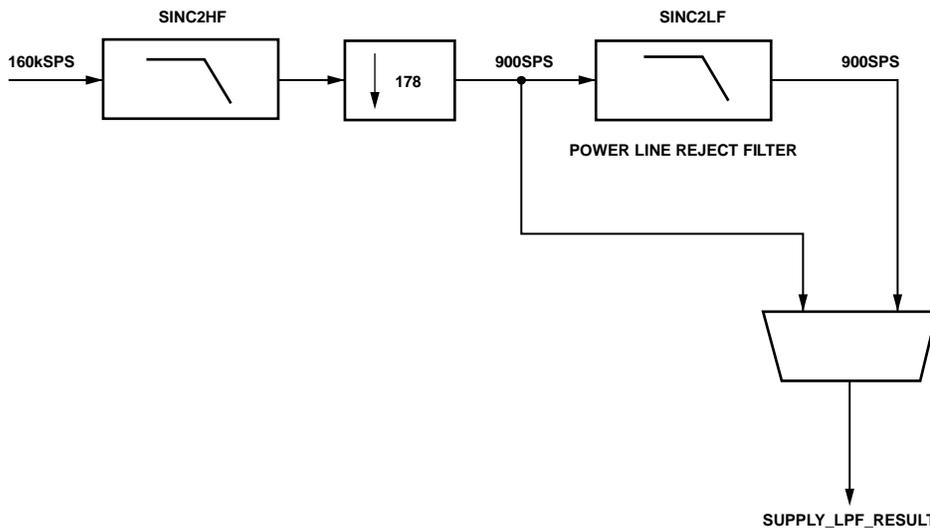
Figure 3. ADuCM350 Supply Rejection Filter Block Diagram
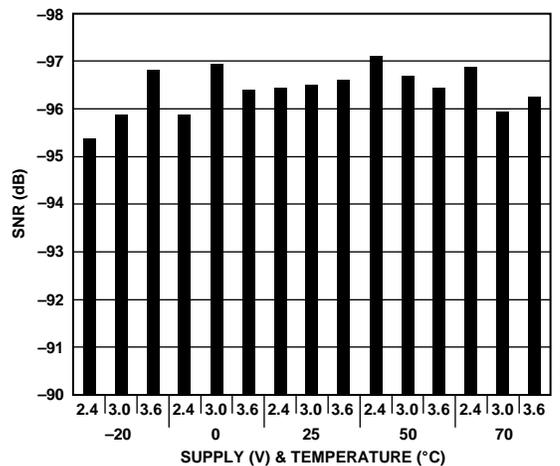
Figure 4. TIA Channel Signal-to-Noise Ratio

DISCRETE FOURIER TRANSFORM BLOCK

This block performs a 2048-point single frequency discrete Fourier transform (DFT). It takes the 16-bit ADC output as input and outputs the real and imaginary parts of the complex result.

The DFT engine calculates the signal power at a single frequency bin, which is the bin corresponding to the excitation frequency. As such, there is a tight coupling between the sinusoid waveform generator and the DFT engine. The frequency control word (AFE_WG_FCW) is used by the DFT engine to determine the required frequency bin.

The DFT engine outputs the results as a complex number. The magnitude and phase of the impedance at the excitation frequency are calculated by the Cortex-M3 using the following formulas:

$$Magnitude = \sqrt{R^2 + I^2}$$

$$Phase = atan\left(\frac{I}{R}\right)$$

The DFT function is optimized to be very immune to noise because it is highly selective with a very narrow pass-band filter performance. See Figure 6 for simulations performed on DFT performance
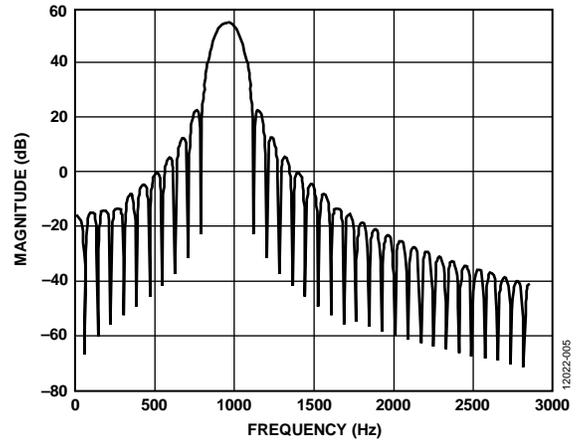
Figure 5. Modeled ADuCM350 DFT Frequency Response
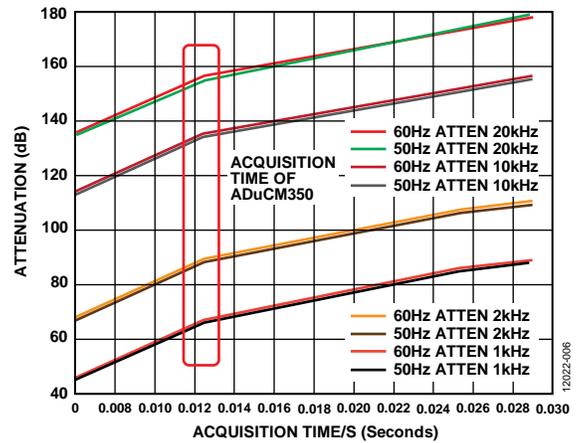
Figure 6. Mathematical Modeling of DFT Narrow Band-Pass Capability

DIGITAL STRESS TESTS

The measurements described in this section are targeted to generate digital noise that may interfere with the precision analog measurements. There are many digital blocks on the ADuCM350 that cannot generate a lot of digital noise, such as UART, RTC, and timers. These tests are intended to be practical and application specific.

Due to the high selectivity of the DFT, the decimated ADC with Sinc2LPF enabled was used for these measurements

For each test, the first set of measurements are done with only the ADC converting and no stress enabled. The second set of measurements are done with the ADC converting using the sequencer while the digital noise source is being excited in parallel.

Measurements were taken at ambient temperature.

CRC STRESS TEST

Purpose

This is a data transfer test where the DMA performs a 512 32-bit transfer from SRAM0 (source) to CRC (destination) with no wait states. This is repeated using SRAM1. This test is looped while precision analog measurements are being made using the AFE sequencer.

Digital Blocks Exercised

- CRC
- DMA
- Bus matrix
- SRAM0
- SRAM1

Results

Results show that the CRC stress noise has negligible impact on the analog precision measurements.
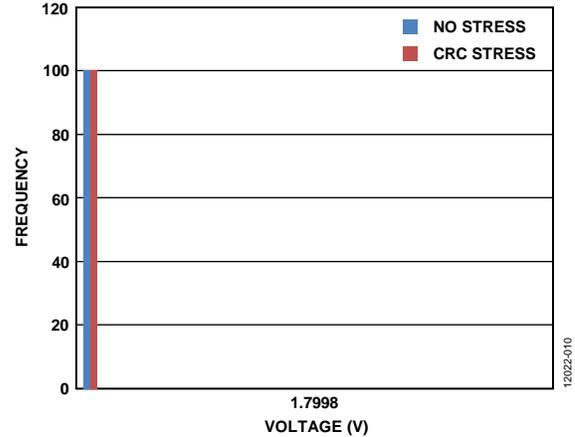
Figure 7. REF_EXCITE Measurement Internally Through ADC Mux
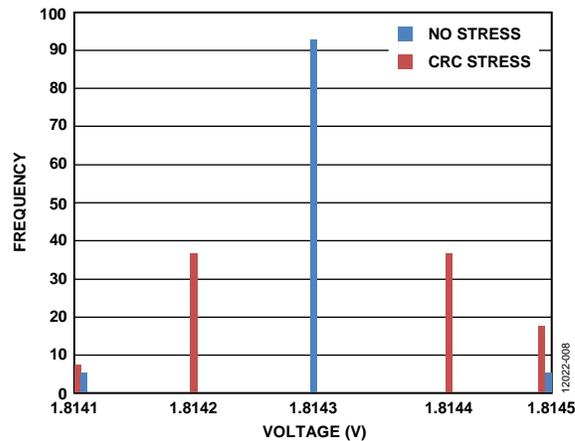
Figure 8. ½ DVDD Measurement Internally Through ADC Mux
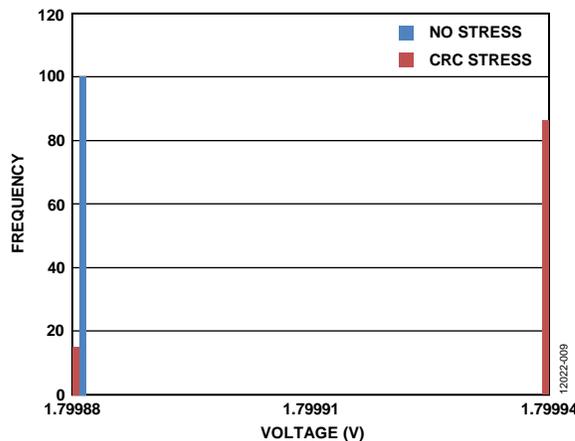
Figure 9. REF_EXCITE Measured Through Pin An_B

PARALLEL DISPLAY INTERFACE STRESS TEST

Purpose

The parallel display interface (PDI), similar to the CRC, can transfer large amounts of 32-bit data internally. In addition, the PDI also switches a wide parallel port (16 bits) with the potential for noise during basic display operations. The PDI represents the most number of pins a single interface can switch simultaneously.

Data is prepared in the general-purpose (GP) flash and this is used as a DMA source. Data is transferred, through the DMA, from GP flash (source) to PDI (destination) using the DMA. This test is run at the maximum data rate possible. This transfer is looped while a precision AFE measurement is made.

Digital Blocks Exercised

- PDI
- DMA
- Bus matrix
- General-purpose flash

Results

Results show that the PDI stress noise has negligible impact on the analog precision measurements.
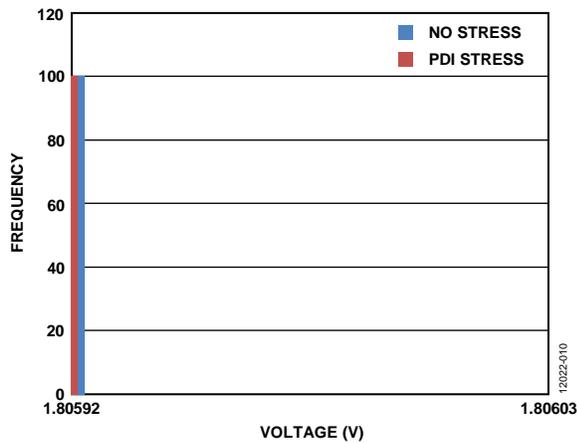
Figure 10. REF_EXCITE Measurement Internally Through ADC Mux
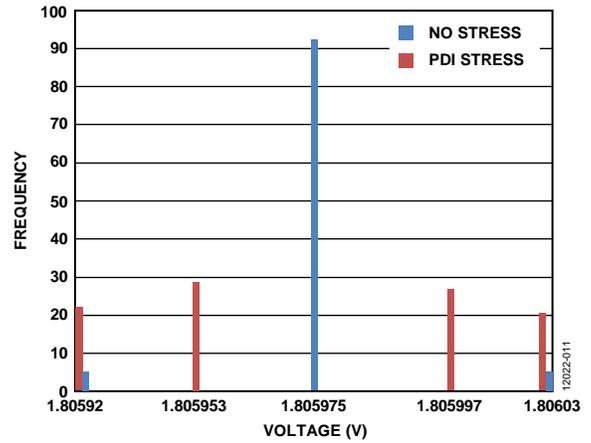
Figure 11. ½ DVDD Measurements Internally Through ADC Mux
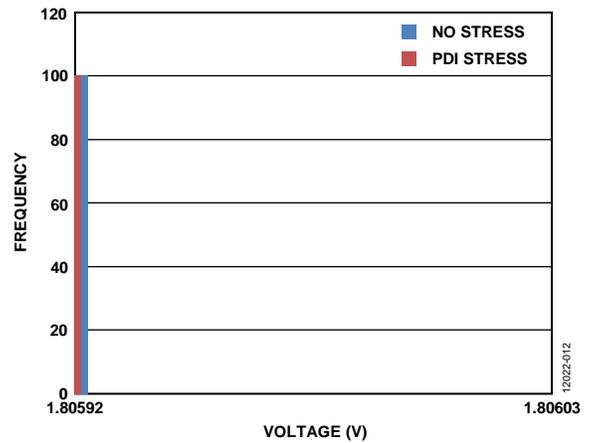
Figure 12. REF_EXCITE Measured Through Pin An_B

SERIAL PERIPHERAL INTERFACE STRESS TEST

The high speed SPI bus (SPIH) is suitable for flash storage of video or audio data. It can be accessed at 8 MHz and run in bursts.

In this stress test, the SPIH is set up to transfer 512 byte blocks of data to and from SRAM 1 at 8 MHz SCLK speed. The DMA is used for data transfers to and from the SPIH.

Digital Blocks Exercised

* SPIH

* DMA

* Bus matrix

Results

Results show that the SPI stress noise has negligible impact on the analog precision measurements.

Figure 14. ½ DVDD Measurement Internally Through ADC Mux
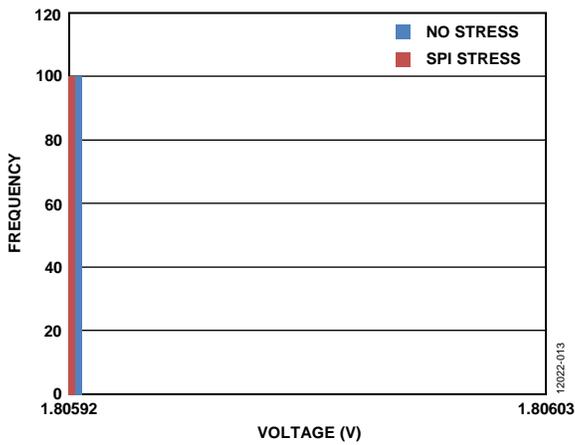
Figure 13. REF_EXCITE Measurement Internally Through ADC Mux
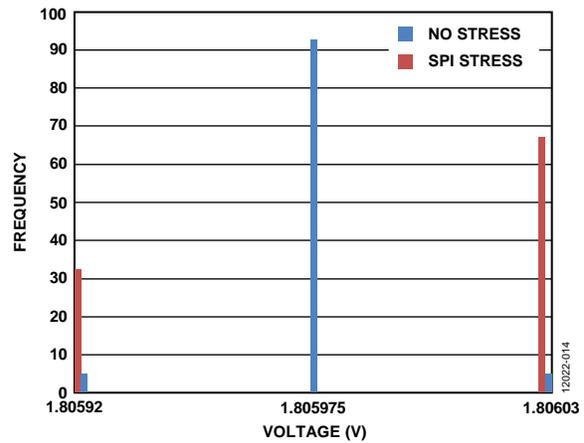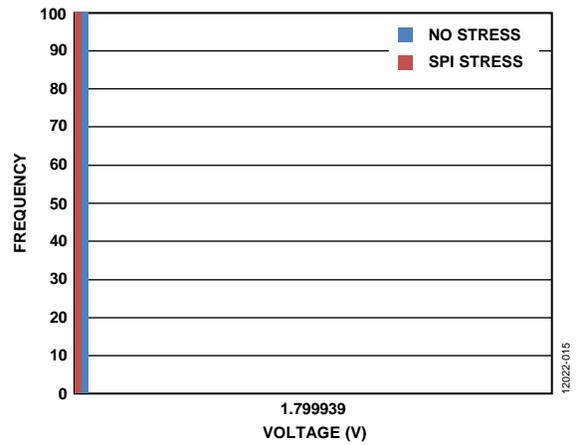
Figure 15. REF_EXCITE Measured Through Pin An_B

I²S STRESS TEST

I²S represents a continuous 8k bits/second data transfer rate through the system at low performance audio rates. This represents 8 kHz sample rate, mono sound, with 8-bits/sample. It is a combination of a steady stream of data using the DMA, SRAM, I²S, and I/O pins.

Digital Blocks Exercised

- I²S
- DMA
- SRAM1

Results

Results show that the I²S stress noise has negligible impact on the analog precision measurements.
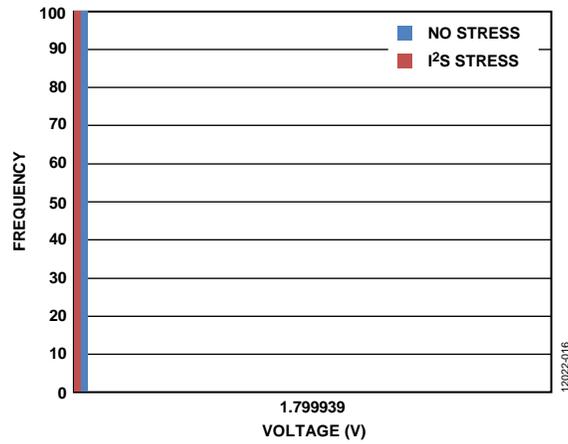
Figure 16. REF_EXCITE Measurement Internally Through ADC Mux
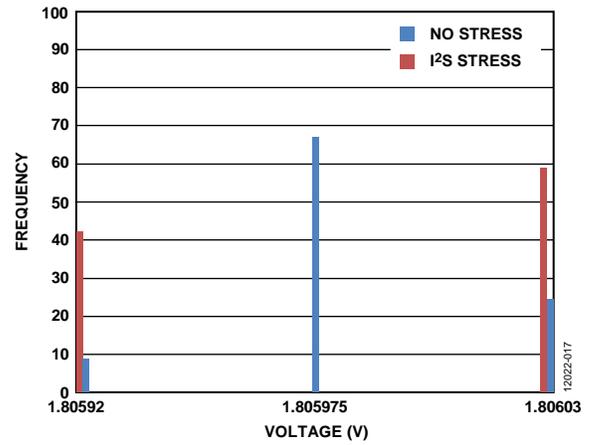
Figure 17. ½ DVDD Measurement Internally Through ADC Mux
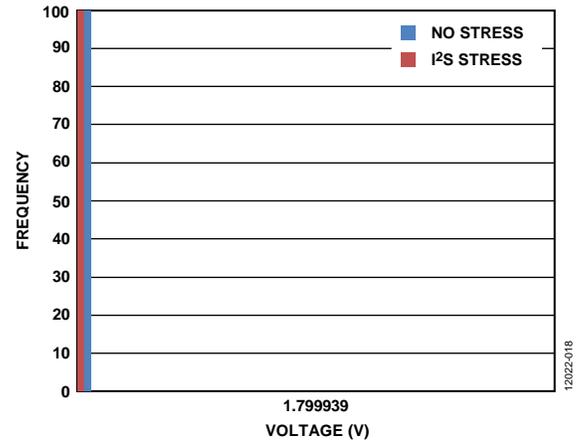
Figure 18. REF_EXCITE Measured Through Pin An_B

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