ANALOG DEVICES

EVAL-ADuM1250EBZ User Guide
UG-1100

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Evaluating the ADuM1250, ADuM1251, ADuM2250, and ADuM2251 Hot Swappable, Dual I²C Isolators

FEATURES

Access to two bidirectional data channels
Multiple connection options
Support for active probes
Provisions for cable terminations
Support for PCB edge mounted coaxial connectors
Easy configuration

SUPPORTED *i*Coupler DEVICES

ADuM1250, ADuM1251, ADuM2250, and ADuM2251

GENERAL DESCRIPTION

The EVAL-ADuM1250EBZ supports two bidirectional channels for evaluation of isolated I²C interfaces in 8-lead SOIC packages. The evaluation board provides a JEDEC standard, 8-lead SOIC_N pad layout. This layout supports signal distribution, loopback, and loads referenced to the VDDx or GNDx planes, as well as optimal bypass capacitance. Signal sources can be conducted to the board through header pins or through edge mounted Sub-miniature Version A (SMA) connectors (SMA connectors must be ordered separately). Screw terminal blocks on the evaluation board provide power connections. The board includes 200 mil (5.08 mm) header positions for compatibility with active probes (probe header pins must be ordered separately).

The EVAL-ADuM1250EBZ evaluation board can be used to evaluate the ADuM1250, ADuM1251, ADuM2250, and ADuM2251 devices. Although the pad layout on the EVAL-ADuM1250EBZ does not support the ADuM2250 and ADuM2251 16-lead SOIC_W and SOIC_IC packages, these devices are functionally equivalent to the ADuM1250 and ADuM1251, respectively, for the purposes of evaluation. They differ only by package and isolation capabilities. Therefore, evaluations of the ADuM1250 and ADuM1251 can be applied to the ADuM2250 and ADuM2251 as well.

The evaluation board follows best printed circuit board (PCB) design practices for 4-layer boards, including a full power and ground plane on each side of the isolation barrier. No other electromagnetic interference (EMI) or noise mitigation design features are included on this evaluation board. For high speed operation, or when ultralow emissions are required, refer to the AN-1109 Application Note for additional evaluation board layout techniques.

Full specifications for the ADuM1250 are available in the ADuM1250 data sheet, which must be consulted in conjunction with this user guide when working with the evaluation board.

EVALUATION BOARD PHOTOGRAPH

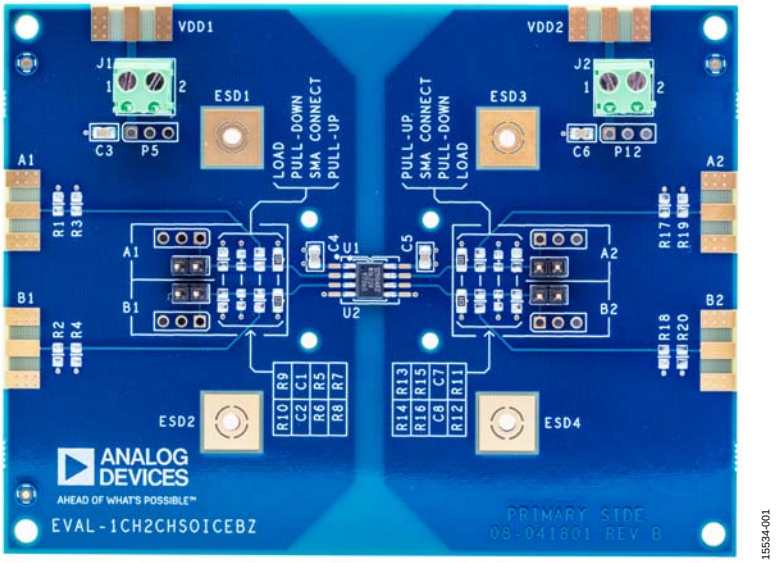

Figure 1.

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REVISION HISTORY

11/2017—Revision 0: Initial Version

EVALUATION BOARD CIRCUITRY

PCB EVALUATION

The EVAL-ADUM1250EBZ evaluation board is designed to do the following:

- Evaluate the full range of *i*Coupler data transfer functions.
- Independently power each side of an *i*Coupler isolator.
- Allow high differential voltage to be applied between the two sides of an *i*Coupler isolator. Note that this evaluation board is intended for evaluation of the components, but has not been safety certified for high voltage operation. If differential voltages above 60 V are applied, external safety measures appropriate for the voltage must be in place.
- Allow easy connection to power supplies, data channels, and instrumentation.

The EVAL-ADuM1250EBZ evaluation board ships installed with an ADuM1250 dual I^2C isolator, power terminals, bypass capacitors, and header pins for access to the data channels. The EVAL-ADuM1250EBZ evaluation board is also compatible with the ADuM1251 device. The ADuM1251 digital isolators must be ordered and installed separately in place of the ADuM1250.

CONNECTORS

The PCB provides support for three types of interconnections:

- Terminal blocks for power connections (preinstalled).
- Through-hole signal ground pairs (on PCB).
- SMA edge mounted connectors (ordered separately).

With these three options, both temporary and permanent connections to the evaluation board can be made.

When coaxial connections are required, SMA connector positions are available for digital input/output (I/O) signals and the VDDx power supplies. The SMA connector positions are unpopulated on the board when it ships and must be ordered separately from a distributor. Table 1 lists an example device number.

Power can be connected through the J1 and J2 screw terminals or through the optional VDDx SMA connectors. Signals can be routed on and off the evaluation board with the provided header pins or the optional SMA connectors. The pin spacing of each through-hole connector is 100 mil (2.54 mm) between the centers. There are additional through-hole pairs at signal test points with 200 mil (5.08 mm) spacing provided for active scope probes. These header pins must be added separately.

INPUT POWER

Each side of the ADuM1250 isolator requires its own off-board power source. The VDD1 and VDD2 supplies are routed in through the J1 and J2 screw terminals (or through the optional VDDx SMA).

Divided power and ground planes are present on Layer 2 and Layer 3 of the PCB on each side of the isolation barrier. These configurations are shown in Figure 6 and Figure 7, respectively.

DATA I/O STRUCTURES

Each data channel has a variety of structures to configure, load, and monitor both the input and the output. Figure 2 shows an example of the routing from an external connection to the pin of the device under test (DUT). Each data channel has similar connections.

Starting at the external connection, the signal path is constructed in the following order (see Figure 2 for the locations of these components):

1. A pad layout for a PCB edge mounted SMA connector.
2. Two 0805 pads where 100 Ω resistors to ground can be installed; the combined resistance is 50 Ω to provide a termination for a standard coaxial cable.
3. A standard 0805 pad layout that allows the coaxial and termination structures to be connected to the rest of the signal path.
4. A 0603 pad layout between the signal path and VDDx for a pull-up resistor, if required.
5. A populated 2-pin header to provide a signal ground pair for use with clip leads or for temporarily shorting a channel to ground.
6. Groupings of three open through holes, consisting of a signal and two ground connections. These holes can be used for hardwiring signal wires into the PCB, installing a header to accept an active probe, or installing a 2-pin header to allow adjacent channels to be shorted together temporarily.
7. A 0805 pad layout between the signal and GNDx where a load capacitor or pull-down resistor can be installed.

BYPASS CAPACITANCE ON THE PCB

Several positions and structures are provided to allow optimal bypass capacitance for the DUT on the evaluation board. The EVAL-ADuM1250EBZ board has surface-mount 10 µF bulk capacitors installed near the power connectors to compensate for long cables to the power supply (C3 and C6).

HIGH VOLTAGE CAPABILITY

This PCB is designed in adherence with 2500 V basic insulation practices. High voltage testing beyond 2500 V is not recommended. Do not rely on the evaluation board for safety functions.

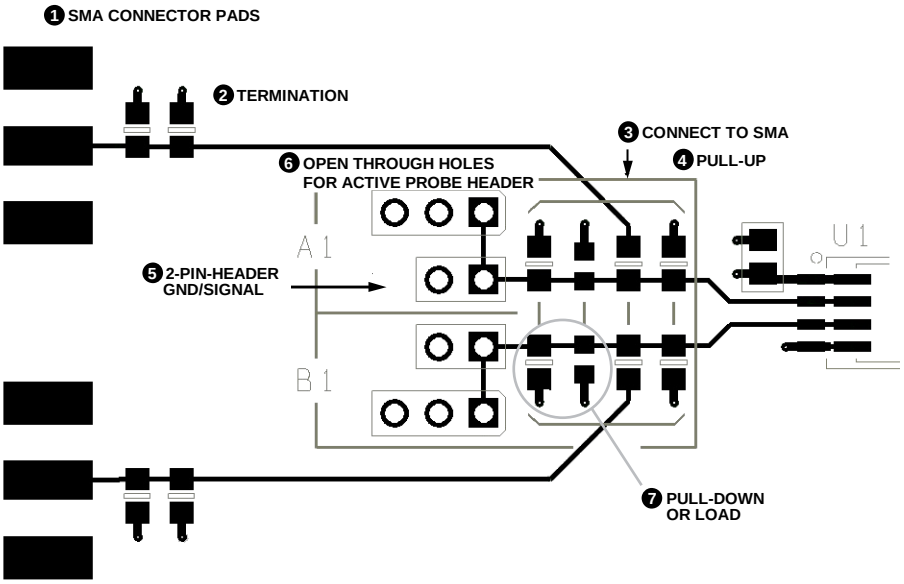

Figure 2. Detail of Signal Path

FEATURES OF THE ADUM1250

ADUM1250 OVERVIEW

The ADuM1250 is a hot swappable, bidirectional digital isolator compatible with I²C interfaces. The ADuM1250 provides two bidirectional channels for the SDA and SCL lines. The ADuM1251 has a unidirectional SCL channel for applications that do not require a bidirectional clock.

HOT SWAP

The ADuM1250 can be inserted to a powered system with an active bus. After being inserted into a powered system, signal lines may make contact before the digital isolator is powered. A high signal on a bus line powers the device parasitically through the electrostatic discharge (ESD) structure, which may disturb bus communication. To eliminate this behavior, the ADuM1250/ ADuM1251 do not have the pin to V_{DD2} ESD diode on the SDA_2 pin and the SCL_2 pin. The secondary side of the ADuM1250 must make the hot swap connection to use this feature, because the SDA_1 pin and the SCL_1 pin do have pin to V_{DD1} ESD diodes in place. External diodes are recommended on the bus lines for additional ESD protection.

V_{OL} LEVELS

The primary and secondary side channels of the ADuM1250 differ in logic low output (V_{OL}) level. The secondary side of the ADuM1250 device is I²C compliant and pulls an output low down to a typical complementary metal-oxide semiconductor (CMOS) V_{OL} level. The primary side, however, is I²C compatible and produces a V_{OL} of 0.9 V. Devices connected to the primary side of the ADuM1250 must be I²C compliant, or have standard CMOS levels for robust communication.

The ADuM1250 uses a pair of unidirectional isolation channels to create both the SDA and SCL bidirectional channels. The secondary side of the ADuM1250 has each pair of forward and reverse channels connected input to output, as shown in Figure 3. Directly connecting the channels on both sides of the ADuM1250 is not possible because it causes the logic to latch in the low state. To prevent the logic low latch, the primary side output buffer has a higher output low level, and the corresponding input buffer set to interpret this output low level has an input high level (see Figure 3 for functional details).

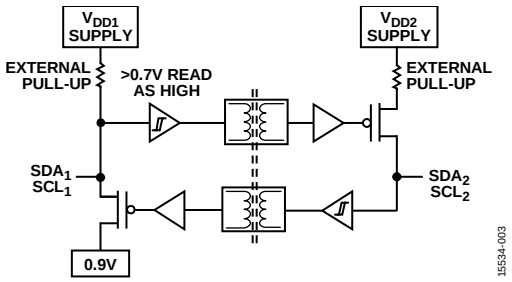

Figure 3. Functional Diagram of the ADuM1250 SDA and SCL Channels

EXTERNAL CIRCUITRY

The ADuM1250 SDA_1 pin, SDA_2 pin, SCL_1 pin, and SCL_2 pin are open collector outputs. Each requires an external pull-up resistor to set a high level. The EVAL-ADuM1250EBZ evaluation board ships with 10 kΩ 0805 pull-up resistors installed in the R7, R8, R13, and R14 positions, which can easily be modified. The pull-up resistors on the EVAL-ADuM1250EBZ evaluation board tie the channels to the same supply as their power pin.

The open collector output sinks current through the external pull-up resistors to drive the data channel low. The sink current limit, at which the device maintains required V_{OL} levels, is given in the ADuM1250 data sheet. Exceeding these current limits causes the V_{OL} levels to rise and can cause unreliable communication. Note that the secondary side outputs have greater drive strength than the primary side outputs. In applications in which a highly capacitive bus is driven, it is recommended that the ADuM1250 be oriented such that the secondary side outputs drive the bus.

The ADuM1250 data sheet also specifies resistance values to meet timing specifications at the maximum data rate. At lower data rates, greater pull-up resistances can be used while still maintaining signal integrity. Increasing the pull-up resistance values for lower data rates decreases the total power consumption of the application.

The ADuM1250 also requires low effective series resistance (ESR) 0.1 µF bypass capacitors located close to the V_{DDx} pins. These capacitors are required for data integrity.

EVALUATION BOARD SCHEMATIC AND ARTWORK

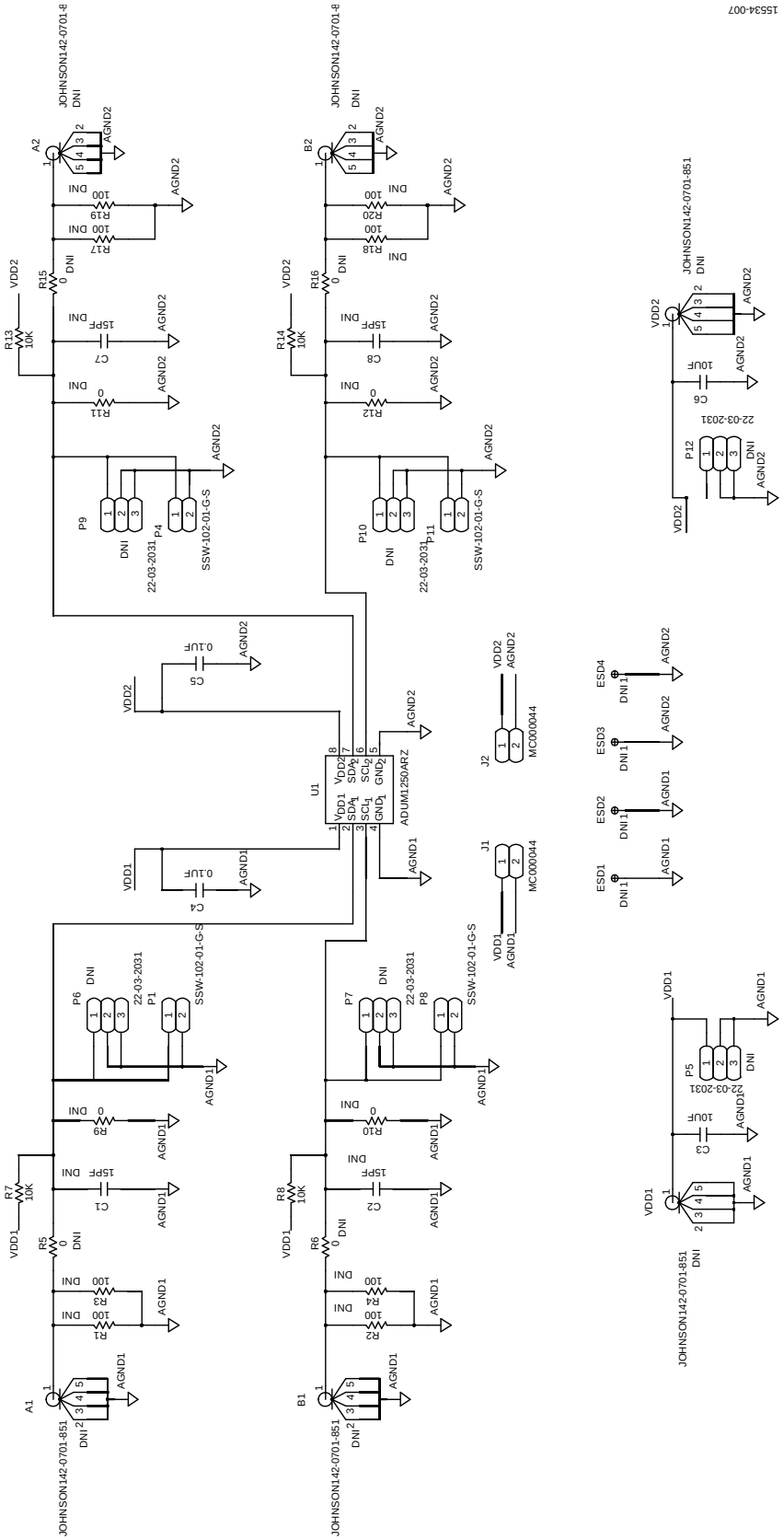

Figure 4. EVAL-ADM1250EBZ Schematic

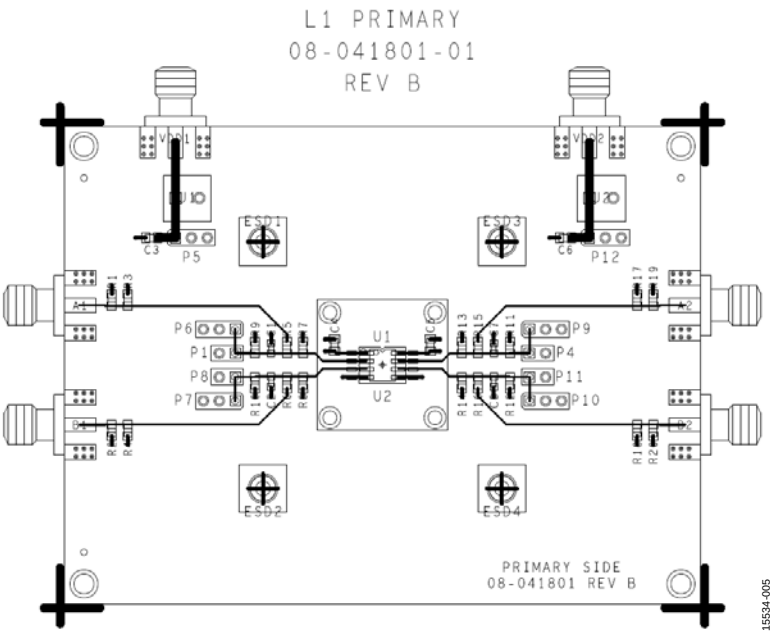

Figure 5. Top Level Signal Routing and Assembly (Layer 1)

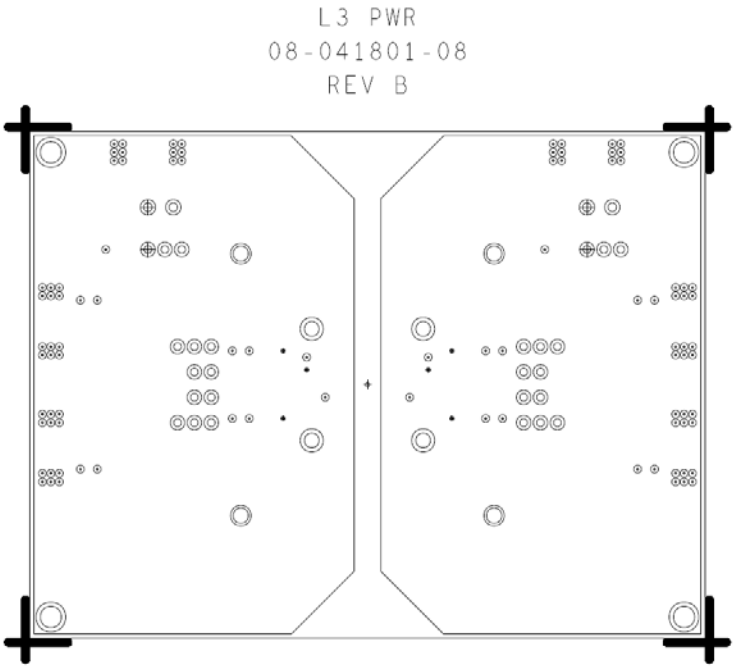

Figure 6. GND1 and GND2 Planes (Layer 2)

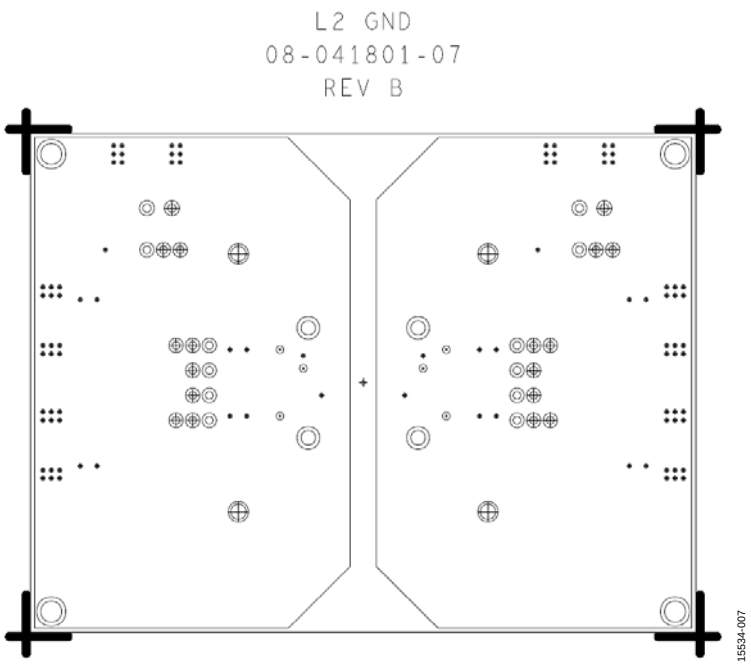

Figure 7. VDD1 and VDD2 Power Plane (Layer 3)

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Qty	Reference Designator	Description	Manufacturer	Part Number
1	U1	DUT	Analog Devices, Inc.	ADuM1250ARZ
4	R7, R8, R13, R14	0805, 10 kΩ resistors	Panasonic	ERA-6AEB103V
2	C3, C6	0805, 10 µF capacitors, CER monolithic	Murata	GRM21BR61C106KE15L
2	C4, C5	0805, 0.1 µF capacitors, chip X7R	Murata	GRM21BR71H104KA01L
2	J1, J2	PCB screw terminals	Multicomp	MC000044
4	P1, P4, P8, P11	2-pin headers, 100 mm spacing	Wurth	61300211121
6	A1, A2, B1, B2, VDD1, VDD2	SMA edge connectors (not installed)	Johnson	142-0701-851
6	P5 to P7, P9, P10, P12	2-pin headers, 200 mm spacing (not installed)	Not applicable	Not applicable
4	C1, C2, C7, C8	0603 signal loads (not installed)	Not applicable	Not applicable
8	R1 to R4, R17 to R20	0805, 100 Ω resistors (not installed)	Not applicable	Not applicable
12	R5, R6, R9 to R12, R15, R16	0805, 0 Ω resistors (not installed)	Not applicable	Not applicable