AN-1478
APPLICATION NOTE

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Isolated SPI Bus for Distinct System Requirements

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INTRODUCTION

A serial peripheral interface (SPI) is a synchronous serial bus interface often used for short distance communication between microprocessor and peripheral devices. The SPI bus is not a strictly governed protocol and can be implemented in various ways. There often arises the need or benefit to include galvanic isolation. This application note discusses various SPI isolation techniques to help designers facing distinct system level challenges, such as high communication speeds, limited printed circuit board (PCB) area, and low power consumption. This application note also serves as a selection guide for various SPI isolation solutions.

The SPI protocol typically consists of four unidirectional single-ended channels. The SPI master outputs three signals: clock, serial data, and slave select. From the slave device, a single serial data line returns to the master. At kbps and low mbps data rates, this physical layer makes SPI among the easier protocols to implement with galvanic isolation between the master and slave devices. Standard four channel digital isolators are often an adequate and transparent drop in solution for full duplex communication. Higher data rates require other techniques.

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REVISION HISTORY

5/2018—Revision 0: Initial Version

MAXIMIZING CLOCK SPEED

The more universal and traditional form takes shape as a single master device communicating in full duplex with one or more slave devices. The master initiates communication with a slave device by setting the chip select line low and transmitting a clock signal. Both master and selected slave write to the bus with the clocks rising edge and read in on the clocks falling edge. This form of SPI communication is used by the example systems shown in Figure 1 and Figure 3.

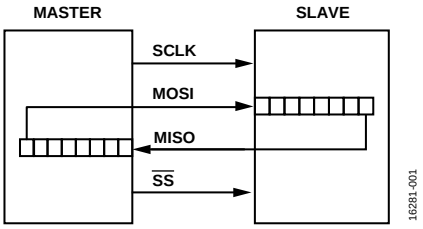

Figure 1. Standard SPI Implementation

STANDARD THREE FORWARD CHANNEL, ONE REVERSE CHANNEL (3/1) DIGITAL ISOLATORS

Adding isolation to directional channels is a straightforward process. Digital isolators are a natural choice for SPI isolation because these isolators offer low propagation delay, good channel to channel matching, a compact single chip solution, robust communications, and ease of implementation. These features give digital isolators an advantage over optocoupler solutions.

In data acquisition systems, the throughput rate is continuously climbing. Although propagation delays are short, these delays do impose a limit on the maximum data rate of full duplex communication. The effect is the difference between Figure 2 and Figure 4.

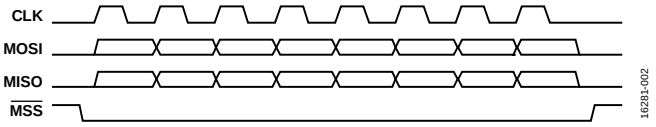

Figure 2. Standard SPI Timing Diagram

Clock Rate Limitations

Full duplex drop in implementations must consider several specifications of a digital isolator to calculate the maximum SPI clock speed. The minimum pulse width, the maximum data rate, and the propagation delay can all be limiting factors.

Figure 3 shows the SPI bus isolation using a generic 3/1 quad-channel standard digital isolator as a drop in solution for galvanic isolation. The SPI clock signal changes state twice per cycle, although this is not the case for the digital data passing through a digital isolator. The standard digital isolator must have a maximum data rate specification that supports the clock signal. In this example device, the maximum data rate specification is not the limiting factor.

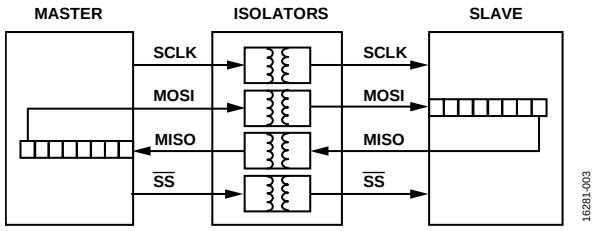

Figure 3. Standard Digital Isolator SPI Isolation

Notice the effect of propagation delay in Figure 4. In this example, data is transmitted on the rising clock edge and received on the falling edge.

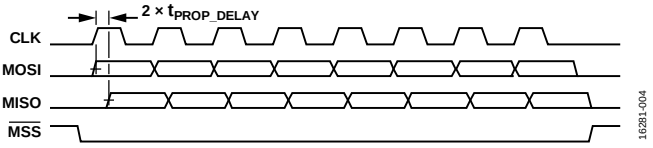

Figure 4. Standard SPI Timing Diagram with Isolation

The master device begins the transmission of the clock and master out, slave in (MOSI) signal simultaneously. Transmission by the slave device of the master in, slave out (MISO) signal is triggered by the rising clock edge, and because the clock edge is delayed, the MISO signal is also delayed. The MISO signal must then travel though the standard data isolator before reaching the master. In this example, data is read by both the slave and the master on the falling clock edge.

SPI communication is dependent on the clock signal synchronized to the MISO signal. Figure 5 shows the effect of propagation delay when the data rate is increased until communication breakdown. Because of the propagation delay, the falling edge of the clock causes a read point at the MISO signal transitions rather than when the MISO signal is settled. The data rate for this system is too high and has unreliable communication.

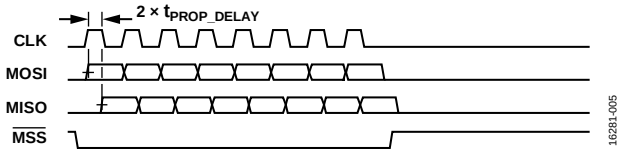

Figure 5. Timing Diagram from Perspective of Master

As shown in Figure 5, the propagation delay to the slave and back to the master must occur in less than half the SPI clock period. In applications, PCB trace delay, setup time, and slave response time can further reduce the maximum clock rate. These factors are ignored for simplicity in this application note, leaving the following relationship for drop in full duplex implementations:

$$\text{SPI Clock Half Period} \geq 2 \times t_{PROP\_DELAY}$$

Use the maximum propagation delay data sheet value to calculate the maximum data rate. Although systems may achieve higher speeds in a lab, temperature, supply voltage, and device variation must be considered for robust communication. Table 1 provides a guide for the maximum SPI data rates for a variety of Analog Devices, Inc., digital isolators.

Table 1. Drop In, Full Duplex Digital Isolator Maximum SPI Clock Rate

Part Number	Data Rate (Maximum)	Propagation Delay (Maximum)	Drop In, Full Duplex SPI Clock (Maximum)	Distinct Special Features
ADuM1401ARWZ	1 Mbps	100 ns	500 kHz[1]	Isolated SPI benchmark
ADuM1441	2 Mbps	180 ns	1 MHz[1]	Ultralow power, intrinsic safe for IS-IS isolation under IEC60079-11
ADuM7441	25 Mbps	50 ns	5 MHz	Cost sensitive basic insulation
ADuM141D/ADuM141E	150 Mbps	13 ns	19.2 MHz	High robustness to radiated and conducted noise, 1.8 V operation, package options as small as QSOP available
ADuM241D/ADuM241E	150 Mbps	13 ns	19.2 MHz	High robustness to radiated and conducted noise, 1.8 V operation, 5 kV withstand
ADuM3151/ADuM3152/ADuM3153	34 Mbps	14 ns	17.8 MHz	High data rate, three additional 250 kbps control/signal channels, small SSOP footprint
ADuM4151/ADuM4152/ADuM4153	34 Mbps	14 ns	17.8 MHz	High data rate, three additional 250 kbps control/signal channels, 5 kV withstand

[1] Limited by minimum pulse width specification.

INDEPENDENT DELAYED CLOCK (WRAPPED CLOCK)

Some full duplex applications require faster SPI data rates than can be achieved by simply inserting a standard data digital isolator into the SPI signal chain. The synchronization dilemma shown in Figure 5 can be managed by returning the clock signal along with the MISO signal to the master. Higher data rates are achievable; however, a consideration of employing this method is the additional complications to the SPI master design. Typically, an additional shift register is required to read in the delayed MISO and clock signals.

Implemented with standard data isolators, the independent delayed clock technique requires an additional isolation channel to return (or wrap back) the master clock signal. The wrapped clock signal returns to the master on the additional isolation channel. This delayed clock signal is delayed by the isolators forward and reverse propagation delay just as the MOSI signal trip to the slave and the MISO signal return are delayed (see Figure 6). Using a digital isolator with low channel matching timing specifications is important for this method. The minimum SPI clock period (without accounting for slave and trace delays) is determined by the maximum pulse-width distortion and codirectional channel matching specifications. Ensure that the calculated minimum SPI half clock is greater than the devices minimum pulse width specification.

$$\text{SPI Clock Half Period} \geq 2 \times t_{PWD} + t_{PSKCD}$$

The ADuM152N, for example, has 4.5 ns maximum pulse-width distortion and 4.0 ns maximum codirectional channel matching which theoretically leads to a maximum 38.4 MHz clock speed.

In practice, delays for trace length and slave response must be considered.

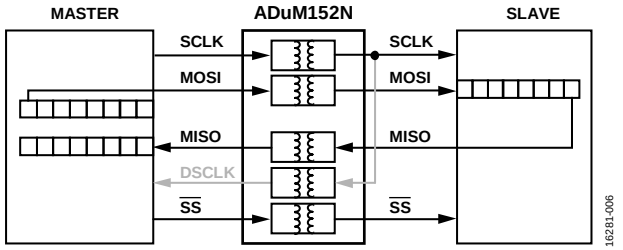

Figure 6. High Speed SPI Using Isolation Channel Delay

The ADuM3150 and the ADuM4150 SPI digital isolators provide a tuned delayed clock signal as a standard feature. As is shown in Figure 7, the ADuM3150 implements a delay circuit on the primary side. The ADuM4150 also implements a delay circuit on the primary side. The delayed clock (DCLK) signal is trimmed during the ADuM3150 production test to match the round trip propagation delay of each isolator. Unlike Figure 6, the ADuM3150 eliminates the need for the extra isolation channel. These SPI digital isolators can accommodate a clock rates of up to 40 MHz.

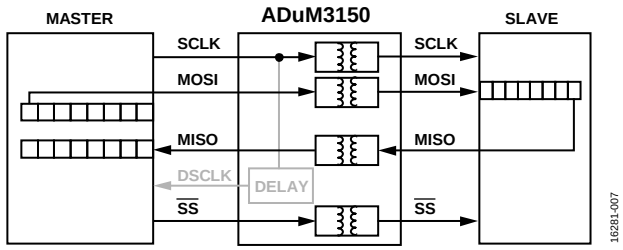

Figure 7. High Speed SPI Using Precision Clock Delay

Table 2. Wrapped Clock SPI Data Rates

Part Number	Supply Voltage (V)	SPI Clock (Maximum)	Distinct Special Features
ADuM152N/ADuM162N	1.7 to 5.5	38.4 MHz	High robustness to radiated and conducted noise, 1.8 V operation
ADuM252N/ADuM262N	1.7 to 5.5	38.4 MHz	High robustness to radiated and conducted noise, 1.8 V operation, 5 kV withstand
ADuM3150/ADuM4150	3.0 to 5.5	40 MHz	Delayed clock feature, two additional 250 kbps control/ signal channels, small SSOP footprint

DELAYED READBACK ISOLATOR

Instead of adding a delayed clock signal to synchronize the delayed MISO data signal, a delayed readback isolator buffers the MISO data on the primary side until the following word is clocked on the bus. Buffering the MISO data removes the need for the master to support a delayed clock. This process requires that the application tolerate a one word delay in the MISO data. For applications in which the data is primarily written from the master to the slave, this is not a significant limitation. The delayed readback technique is implemented by the LTM2895, which also includes three bidirectional select signals and a low jitter $\overline{\text{LOAD}}$ signal, making the device ideal for isolating digital-to-analog converters (DACs).

The LTM2895 supports SPI bus operation with 100 MHz clocks by only transferring across the isolation barrier the salient edges for the key signals (see Figure 8). Using a combination of integrated state machines and a buffer, the LTM2895 can fully regenerate the SPI signals. The required configuration information, such as SPI clock frequency and word length, are configured via the SPI interface and secondary slave select ($\overline{\text{SSB}}$). After the LTM2895 is configured, this secondary slave select can be repurposed to allow writing to a second isolated side SPI device.

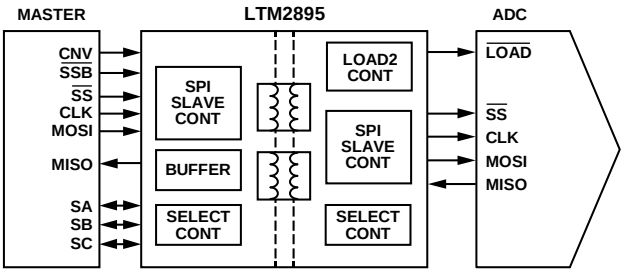

Figure 8. Super High Speed DAC Streaming Isolator

The primary and secondary sides of the LTM2895 internally communicate across the isolation barrier by using high speed asynchronous serial links, one forward and one reverse. A preemptive prioritization scheme assures that the timing critical signals are updated with low latency and jitter.

Figure 9 shows the LTM2895 normal operational sequence that starts with the falling edge of the primary side ($\overline{\text{SS}}$) which generates a corresponding falling edge on the secondary side ($\overline{\text{SS2}}$) and causes MISO to output the MSB of the previously sampled MISO2 word. The first rising edge of the primary side SCLK triggers the LTM2895 to sample MOSI and send the information across the barrier. When the secondary side state machine receives this data, the machine updates MOSI2 and leaves SCLK2 low for a fixed time (determined by the SPI clock frequency configuration). After the specified low time for SCLK2 has elapsed, the secondary side state machine raises SCLK2, samples MISO, and then sends the data to a primary side buffer. When the primary side SCK falls, the buffered MISO data is updated. Subsequent rising edges of SCLK forces SCKL2 low for the defined time while the other signals remain the same. The SPI transaction ends when $\overline{\text{SS}}$ rises, driving MISO high-Z and causing the secondary side SCLK2 and MOSI2 low and $\overline{\text{SS2}}$ high. Because MISO is high-Z when the LTM2895 is not selected, MISO can share the primary side SPI bus with other slave devices.

The MISO data buffer is circular and uses read and write pointers that are separated by the configured word size.

When SPI clock frequencies of 66 MHz or 100 MHz are selected, the LTM2895 updates the primary side MISO data on the rising SCK edge to provide additional propagation and set up time.

SPI page mode is supported by holding $\overline{\text{SS}}$ low while clocking as many multiples of the word length as desired.

When isolating a DAC with a $\overline{\text{LOAD}}$ DAC input, the LTM2895 $\overline{\text{LOAD}}$ signal produces a narrow pulse with a typical jitter of 30 ps rms between the falling edges. The rising edge of $\overline{\text{LOAD2}}$ is generated by the LTM2895 with a pulse width of either 40 ns or 60 ns depending on SCLK2 frequency setting.

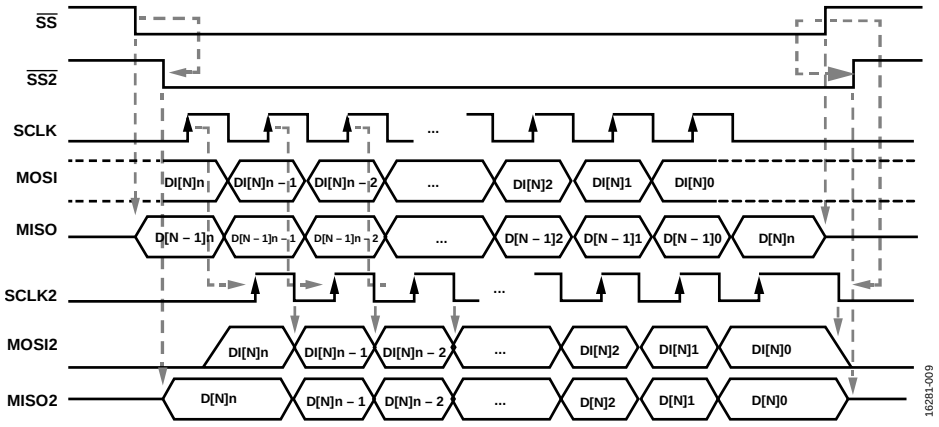

Figure 9. LTM2895 SPI Timing

INTEGRATED ISOLATED POWER

Independent power supplies may be uneconomical or not feasible in some applications. In these designs, isolated power from the primary side is required to supply the secondary side devices. Traditional isolated power solutions are bulky and struggle to meet isolation robustness and certification requirements. These challenges can be addressed simply by several *iso*Power® or µModule® devices. The ADuM5411 is one such solution (see Figure 10). The device provides four isolated signal channels with up to 150 mW integrated isolated power while only occupying a mere 90 mm² PCB area including supporting bypass capacitors. An integrated isolated power of 150 mW is often enough to support a precision ADC or low power microcontroller unit (MCU).

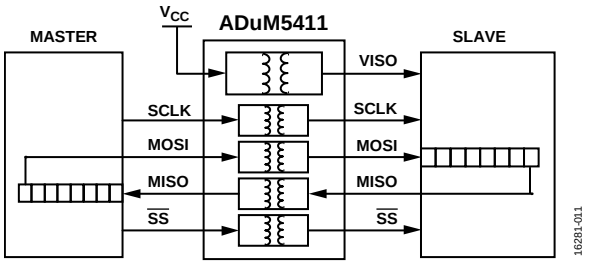

Figure 10. SPI Isolation with isoPower

For isolated SPI applications with higher isolated power requirements, additional solutions are shown in Table 3. The ADuM5401 can deliver isolated power up to 500 mW on its own. The ADuM5401 is also designed with the capability to control additional compatible *iso*Power devices. The ADuM5401 can work as a master and send its pulse-width modulation (PWM) signal to one or more ADuM5000 devices, regulating itself and each slave ADuM5000 device.

The LTM2883-S, LTM2886-S, and LTM2887-S are 6-channel digital µModule isolators capable of delivering up to 1 W output power with various output voltage range options.

The ADuM3471 integrates four isolated data channels for SPI along with a switching regulator. The device provides up to 2 W of regulated, isolated power at 3.3 V to 24 V using an external transformer. The ADuM3471 output capability makes it suitable to deliver isolated power in a system that requires higher power and a wider voltage range, such as analog output modules.

Table 3. SPI Signal Isolation with Integrated Isolated Power

Part Number	Isolated Supply Voltage	Isolated Power	Data Rate (Maximum)	Drop In, Full Duplex SPI Clock (Maximum)
ADuM5411	Adjustable 3.3 V to 5 V	150 mW	150 Mbps	19.2 MHz
ADuM5401	Fixed 3.3 V or 5 V	500 mW	25 Mbps	4.1 MHz
ADuM5401/ADuM5000	Fixed 3.3 V, 5 V	1 W	25 Mbps	4.1 MHz
LTM2883-S	Fixed 5 V Fixed +12.5 V Fixed −12.5 V	100 mW 250 mW 187.5 mW	20 Mbps	4 MHz
LTM2886-S[1]	Adjustable 3.0 V to 5 V Fixed +5 V Fixed −5 V	500 mW 500 mW 500 mW	20 Mbps	4 MHz
LTM2887-S	Adjustable 3 V to 5 V Adjustable 0.6 V to 5 V	500 mW 500 mW	20 Mbps	4 MHz
ADuM3471	Adjustable 3.3 V to 24 V	2 W	25 Mbps	4.1 MHz

[1] Total output power is up to 1 W.

AUXILIARY DATA CHANNELS

Besides multiple slave selection, the low speed channel can also transmit additional control signals across the isolation barrier, as shown in Figure 11. In this case, the ADuM3152 low speed channel allows mixed channel direction, sending the reset signal from the master to the slave, while sending power good and interrupt signals in the opposite direction. Different auxiliary data channel direction combinations are created by different devices in the SPIsolator® device family.

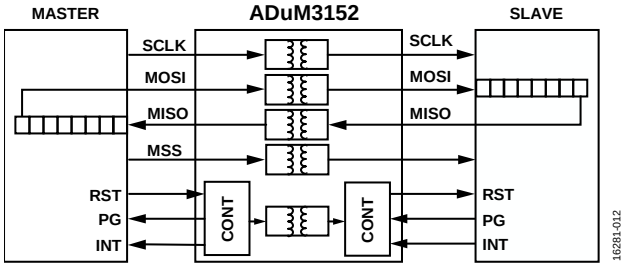

Figure 11. SPI Isolation with Supplemental Functions

MULTIPLE SLAVE CONTROL

There are two ways to tie multiple slaves to an SPI bus: a daisy chain or an independent slave configuration. A daisy chain only requires a single slave selection (SS) line and shifts the entire contents of the chain out serially through a single isolated port. When the sequence of data acquisition is not fixed, each SPI slave must be addressed individually.

One straightforward solution is to add more digital isolation channels, such as the ADuM161N. This solution is recommended for a system desiring accurate timing of the SS signal. For example, when the slaves are ADCs, the SS signal also initiates data conversions.

In loose timing constraint applications, the ADuM3154 isolator with integrated four high speed channels and one low speed channel provides an alternative solution, as shown in Figure 12. The ADuM3154 supports a maximum SPI clock speed of 17 MHz and controls up to four independent slaves. The propagation delay for mux select lines is between 100 ns and 2.6 µs, depending on where the input data edge changes with respect to the internal sample clock. By eliminating three isolation channels, this solution is more compact and cost effective compared to the standard digital isolator solution.

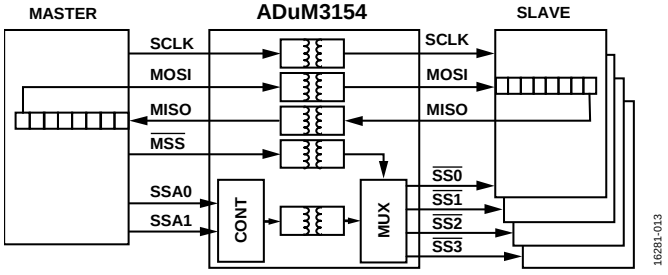

Figure 12. SPI Isolation with Multiple Slave Control

When a master is communicating with multiple slaves on separate isolated planes, such as in Figure 13 the digital isolators must have the ability to tristate the MISO line on the master side. Without tristating the MISO, communication is not possible because the output pins of the digital isolator are in contention.

A tristate buffer on the MISO signal from the isolator is also required with a master and nonisolated and isolated slaves.

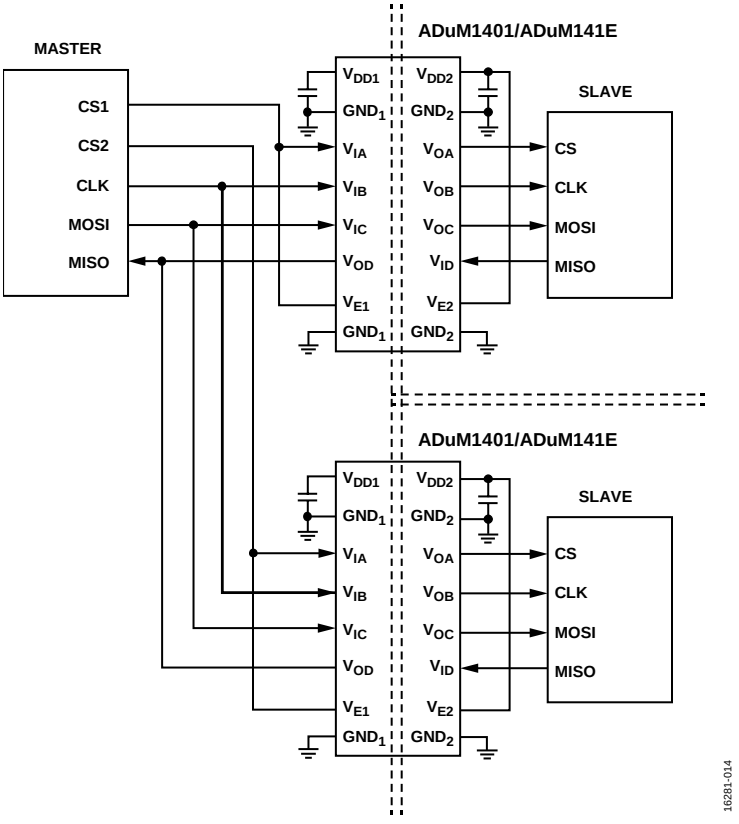

Figure 13. MISO Tristate for Slaves Isolated from One Another

ULTRALOW POWER APPLICATIONS

Isolation is considered necessary for safe electronic systems, but isolation is also considered a burden because it limits communication speed, occupies board space, and consumes a considerable amount of power. The former two are addressed by innovations that maximize the clock speed and minimize the board space. There are some applications that require ultralow power consumptions, such as battery-powered devices and 4 mA to 20 mA loop-powered industrial transmitters. Currently, the power consumption in digital isolators, while significantly lower than the optocoupler, must be two to three orders of magnitude lower to allow entry into these new application domains.

After the data rate is fixed, the power level in the digital isolator is primarily determined by the data encoding schemes, which can broadly be divided into pulse encoding architecture and on-off keying (OOK) architecture. The pulse encoding scheme shows the advantage of consuming low supply current at low data rates, while the OOK consumes less current at high data rates (above 10 Mbps) than the pulse encoding method. In most low power applications, the SPI clock speed runs at less than 1 MHz, which makes the pulse encoding scheme a better choice.

The pulse encoding scheme does have one drawback. If there are no logic changes at the input, no data is sent to the output. A mismatch between input and output can occur after system power-up, or external noise can upset the output data. Resending the dc status on a regular basis can solve this problem. Most pulse encoding digital isolators refresh the dc status every 1 µs, but the refresh rate also sets a point where the power consumption stops to decline as the data rate drops.

The ADuM1441 offers ultralow power consumption by reducing the refresh rate to 17 kHz. For the lowest possible power consumption, the refresh circuits can be disabled completely. As shown in Figure 14, the ADuM1441 pushes power consumption down to the µW range with the fresh circuit disabled. The system designer can send a dc correctness pulse at a much lower frequency to balance between power consumption and data integrity.

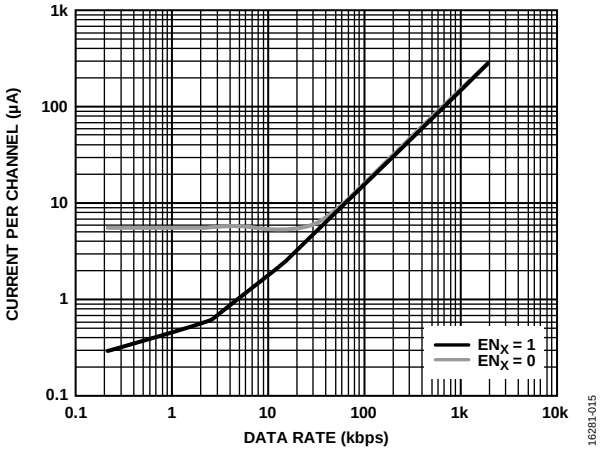

Figure 14. Total Supply Current per Channel for ADuM1441 (V_{DDX} = 3.3 V)

The majority of field instruments are loop-powered devices. The power taken from the loop must power everything inside the instrument, including the sensor and all supporting electronic circuitry. Because the minimum loop current is 4 mA, the 3.5 mA maximum allowable system power budget available for such a design cannot be increased. Power consumption is a primary consideration when selecting components for field transmitter designs. Most standard data digital isolators draw several mA current on both sides, while the ADuM1441 and its ultralow power consumption enables this functionality in isolated field instruments as shown in Figure 15.

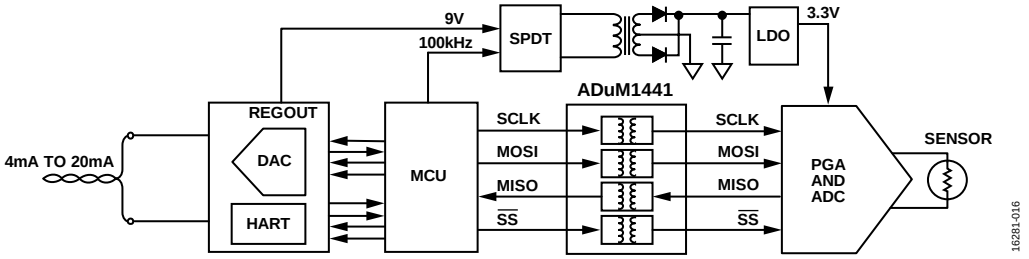

Figure 15. Ultralow Power SPI Isolation in a 4 mA to 20 mA Loop-Powered Instrument

CONCLUSION

SPI bus isolation can be more complex than merely inserting a quad-channel digital isolator between the master and the slave. Data acquisition systems requiring galvanic isolation for noise immunity and safety no longer sacrifice throughput. Recent innovations enable an isolated clock speed up to 100 MHz. This is the first time that an invisible isolator (that is, one that does not slow down clock speeds) becomes viable at such high speeds. Integrated signal and power isolation in a small package dramatically simplifies the design for SPI isolation with secondary power supply and significantly reduces board space and cost compared to discrete solutions. Integrating additional low speed isolation channels offers compact and cost effective options for multiple slave control or auxiliary channel applications. Advanced pulse encoding technology optimized for extremely low power enables SPI isolation not previously possible due to limited power supply.

For more information on any of the products mentioned in this application note, visit www.analog.com/icoupler.

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