AN-1536
APPLICATION NOTE

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ADuM4135 Gate Driver Performance Driving APTMC120AM20CT1AG SiC Power Switches

by Martin Murnane

INTRODUCTION

In solar photovoltaics (PV) and energy storage applications, there is a trend towards increased power density, along with the ever present need of improved efficiency. A solution to this problem comes in the form of silicon carbide (SiC) power devices. SiC devices are wide band-gap devices that can operate at an increased voltage of >1000 V dc and tend to have a low drain source impedance (R_{DSON}). SiC devices also fill the need for reduced conduction and, therefore, increased efficiency. SiC devices can also exhibit fast switching speeds of >100 kHz with low parasitic capacitance and associated charge during switching. However, disadvantages include a requirement for higher common-mode transient immunity (CMTI) greater than 100 kV/µs required for gate drivers. Another disadvantage is that higher switching across the drain source of the SiC can lead to ringing at the gate of the device. These disadvantages can cause problems when driving higher voltage SiC devices, where significant power density improvement can be achieved by their implementation. One combination of gate driver and SiC that can solve these problems is the ADuM4135 and the Microsemi APTMC120AM20CT1AG module. The ADuM4135 gate driver is a single-channel device with a typical drive capability of 7 A source and sink at a 25 V operating voltage (V_{DD} to V_{SS}). It has a minimum CMTI of 100 kV/µs. The APTMC120AM20CT1AG power module is a half bridge SiC device with a 1200 V collector emitter voltage rating, R_{DSON} of 17 mΩ, and a continuous current capability of 108 A. Its gate source voltage (V_{GS}) rating is −10 V to +25 V.

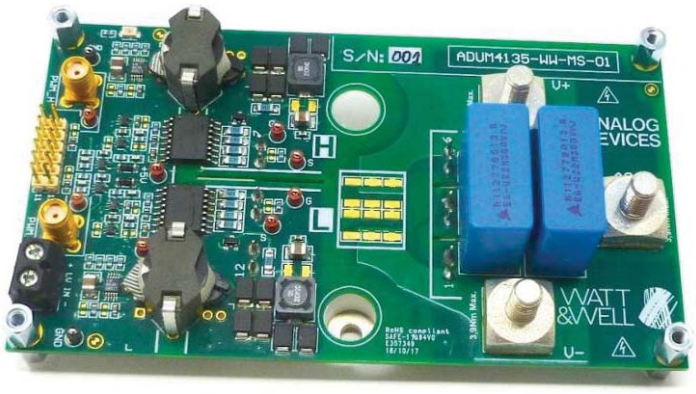

Figure 1. ADuM4135 Gate Drive Module

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REVISION HISTORY

4/2018—Revision 0: Initial Version

TEST SETUP

ELECTRICAL SETUP

The system test circuit setup is shown in Figure 2. A dc voltage is applied to the inputs across the full half bridge, where a decoupling capacitor of 900 µF is added to the input stage. The output stage is an inductor capacitor (LC) filter stage of 83 µH and 128 µF, filtering the output into the load, R1, of 2 Ω to 30 Ω.

Table 1 shows a list of the test setup power components. A physical setup is shown in Figure 3, and Table 2 details the setup equipment used for testing.

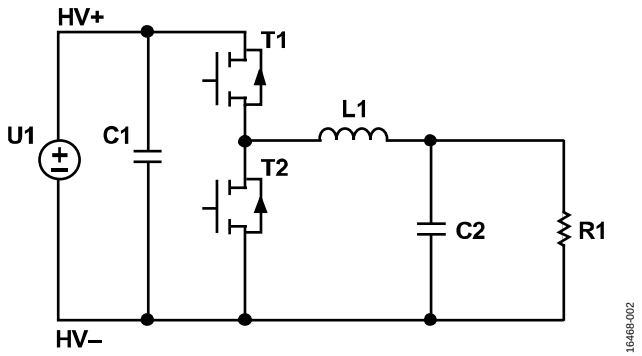

Figure 2. System Test Circuit Setup

Table 1. Test Setup Power Components

Equipment	Value
U1	200 V to 900 V
C1	900 µF
L1	83 µH
C2	128 µF
R1	2 Ω to 30 Ω

Table 2. Setup Equipment Used for Testing

Equipment	Manufacturer	Type
Oscilloscope	Keysight	DSO-X 3024T
DC Supply	Delta Elektronika	SM 660-AR-11 (two in serial)
Gate Driver Board	Watt&Well	ADUM4135-WW-MS-01 SN001
Waveform Generator	Agilent	33522A
Current Probe	Hioki	3275
Passive Voltage Probe	Keysight	N2873A 500 MHz
Passive High Voltage Probe	Elditest	GE3421 100 MHz

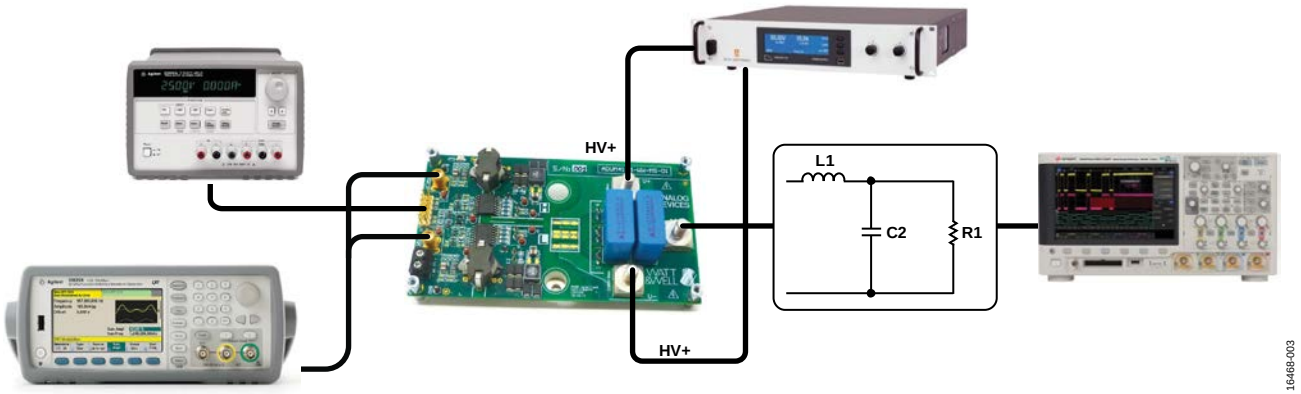

Figure 3. Physical Setup

TEST RESULTS

NO LOAD TESTING

Table 3. No Load Testing—Figure Assignments

Test	V_{HV} (V)[1]	Switching Frequency, f_{SW} (kHz)	Duty Cycle (%)	I_{IN} (A)[2]	Figures
1	600	50	50	0.26	Figure 4 and Figure 5
2	600	100	50	0.22	Figure 6 and Figure 7
3	900	50	50	0.37	Figure 8 and Figure 9

[1] V_{HV} is the differential voltage between HV+ and HV−.
[2] I_{IN} is the input current through U1.

Table 4. No Load Testing—Temperature Summary

Test	V_{HV} (V)	f_{SW} (kHz)	Ambient Temperature (°C)	Heatsink Temperature (°C)	DC-to-DC Power Supply Temperature, High-Side (°C)	DC-to-DC Power Supply Temperature, Low-Side (°C)	Gate Driver Temperature, High-Side (°C)	Gate Driver Temperature, Low-Side (°C)
4	600	50	20	21.3	25.4	25.4	34	33.5
5	600	100	20	23.5	31.5	31.5	42	42
6	900	50	20	23	29	29	37	37

In the latest revision of ADuM4135, some changes include: a capacitor of 2.2 nF was added on the gates of the power metal-oxide semiconductor field effect transistors (MOSFETs), Q1, and Q2. C0G decoupling capacitors of 15 nF have been added to V_{HV}. Table 3 and Table 4 summarize of the results observed, and Figure 4 through Figure 9 show the proof of results. Test 1 and Test 2 were carried out at 600 V, respectively, at 50 kHz and 100 kHz switching frequencies, whereas Test 3 was carried out at 900 V at a switching frequency of 50 kHz.

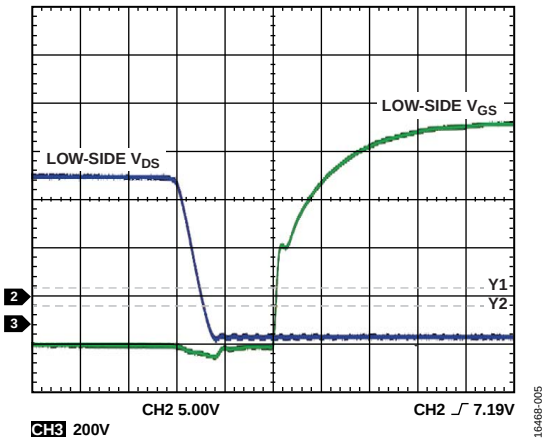

Figure 4. V_{HV} = 600 V, f_{SW} = 50 kHz, No Load, Turn On

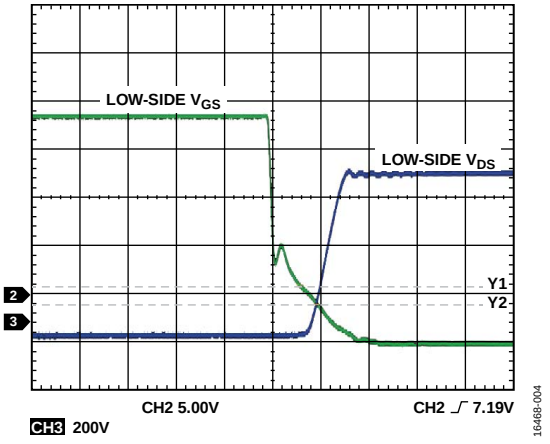

Figure 5. V_{HV} = 600 V, f_{SW} = 50 kHz, No Load, Turn Off

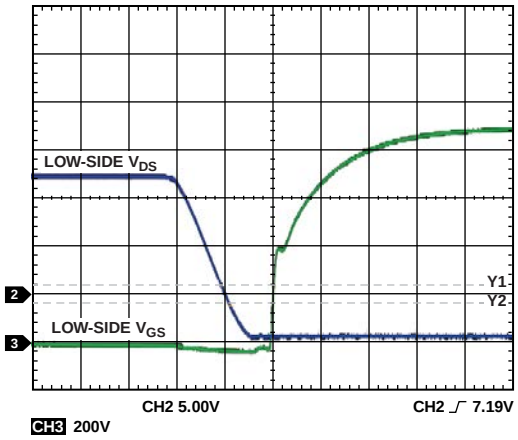

Figure 6. V_{HV} = 600 V, f_{SW} = 100 kHz, No Load, Turn On

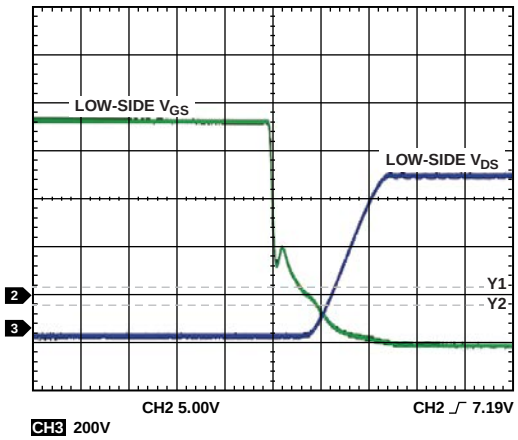

Figure 7. V_{HV} = 600 V, f_{SW} = 100 kHz, No Load, Turn Off

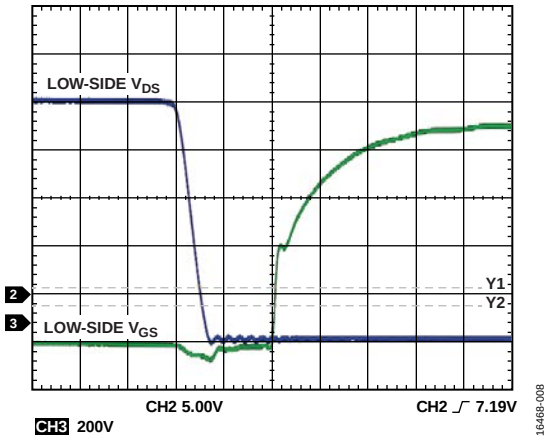

Figure 8. V_{HV} = 900 V, f_{SW} = 50 kHz, No Load, Turn On

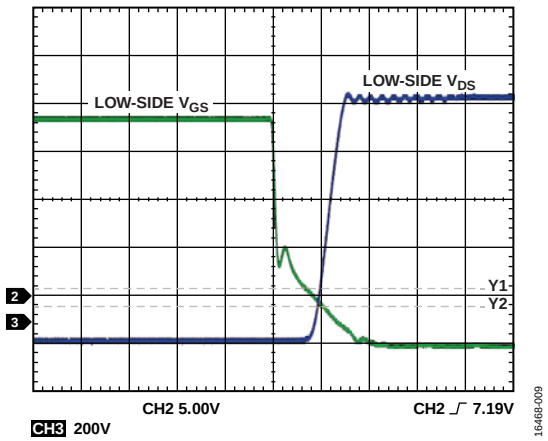

Figure 9. V_{HV} = 900 V, f_{SW} = 50 kHz, No Load, Turn Off

LOAD TESTING

Table 5. Load Testing

Test	V_{HV} (V)	f_{SW} (kHz)	Duty Cycle (%)	I_{OUT}[1] (A)	V_{OUT}[2] (V)	P_{OUT}[3] (W)	I_{IN}[4] (A)	Figures
4	200	50	25	1.7	48	83	0.55	Figure 10 and Figure 11
5	600	50	25	6.9	145	1000	1.66	Figure 12 and Figure 13
6	900	50	25	8.7	215	1870.5	2.47	Figure 14 and Figure 15
7	900	100	25	8.2	200	1640	2.13	Figure 16 and Figure 17

[1] I_{OUT} is the output current in Load Resistor R1.
[2] V_{OUT} is the output voltage across R1.
[3] P_{OUT} is the output power ($I_{OUT} \times V_{OUT}$).
[4] I_{IN} is the input current through U1.

Board configuration is similar to the test setup of the No Load Testing section.

Table 5 is a summary of the results observed for load testing, and Figure 10 through Figure 17 show the proof of results.

Output voltage (V_{OUT}) was measured as the voltage across R1. The test results show some Miller feedback on V_{GS}, but V_{GS} remains at the −5 V level at the gate of the SiC. At 900 V, some ringing is seen on V_{DS}, but it is <100 V of the input dc voltage. This design shows how the ADuM4135 can drive SiC MOSFETs with clean performance.

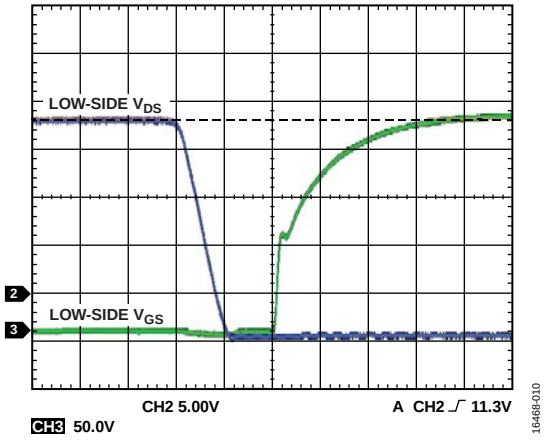

Figure 10. V_{HV} = 200 V, f_{SW} = 50 kHz, P_{OUT} = 83 W, Turn On

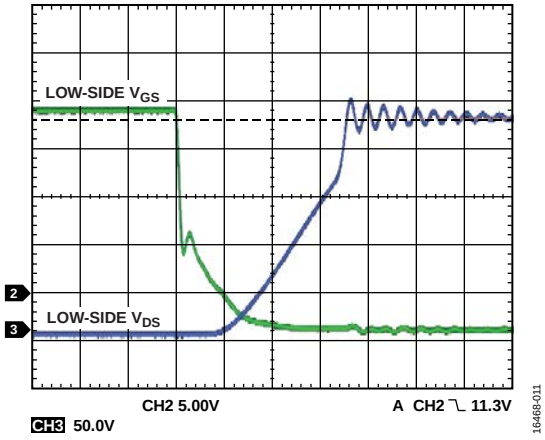

Figure 11. V_{HV} = 200 V, f_{SW} = 50 kHz, P_{OUT} = 83 W, Turn Off

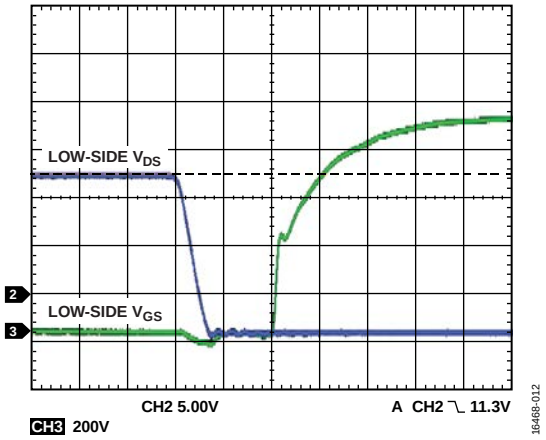

Figure 12. V_{HV} = 600 V, f_{SW} = 50 kHz, P_{OUT} = 1000 W, Turn On

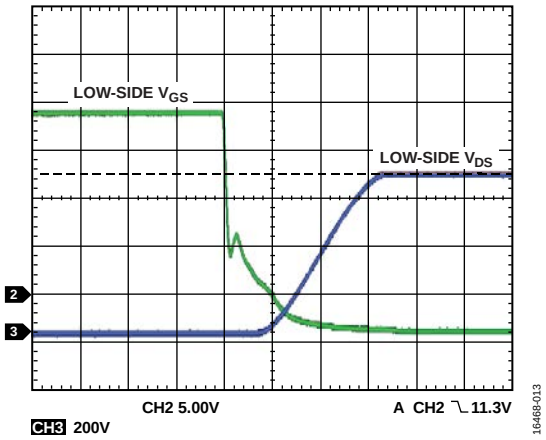

Figure 13. V_{HV} = 600 V, f_{SW} = 50 kHz, P_{OUT} = 1000 W, Turn Off

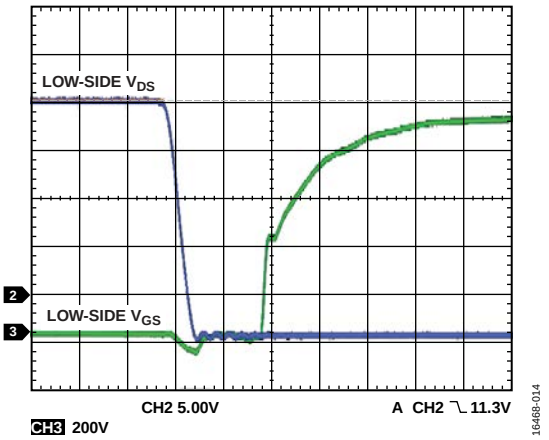

Figure 14. V_{HV} = 900 V, f_{SW} = 50 kHz, P_{OUT} = 1870.5 W, Turn On

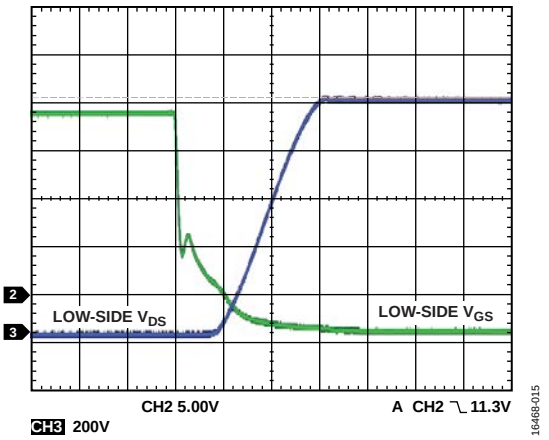

Figure 15. V_{HV} = 900 V, f_{SW} = 50 kHz, P_{OUT} = 1870.5 W, Turn Off

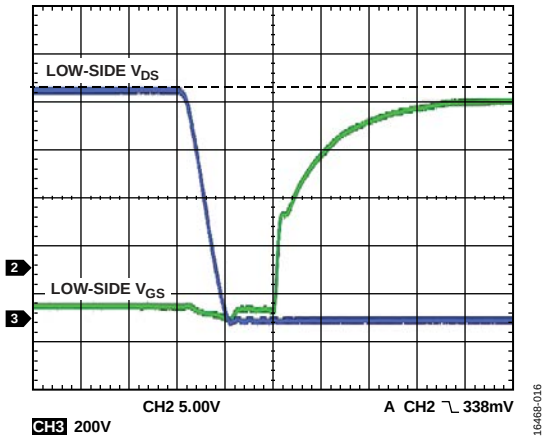

Figure 16. V_{HV} = 900 V, f_{SW} = 100 kHz, P_{OUT} = 1640 W, Turn On

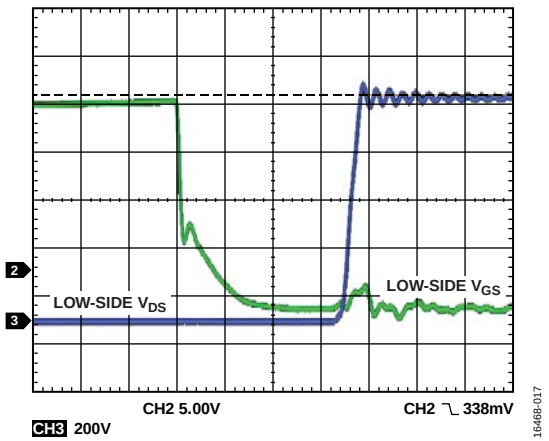

Figure 17. V_{HV} = 900 V, f_{SW} = 100 kHz, P_{OUT} = 1640 W, Turn Off

HIGH CURRENT TESTING

Table 6. High Current Testing

Test	V_{HV} (V)	f_{SW} (kHz)	Duty Cycle (%)[1]	I_{OUT}[2] (A)	V_{OUT}[3] (V)	P_{IN}[4] (W)	I_{IN}[5] (A)	Figures
4	300	50	25	21.8	70.14	1526	5	Figure 18 and Figure 19
5	400	50	25	27.1	93.8	2640	6.6	Figure 20 and Figure 21
6	600	50	25	40.5	141	6000	10	Figure 22 and Figure 23

[1] Duty cycle high side.
[2] I_{OUT} is the output current in Load Resistor R1.
[3] V_{OUT} is the output voltage across R1.
[4] P_{IN} is the input power ($I_{IN} \times V_{HV}$)
[5] I_{IN} is the input current through U1.

Board configuration is similar to the test setup of the No Load Testing section. A Regatron power supply was used in this test.

Table 6 is a summary of the results observed for high current testing, and Figure 18 through Figure 23 show the proof of results.

V_{OUT} was measured as the voltage across R1.

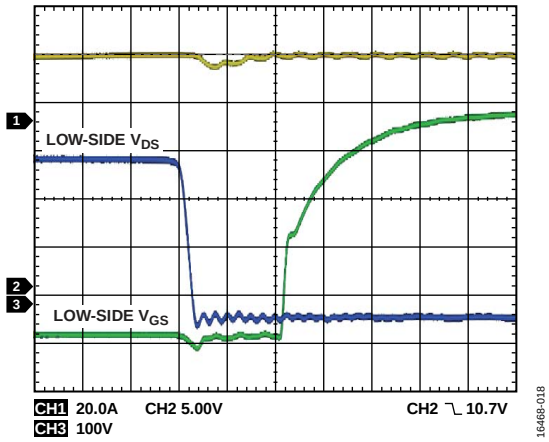

Figure 18. V_{HV} = 300 V, f_{SW} = 50 kHz, Output Current (I_{OUT}) = 21.8 A, Turn On

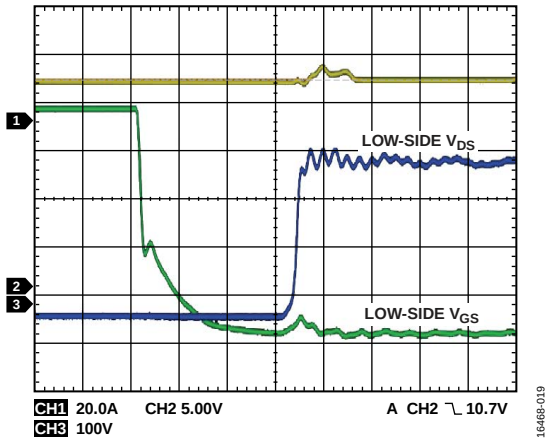

Figure 19. V_{HV} = 300 V, f_{SW} = 50 kHz, Output Current (I_{OUT}) = 21.8 A, Turn Off

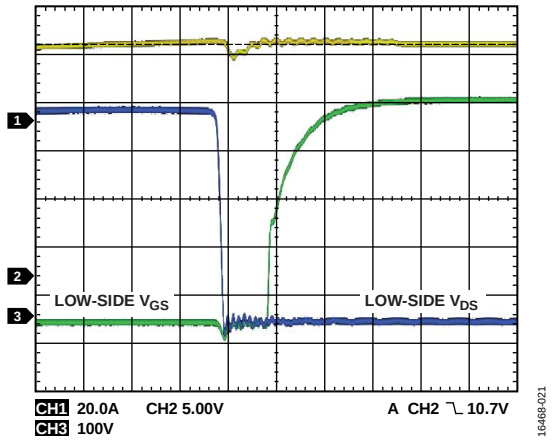

Figure 20. V_{HV} = 400 V, f_{SW} = 50 kHz, Output Current (I_{OUT}) = 27.1 A, Turn On

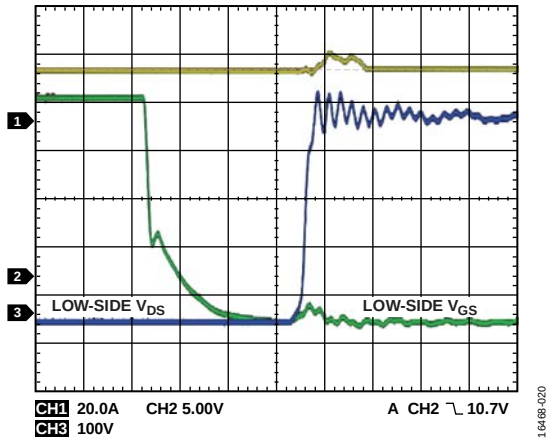

Figure 21. V_{HV} = 400 V, f_{SW} = 50 kHz, Output Current (I_{OUT}) = 27.1 A, Turn Off

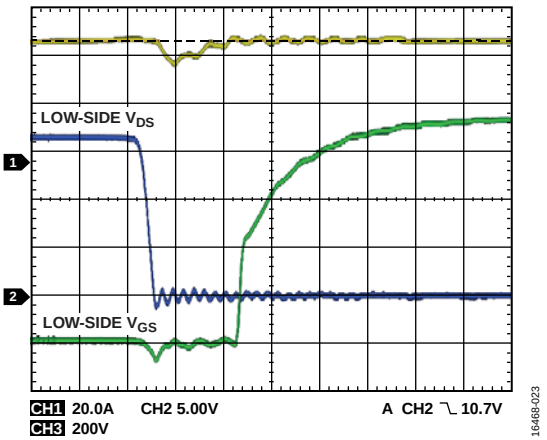

Figure 22. V_{HV} = 600 V, f_{SW} = 50 kHz, Output Current (I_{OUT}) = 40.5 A Pulse-Width Modulation (PWM) Delay, Turn On

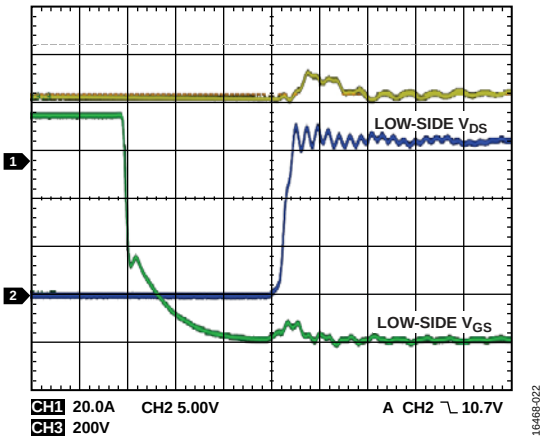

Figure 23. V_{HV} = 600 V, f_{SW} = 50 kHz, Output Current (I_{OUT}) = 40.5 A, Turn Off

PWM DELAY

The ADuM4135 input and output PWM measures the delay between the two signals. The measures have been made directly on the input and output pins of the ADuM4135. The delay is to 59.4 ns.

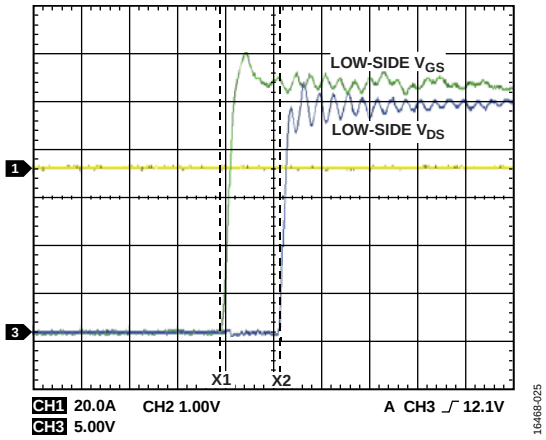

Figure 24. Delay Between Input and Output PWM, Turn On

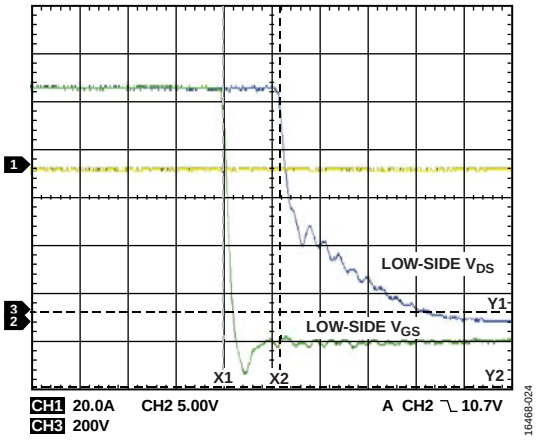

Figure 25. Delay Between Input and Output PWM, Turn Off

SCHEMATIC

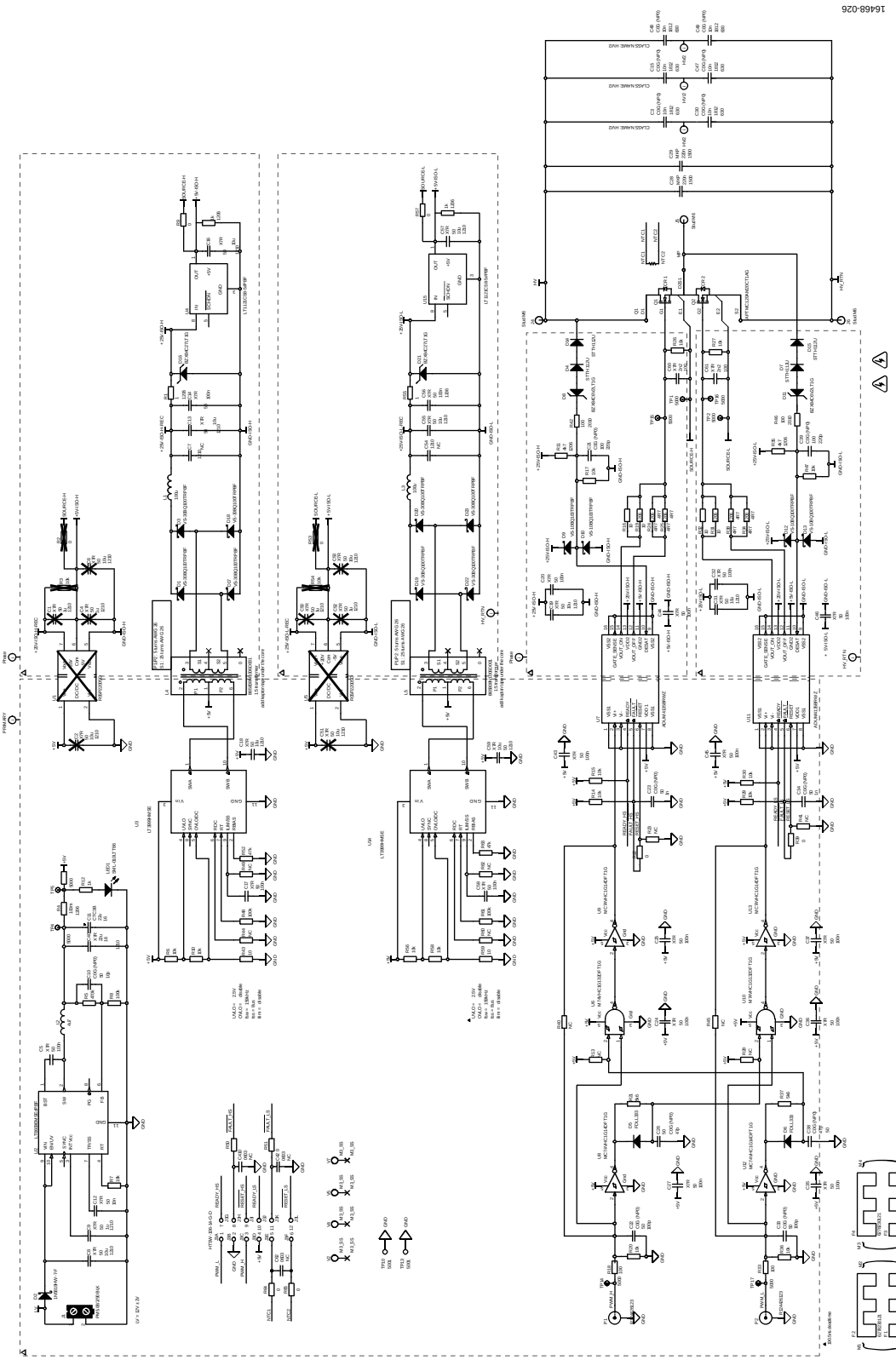

Figure 26. ADuM4135 Gate Drive Board Schematic

CONCLUSION

The ADuM4135 gate driver has the current drive capability, the correct power supply range, and a strong CMTI capability of >100 kV/µs to deliver clean performance when driving SiC MOSFETs.

The test results provide data showing a solution is available for isolated power supply, high voltage gate drivers driving SiC.