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Evaluating the ADuM4138 *i*Coupler, High-Voltage Isolated IGBT Gate Driver with Isolated Flyback Controller

FEATURES

- 6 A peak drive output capability
- Output power device resistance <1 Ω
- Test infrastructure for
  - SPI communication
  - Miller clamp
  - Desaturation detection
  - Two overcurrent protection pins
  - Two temperature sensor pins
  - Fault reporting
  - Two dummy loads

EVALUATION KIT CONTENTS

EVAL-ADuM4138EBZ evaluation board

ADDITIONAL HARDWARE REQUIRED

Variable power supply up to 20 V and up to 1 A
USB-SDP-CABLEZ required for SPI communication

SUPPORTED *i*COUPLER MODELS

ADuM4138

GENERAL DESCRIPTION

The EVAL-ADuM4138EBZ evaluation board demonstrates the advanced features of the ADuM4138 while maintaining flexibility in a testing environment. The EVAL-ADuM4138EBZ evaluation board layout delivers a circuit that is easy to manipulate via jumper pins. A more optimized layout is possible, which increases the performance of the system as a whole.

The evaluation board works with the USB-SDP-CABLEZ programming cable to access the secondary side electronically erasable programmable read-only memory (EEPROM), and also includes the option to drive the serial peripheral interface (SPI) bus with any other SPI compatible system. The USB-SDP-CABLEZ operates with a 3.3 V logic supply, while the ADuM4138 has an internal 5 V regulator. To allow for interfacing, a resistor divider on the MISO line is included in R21 and R22.

This user guide demonstrates how to use the included ADuM4138 evaluation software for accessing the user trim bits. This user guide shows how to simulate EEPROM settings, as well as program bits into nonvolatile memory.

EVALUATION BOARD PHOTOGRAPH

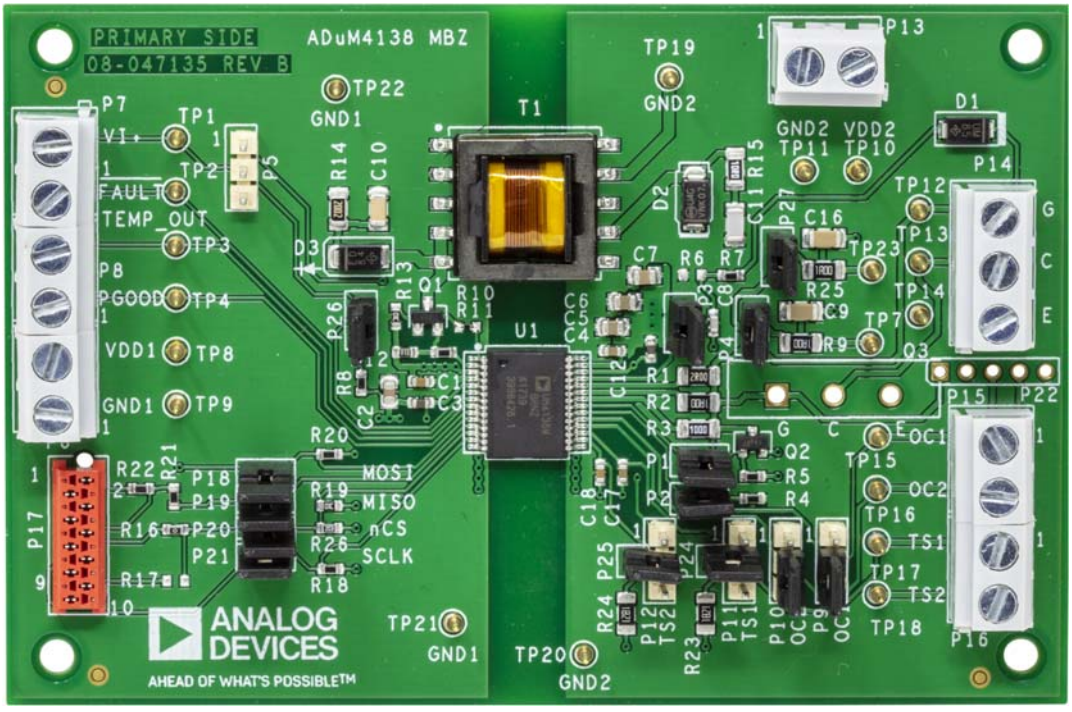

Figure 1. EVAL-ADuM4138EBZ Evaluation Board

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REVISION HISTORY

12/2018—Revision 0: Initial Version

SETTING UP THE EVALUATION BOARD

The EVAL-ADuM4138EBZ evaluation board comes ready to display VI+ to gate operation.

LOAD

In the stock configuration, two parallel resistor capacitor (RC) loads, a 1 Ω resistor (R9 or R25) in series with a 100 nF capacitor (C9 or C16) can be jumped in via Jumper P4 and/or Jumper P27.

Figure 2. Simulated IGBT Gate Loads

Removing the P4 and P27 jumpers removes the RC load. Screw terminals and TO-264 through-holes are provided on the evaluation board as methods to connect other loads to the ADuM4138. TP7 and TP23 provide test points to show the simulated internal gate connection within an insulated gate bipolar transistor (IGBT) module that has an integrated 1 Ω series gate resistor. By jumping P4 or P27, a single RC load can remain.

POWER CONNECTIONS

In the stock configuration, the only power connections required are the V_{DD1} pin and the GND_1 pin on the ADuM4138. Voltages between 6 V and 25 V are recommended for testing. DC current limits of approximately 1 A are also recommended for up to 20 kHz operation, although lower current limits are acceptable.

INPUT/OUTPUT CONNECTIONS

The VI+ pin can be driven with any 5 V logic or 3.3 V logic push pull complementary metal-oxide semiconductor (CMOS) connection or with an adequate open-drain configuration if the correct pull-up resistor is used. It is recommended to drive the VI+ pin with a 50 Ω load capable source. If a jumper is in P26, the 50 Ω load is connected. (Note that the EVAL-ADuM4138EBZ comes configured with a jumper installed in P26.) R8 is a 0603 surface mount device (SMD) resistor that allows 50 Ω termination.

If a 50 Ω termination is not used, do not allow the VI+ pin to be driven by a high-Z signal. When not driven, the VI+ pin can be brought to a safe state by jumping Pin 2 and Pin 3 of Jumper P5, which shorts VI+ to GND_1. If no 50 Ω termination is used, VI+ can be driven high by jumping Pin 1 and Pin 2 of Jumper P5. Do not jump Pin 1 and Pin 2 of P5 if the P26 jumper is set to have the 50 Ω termination load present. This configuration sinks the V5 low dropout (LDO) regulator on the primary side.

USING SPI

The ADuM4138 evaluation board interfaces easily with the USB-SDP-CABLEZ cable. When using the SPI bus, place jumpers on P18, P19, P20, and P21. Connect the USB-SDP-CABLEZ to P17. The evaluation board has an indexing hole to ensure proper polarity. If the USB-SDP-CABLEZ system is to be used for SPI communication, refer to the Software Installation Procedure section for more information.

Alternately, any other SPI system can be tested on the evaluation board by connecting cables to the right side of the P18, P19, P20, and P21 jumpers. The pins of the evaluation board are labeled on the silkscreen.

When programming, it is recommended to have Pin 2 and Pin 3 of Jumper P5 shorted to prevent the VI+ pin from affecting the transfer of the gate drive signal. This configuration shorts VI+ to GND_1.

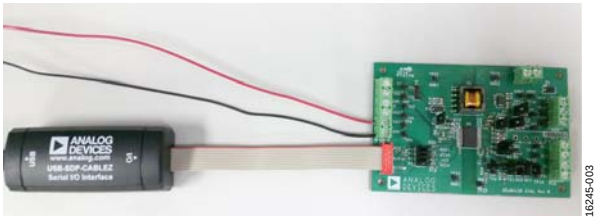

Figure 3. EVAL-ADuM4138EBZ with USB-SDP-CABLEZ Connected

STOCK CONFIGURATION FAULT OVERIDES

To present the EVAL-ADuM4138EBZ evaluation board with a simplified test platform, the evaluation board comes configured with fault mode overrides that normally do not exist in the application. These overrides can be removed to evaluate the fault modes, or the user can leave the overrides on the evaluation board to disable the fault condition and focus on other parts of the IC.

Desaturation Fault Override

Jumping P3 shorts the desaturation detection blanking capacitor (C8) to the GND_2 pin, which blocks the desaturation fault from being detected. Removing the jumper on P3 allows the C8 capacitor to be charged via the precision internal 500 µA current source if an active IGBT is not connected to the collector pins on the evaluation board. This configuration causes a desaturation fault approximately 6 µs after the rising edge of an input signal on the VI+ pin.

Overcurrent Fault Overrides

P9 and P10 provide a way to connect the OC1 pin and the OC2 pin either high or low. The default configuration is to tie the overcurrent pins low by connecting Pin 2 and Pin 3 of Jumper P9 and/or Jumper P10. This connects OC1 to GND_1 and OC2 to GND_2. If the user want to force an overcurrent fault, connect Pin 1 and Pin 2 of either P9 or P10 to force the overcurrent fault to be read as soon as possible. This method is a simplified approach to seeing the overcurrent blanking time as set by the EEPROM registers.

Temperature Sense Fault Override

Without remote temperature sensing resistors in place, the TS1 and TS2 pins float high, which produces a low temperature operation mode. To create a middle range voltage on the temperature sense pins, place an approximately 1.8 kΩ resistor on R23 or R24. These resistors can be removed by jumping P12 and P13 to different pin configurations, or the TS1 and TS2 pins can be fed by a voltage source. Jumper P11 and Jumper P12 are provided to allow the user to quickly tie Pin TS1 or Pin TS2 high or low, effectively railing these pins to make the ADuM4138 sense that the temperature sensor is experiencing a low or high temperature. A third option is to connect to the 1.8 kΩ resistors to obtain a midrange temperature simulation, as shown in Figure 6.

Figure 4. TS1 and TS2 Pins Jumped High (Low Temperature Simulation)

Figure 5. TS1 and TS2 Pins Jumped Low (High Temperature Simulation)

Figure 6. Midrange Temperature Sense Jumper Configuration

MILLER CLAMP ACTIVATION OR DEACTIVATION

In the stock configuration, P2 is jumpered. In this configuration, the Miller clamp is able to be operated. Removing the P2 jumper removes the pull-up resistor from the gate of the external Miller clamp metal-oxide semiconductor field effect transistor (MOSFET), which sends a low signal to the Miller clamp constantly, because the MILLER_OUT pin is open-drain.

GATE_SENSE PIN

The P1 jumper allows access to connect and disconnect the GATE_SENSE pin for manipulation testing. The left side of this pin is connected directly to the IC and the right side is connected to the available sensing node of an IGBT module. It is recommended always to leave the P1 jumper connected, unless a specific test is required, for example, testing the Miller clamp activation voltage.

EXAMPLE PROPAGATION DELAY TESTING

From a stock configuration, an example propagation delay testing can be performed. Figure 7 shows one possible configuration. The VI+ pin is driven via a 5 V push-pull CMOS driver referenced to GND_1. Pin V_{DD1} is fed with 12 V referenced to GND_1. The E screw terminal is the emitter connection of the secondary side, which is also the GND_2 pin. For this configuration, it is recommended to remove the USB-SDP-CABLEZ, as well as the P18, P19, P20, and P21 jumpers. If an SPI transmission occurs when the VI+ pin is brought high, the output is blocked. It is possible to perform a test with the USB-SDP-CABLEZ connected to the ADuM4138.

Measuring Test Point TP7 and/or Test Point TP23 simulates what an IGBT with a 1 Ω internal series gate resistance sees at its gate.

Adding or removing the P2 jumper affects the rising edge propagation delay, because the ADuM4138 senses when it is safe to turn on the main V_{OUT_ON} driver, based on the Miller MOSFET gate voltage. Do not allow the VI+ pin to be driven by a high-Z signal, which can happen on some function generator models when the output off button is pressed. If the function generator being used has a high-Z when turned off, it is recommended to leave P26 jumpered by placing a 50 Ω terminating resistor, R8, between VI+ and GND_1.

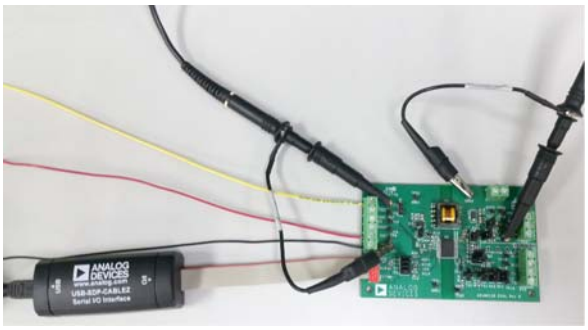

Figure 7. Example Propagation Delay Test Setup

REGISTER DESCRIPTIONS

USER TRIM REGISTER

Table 1. Address 00—User Trim Register Map

Field	Bits	Description
OFFSET_2[5:0]	[23:18]	TS2 offset
GAIN_2[5:0]	[17:12]	TS2 gain
OFFSET_1[5:0]	[11:6]	TS1 offset
GAIN_1[5:0]	[5:0]	TS1 gain

OFFSET_2[5:0]

Internal offset for the Temperature Sense Point 2, TS2, can be adjusted with the OFFSET_2 field of the EEPROM. There are 6 bits of resolution available.

GAIN_2[5:0]

Internal gain for TS2 can be adjusted with the GAIN_2 field of the EEPROM. 6 bits of resolution are available.

OFFSET_1[5:0]

Internal offset for TS1 can be adjusted with the OFFSET_1 field of the EEPROM. There are 6 bits of resolution available.

GAIN_1[5:0]

Internal gain for TS1 can be adjusted with the GAIN_1 field of the EEPROM. 6 bits of resolution are available.

CONFIGURATION TRIM REGISTER

Table 2. Address 01—Configuration Trim Register Map

Field	Bits	Description
Reserved	[23:17]	Reserved
OT_Fault_OP	16	Overtemperature fault disable
OT_fault_Sel	15	Overtemperature fault select
OC_TIME_OP	14	Disable two-level drive and timer during overcurrent event
OC_2Lev_OP	13	Overcurrent two-level operation select
Low_T_OP	12	Low temperature operation select
OC_Blank_OP	11	Overcurrent blanking operation select
tblank	[10:7]	Overcurrent blanking time
ECC_OFF_OP	6	Enable soft shutdown with error correcting code (ECC) fault
Flyback_V	[5:2]	Flyback output voltage setting
T_ramp_OP	1	Overcurrent temperature ramp enable
PWM_OSC	0	Temperature reading output oscillator select

OT_Fault_OP

Set OT_Fault_OP to 1 to disable a fault for over temperature. If set to 0, the ADuM4138 issues a fault if the TS1 pin detects an overtemperature event.

OT_Fault_Sel

OT_Fault_Sel selects between two overtemperature fault voltage thresholds. Selecting 0 sets the falling threshold to 1.64 V (typical) and the rising threshold to 1.68 V (typical). Setting the OT_Fault_SELF bit to 1 sets the falling threshold to 1.68 V (typical) and the rising threshold to 1.72 V (typical).

OC_TIME_OP

Set OC_TIME_OP to 1 to disable two-level drive and timer during an overcurrent event. During an overcurrent event, the output enters soft shutdown immediately. Blanking is still available.

OC_2Lev_OP

Set OC_2Lev_OP to 1 to disable two-level drive during an overcurrent event before a fault is registered. After the overcurrent detection time is complete, a fault is registered, and the output shuts down using the soft shutdown. If set to 0 during an overcurrent event, but before td_OC, the two-level drive level is output to the gate.

Low_T_OP

A special low temperature operation can be disabled in Bit 12 of the configuration trim register. If Low_T_OP is set to 0, when the sensed IGBT temperature is below −20°C, the gate voltage rises to the two level plateau voltage during an on command. Hysteresis allows for operation up to −20°C before the low temperature operation mode is left. If Low_T_OP is set to 1, all nonfault gate signals are at the VDD2 output voltage on an on signal.

OC_Blank_OP

Set OC_Blank_OP to 1 to enable two-level drive during current blanking time. If OC_Blank_OP is set to 1, two-level drive is entered in the case of an overcurrent event during the tblank blanking time.

tblank[3:0]

During the initial turn on of a gate, there can exist a large amount of noise caused by switching actions. To account for this, the overcurrent detection can be masked by setting different tblank values. During the masking time, overcurrent events are ignored.

Table 3. td_OC Blanking Times

tblank[10:7]	Blanking time (µs)
0000	0
0001	0.4
0010	0.6
0011	0.8
0100	1.0
0101	1.2
0110	1.6
0111	2.0
1000	2.4
1001	2.8
1010	3.2
1011	3.6
1100	4.0
1101	4.4
1110	4.8
1111	6.0

ECC_OFF_OP

If set to 1, when an ECC error is detected, the device enters a soft shutdown, and a fault is registered. This fault is registered whether a single or double ECC fault is detected. If set to 0, ECC faults are still set in the control register (Address 10), but the part continues to operate without shutting down.

Flyback_V[3:0]

The isolated flyback output voltage can be set by the Flyback_V bits in the EEPROM. The default code is 0111 (16.00 V target). Table 4 shows the available output voltages.

Table 4. EEPROM Register Map

Flyback_V[5:2]	VDD2 Voltage Setting (V)
0000	14.25
0001	14.50
0010	14.75
0011	15.00
0100	15.25
0101	15.50
0110	15.75
0111 (Default)	16.00
1000	16.25
1001	16.50
1010	16.75
1011	17.00
1100	17.25
1101	17.50
1110	17.75
1111	20.00

T_Ramp_OP

Set to 0 to allow the over current reference voltage to vary with temperature. The current reference varies by 10% across −40°C to +175°C. Set to 1 to have the overcurrent reference voltage set to 2 V (typical) regardless of sensed temperature.

PWM_OSC

The PWM_OSC bit controls whether the reported TEMP_OUT pin pulse-width modulation (PWM) frequency is 10 kHz or 50 kHz. When PWM_OSC is set to 0, the output frequency is 10 kHz (typical). When PWM_OSC is set to 1, the PWM output frequency is 50 kHz (typical).

CONTROL REGISTER

Table 5. Address 10—Control Register Map

Field	Bits	Description
Reserved	23:6	Reserved
ECC2_DBL_ERR	5	ECC Bank 2 double error detected
ECC2_SNG_ERR	4	ECC Bank 2 single error detected
ECC1_DBL_ERR	3	ECC Bank 1 double error detected
ECC1_SNG_ERR	2	ECC Bank 1 single error detected
Prog_Busy	1	Program/busy bit
Sim_Trim	0	Simulate trim

ECC2_DBL_ERR

If two errors are detected in the EEPROM stored data, the ECC2_DBL_ERR bit is set to 1 when read. Two errors are detectable, but uncorrectable using the ECC employed by the ADuM4138. ECC2_DBL_ERR shows that a double error is detected in the memory banks representing trim performed on the parts outside of registers affected by the user trim address and the configuration trim address. A value of 0 means no error is detected.

ECC2_SNG_ERR

If a single error is detected in the EEPROM stored data, the ECC2_SNG_ERR bit is set to 1 when read. A single error can be detected and corrected using the ECC employed by the ADuM4138. ECC2_SNG_ERR shows that a single error is detected in the memory banks representing trim performed on the parts outside of registers affected by the user trim address and the configuration trim address. A value of 0 means no error is detected.

ECC1_DBL_ERR

If two errors are detected in the EEPROM stored data, the ECC1_DBL_ERR bit is set to 1 when read. Two errors are detectable, but uncorrectable using the ECC employed by the ADuM4138. ECC1_DBL_ERR shows that a double error is detected in the memory banks representing trim performed on the parts by the user trim address and the configuration trim address. A value of 0 means no error is detected.

ECC1_SNG_ERR

If a single error is detected in the EEPROM stored data, the ECC1_SNG_ERR bit is set to 1 when read. A single error can be detected and corrected using the error correcting code employed by the ADuM4138. ECC1_SNG_ERR shows that a single error is detected in the memory banks representing trim performed on the parts by the user trim address and the configuration trim address. A value of 0 means no error is detected.

Prog_Busy

Set this bit high in order to program the EEPROM memory. When this bit is set to 1, the EEPROM begins to write to memory. The hardware sets this bit back to 0 to indicate that programming has occurred. The write sequence takes a maximum of 40 ms (maximum) to perform, but may write faster than 40 ms (maximum). If shorter wait times are desired, the Prog_Busy bit can be read back multiple times during the writing time. If a 0 is read back after the user sets the bit to 1, the writing is complete.

Sim_Trim

If Sim_Trim is set to 0, the user trim and configuration trim registers have no effect. Use this bit to simulate trim settings without writing to the registers.

EVALUATION SOFTWARE DESCRIPTION

EVALUATION SOFTWARE SCREENSHOT

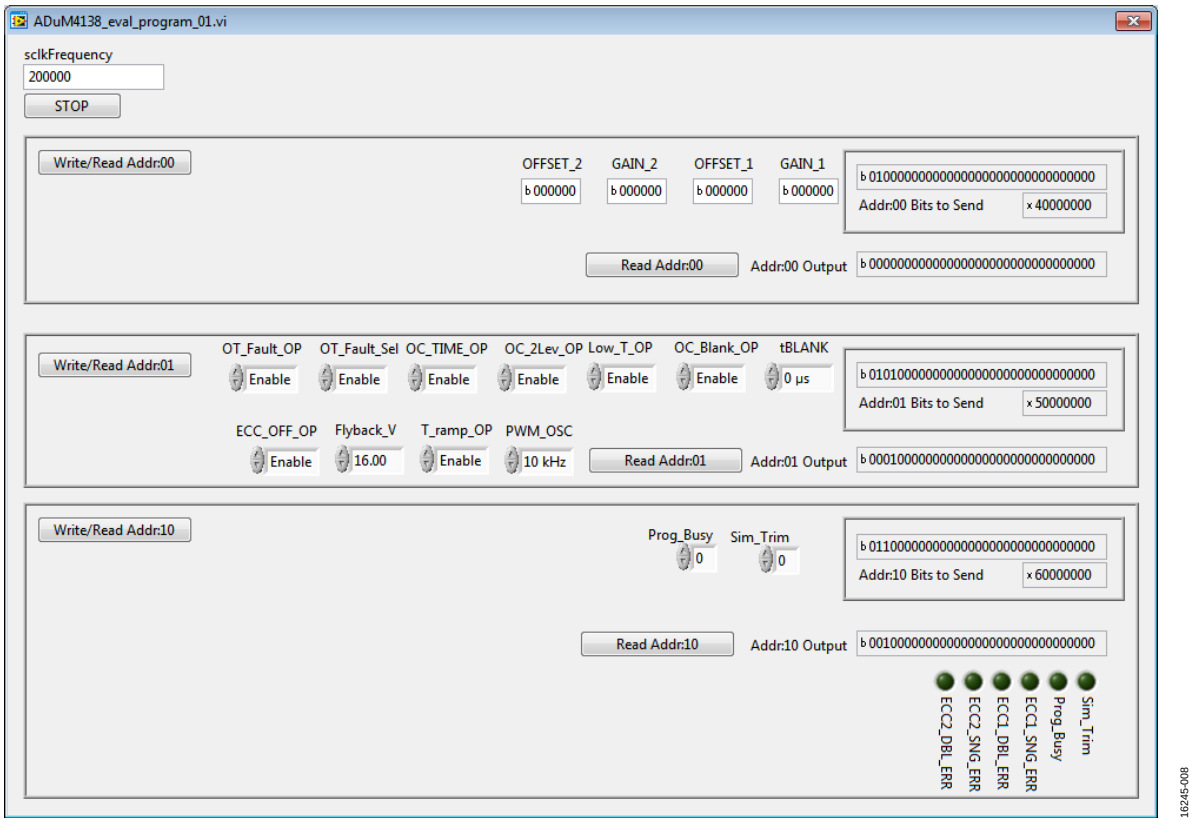

Figure 8. Evaluation Software Screenshot

SOFTWARE INSTALLATION PROCEDURE

To use the USB-SDP-CABLEZ for SPI communication, a LabVIEW executable is available. The LabVIEW executable requires that the USB-SDP-CABLEZ drivers be installed, and that a LabVIEW runtime engine compatible with LabVIEW 2011 is available.

1. Install **SDPdrivers.exe** (available from Analog Devices).
2. Install LabVIEW Runtime Engine 2011 or later (available from National Instruments).
3. Double-click A**DuM4138_eval_progam_01.exe** to run.

STOP

Click **STOP** to halt the LabVIEW program. Alternate methods of stopping the program are to close the window, or force quit the program. All of these options set the $\overline{CS}$ pin to an unknown state, so it is recommended to remove the USB-SDP-CABLEZ connection from the evaluation board before shutting the program down.

Read Addr:00

Click **Read Addr:00** to see what the ADuM4138 has in the EEPROM at Address 00 (user trim bits). Clicking **Read Addr:00** sends two read commands. This is because of the way that the SPI setup operates. The second read command pushes the data loaded by the first read command to the MISO pin. The result of the second read appears in the **Addr:00 Output** field.

Read Addr:01

Click **Read Addr:01** to see what the ADuM4138 has in the EEPROM at Address 01 (configuration trim bits). Clicking **Read Addr:01** sends two read commands. This is because of the way that the SPI setup operates. The second read command pushes the data loaded by the first read command to the MISO pin. The result of the second read appears in the **Addr:01 Output** field.

Read Addr:10

Click **Read Addr:10** to see what the ADuM4138 has in the EEPROM at Address 10 (control bits). Clicking **Read Addr:10** sends two read commands. This is because of the way that the SPI setup operates. The second read command pushes the data loaded by the first read command to the MISO pin. The result of the second read appears in the **Addr:10 Output** field.

Write/Read Addr:00

Click **Write/Read Addr:00** to perform a single write comprised of the bit pattern set by the user in the **OFFSET_2** field, the **GAIN_2** field, the **OFFSET_1** field, and the **GAIN_1** field. After the single write, a single read is performed, allowing the user to verify that the sequence is sent. The result of this read is

sent to the **Addr:00 Output** field. If the Sim_Trim bit at Address 10 is set to 1, the write affects the operation of the ADuM4138 with the new settings written by the user. The Sim_Trim bit is set to 0 until the device is powered down, or until new settings are written.

Write/Read Addr:01

Click **Write/Read Addr:01** to perform a single write comprised of the bit pattern set by the user in the **OC_2Lev_OP** field, the **Low_T_OP** field, the **OC_Blank_OP** field, the **td_OC** field, the **Flyback_V** field, the **T_ramp_OP** field, and the **PWM_OSC** field. After the single write, a single read is performed, allowing the user to verify that the sequence is sent. The result of this read is sent to the **Addr:01 Output** field. If the Sim_Trim bit at Address 10 is set to 1, the write affects the operation of the ADuM4138 with the new settings written by the user. The Sim_Trim bit is set to 0 until the device is powered down, or until new settings are written.

Write/Read Addr:10

Click **Write/Read Addr:10** to perform a single write comprised of the bit pattern set by the user in the **Prog Busy** field and the **Sim Trim** field. After the single write, a single read is performed, allowing the user to verify that the sequence is sent. The result of this read is sent to the **Addr:10 Output** field. If Sim_Trim is set to 1, and then Prog_Busy is set to 1, values written to the ADuM4138 using **Write/Read Addr:00** and **Write/Read Addr:01** are written to EEPROM and are loaded on the next power up. These can be verified with an address read after a power up.

sclkFrequency

This field is used to change the operating frequency of the SPI clocking. The field is set in hertz, and 200 kHz is the default and maximum value.

EVALUATION SOFTWARE EXAMPLE OPERATION

These examples assume that the setup described in the Setting Up the Evaluation Board section is used.

WHEN ADUM4138 IS NOT COMMUNICATING

If the ADuM4138 is not powered, and the USB-SDP-CABLEZ is plugged into the evaluation board, read commands usually report all 0s. By reading all registers, it is possible to see if the ADuM4138 is communicating properly, as the address bits are displayed on a read command. Additionally, with default settings, the Flyback_V setting is 111 (see Figure 9).

EXAMPLE READ COMMANDS

To perform a read command, first power up the ADuM4138. Then click the read button of the desired address to be read. If the ADuM4138 EEPROM has never been programmed, it is expected that all 0s except the address are returned, and a Flyback_V setting of 111 in default configuration. Figure 10 shows **Read Addr:00**, **Read Addr:01**, and **Read Addr:10** clicked on a new ADuM4138.

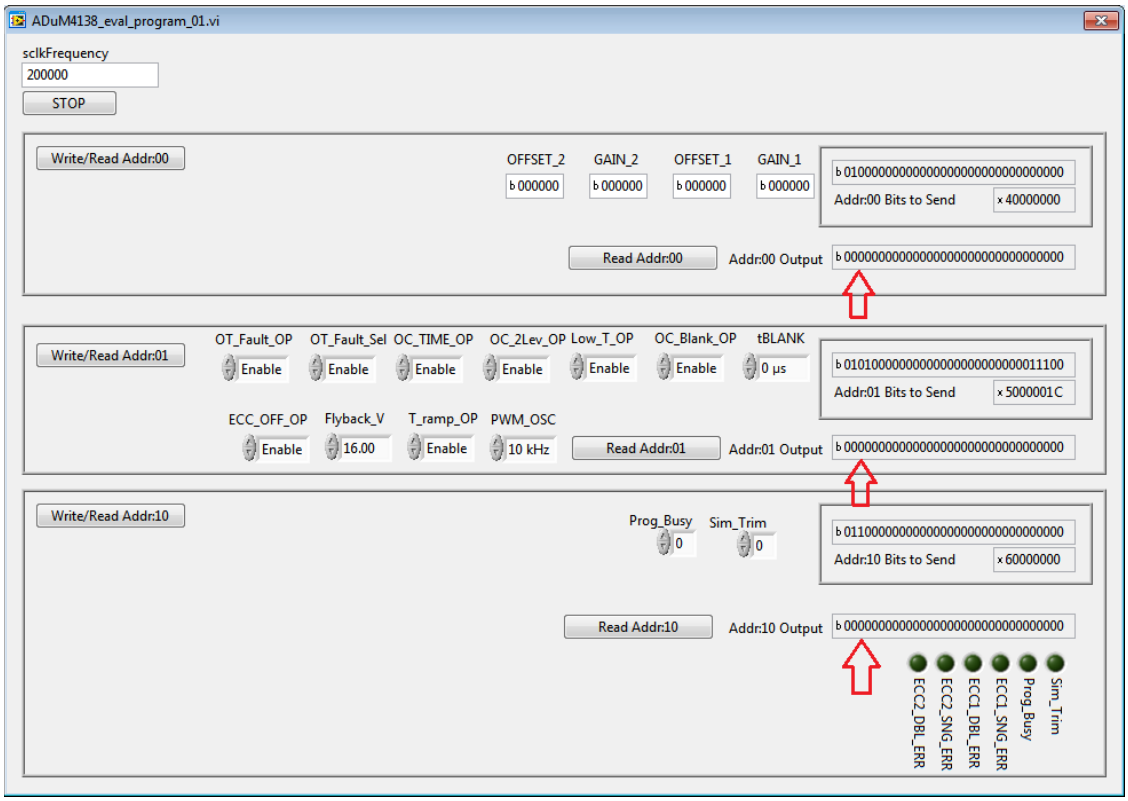

Figure 9. All Zeros Show Communication is Not Occurring

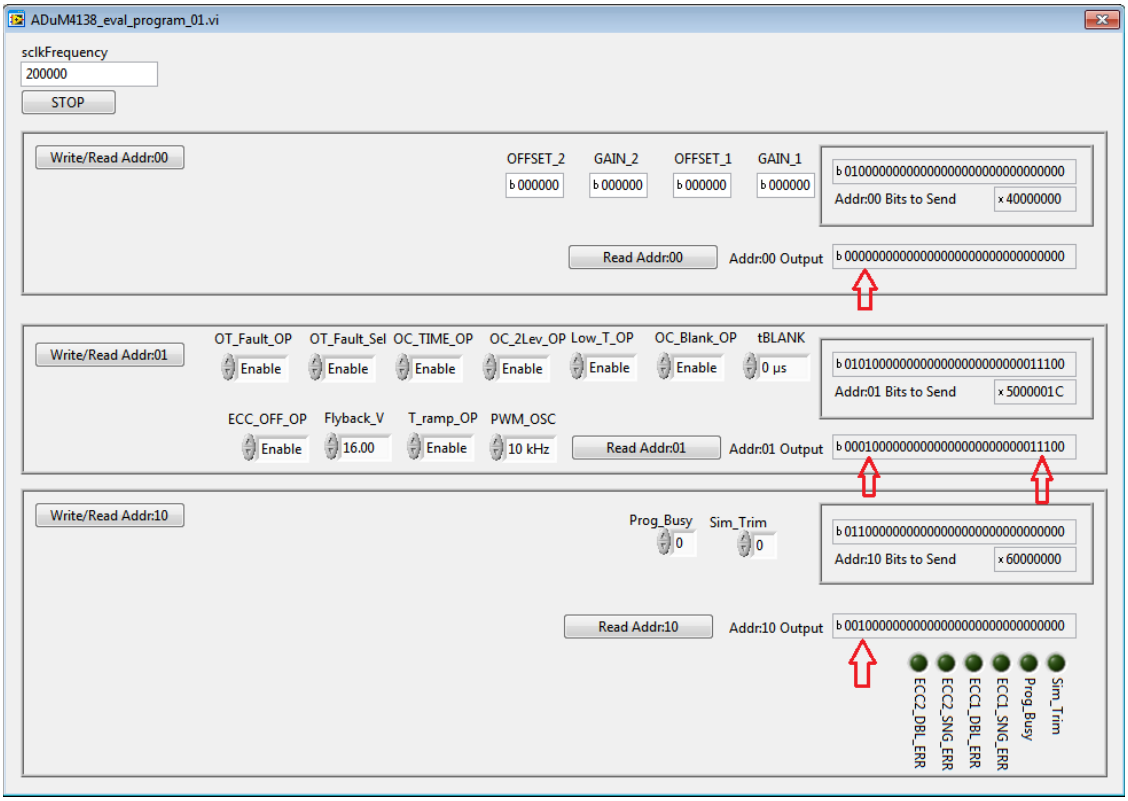

Figure 10. Address Bits Are Being Read Back

EXAMPLE EEPROM WRITE

To write data to the EEPROM, the Sim_Trim bit must first be set. Set this bit by selecting 1 in the **Sim Trim** field, and clicking **Write/Read Addr:10**. This setting results in the **Sim_Trim** green indicator lighting up (see Figure 11).

When the Sim_Trim bit is set to 1, write commands to Address 00 or Address 01 affect the operation of the ADuM4138.

The next step to programming the EEPROM is to set the desired bits in Address 00 and Address 01. In this example, Bit 0 of the **GAIN_1** field is set to 1. When it is set to 1, clicking **Write/Read Addr:00** results in the **Addr:00 Output** field showing that the value was written to the register. At this time, the GAIN_1 EEPROM register is not yet programmed. Note that **Sim_Trim** is still 1 (see Figure 12).

To write Address 00 data to EEPROM, set the **Prog Busy** field to 1, and click **Write/Read Addr:10** (see Figure 13).

The write/read button performs a write and then a read as normal. The **Prog_Busy** green indicator is usually lit up. This state is because the read command occurs quickly after the write, and the Prog_Busy bit in the ADuM4138 is 1 while the device is being programmed. Click **Read Addr:10** after this programming, and once the Prog_Busy bit changes to 0, the EEPROM is programmed. The programming takes approximately 10 µs; therefore, a human user generally cannot click the read button fast enough to see a 1 in the **Prog Busy** field the second time, but an automated program might (see Figure 14).

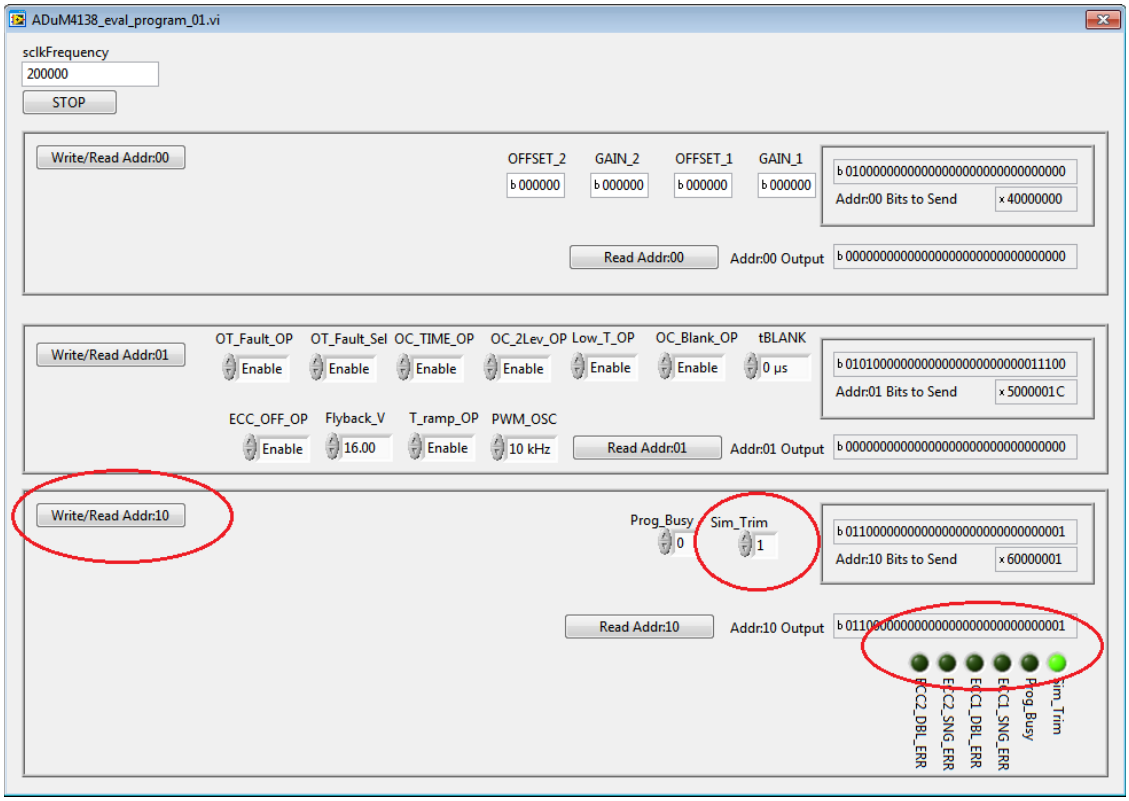

Figure 11. Setting the Sim_Trim Bit

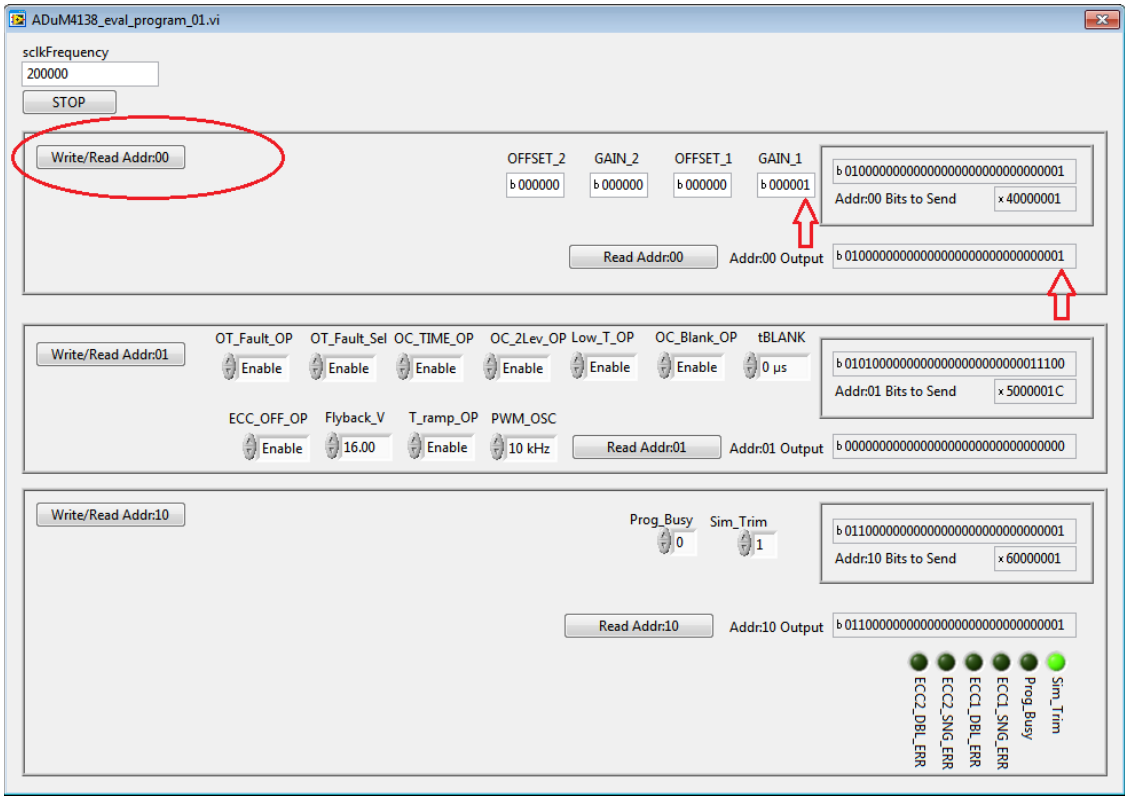

Figure 12. Writing Example Register Edit

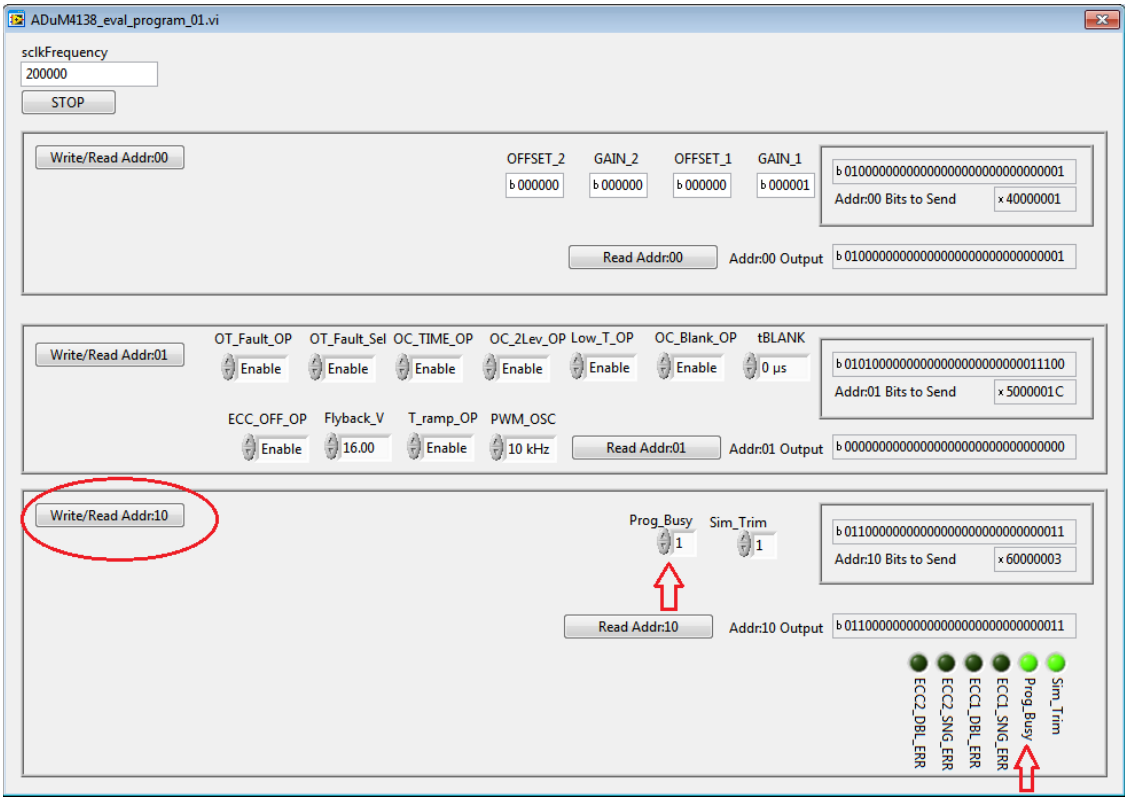

Figure 13. Programming EEPROM

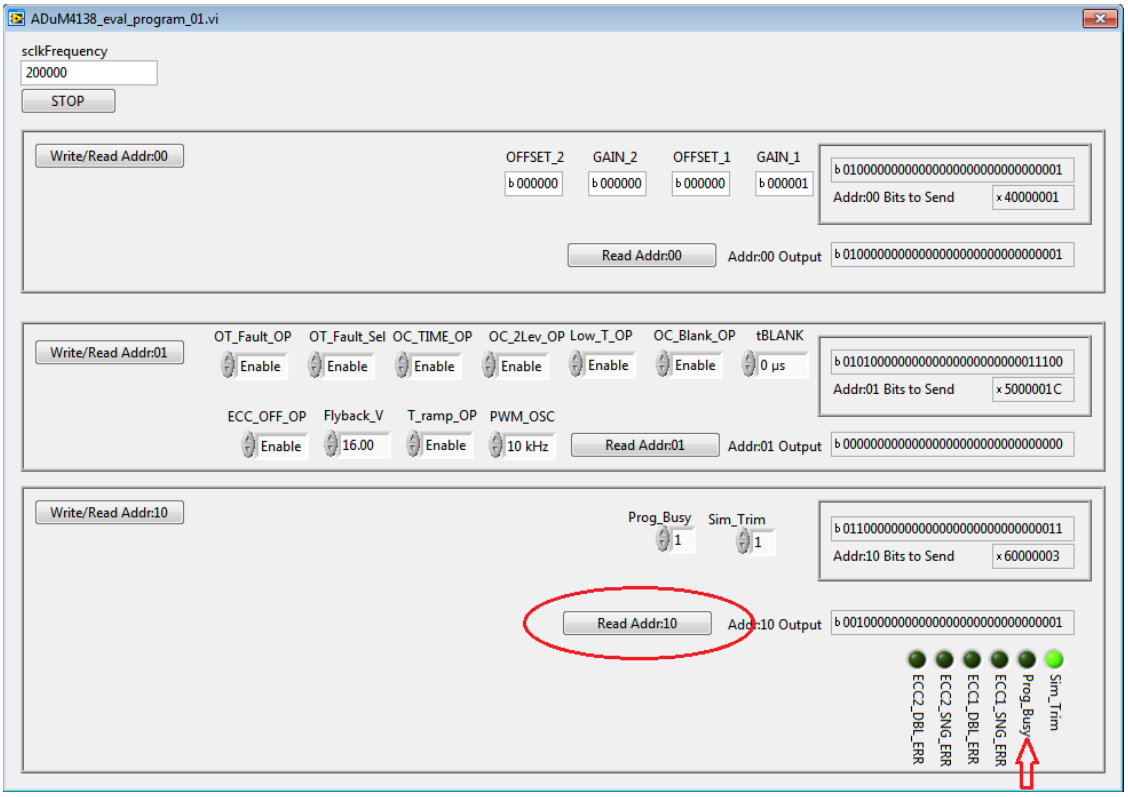

Figure 14. ADuM4138 Showing Programming Complete

After Prog_Busy reads 0, the EEPROM is programmed. Verify this programming by powering down the ADuM4138 and clicking **Read Addr:00**. Expect to receive all 0s back, because the ADuM4138 is unpowered. This read is so that the next read is easier to see. The other read buttons can also be clicked, but it is not necessary. Figure 15 shows all read buttons clicked while the ADuM4138 is off.

Now power up the ADuM4138, and click all the read buttons. It can then be seen that Bit 0 of GAIN_1 survives a power-up, indicating that the EEPROM is programmed. The same steps can be performed with the **GAIN_1** field set to 0 to return the EEPROM to its original programmed state, if desired (see Figure 16).

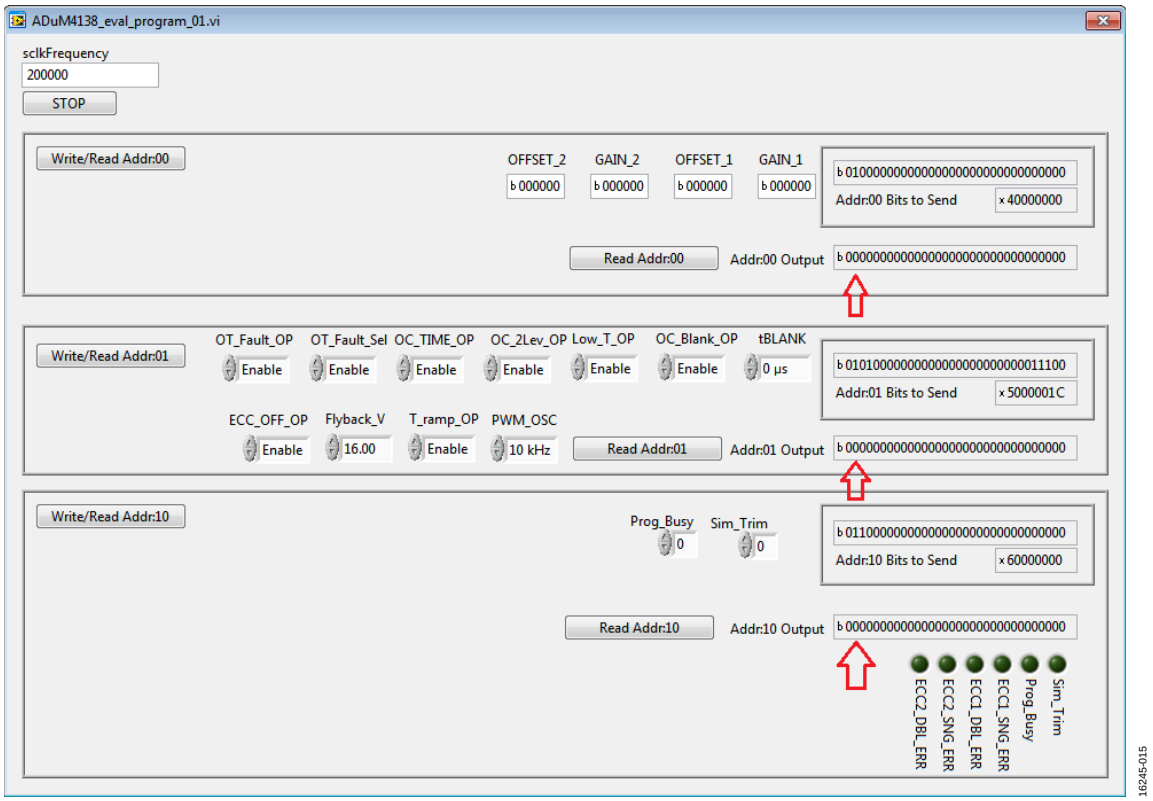

Figure 15. Unpowered Reads

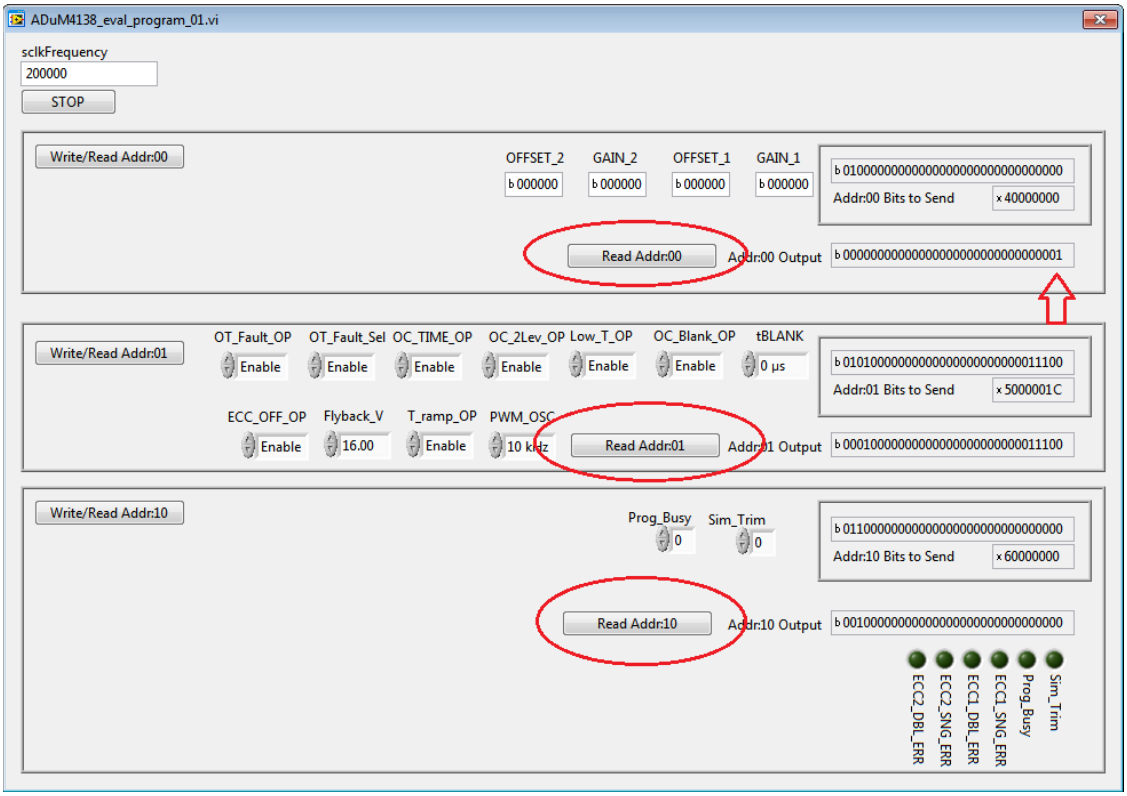

Figure 16. EEPROM Successfully Written

EVALUATION BOARD SCHEMATIC

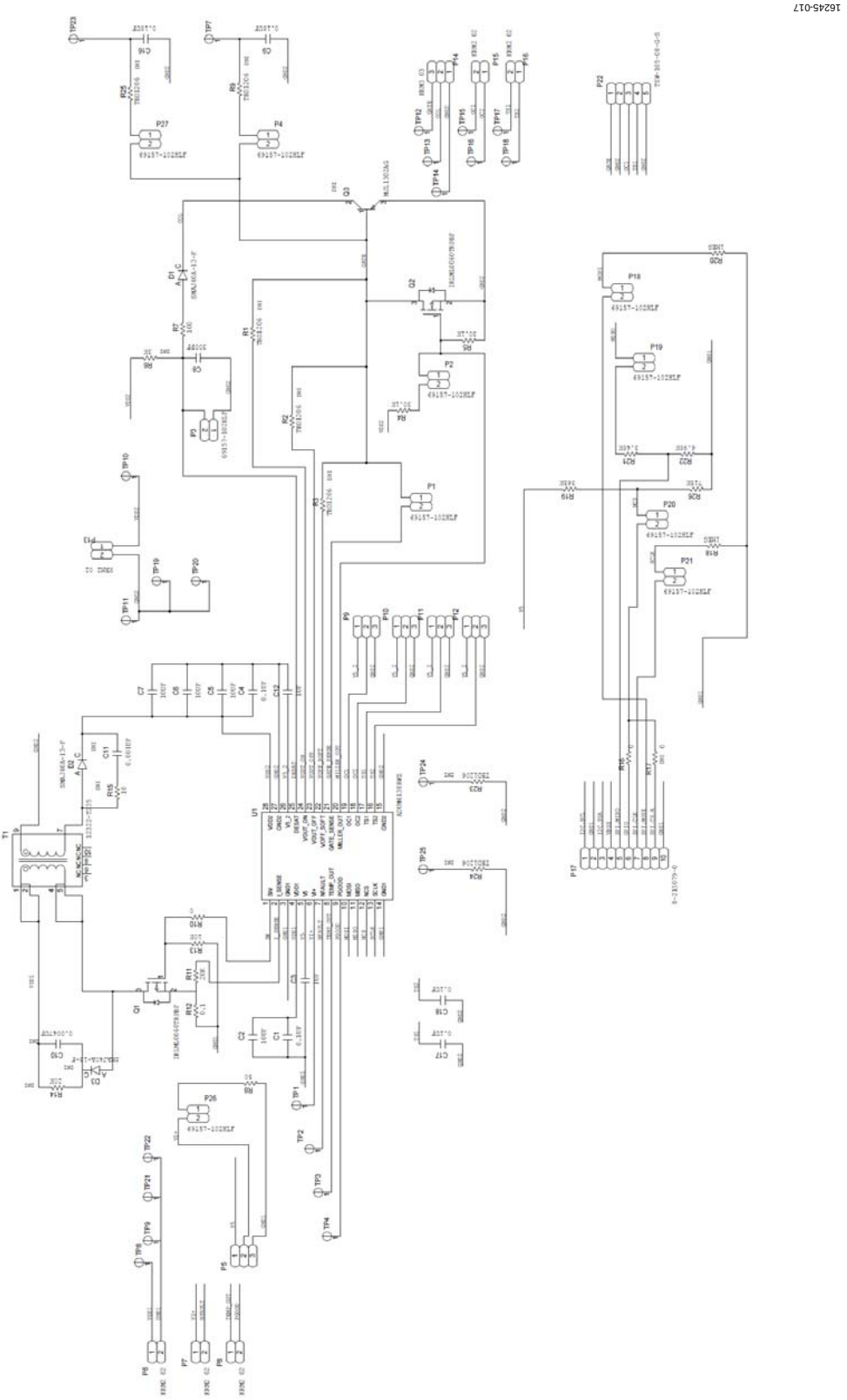

Figure 17. EVAL-ADuM4138EBZ Circuit Schematic

ORDERING INFORMATION

BILL OF MATERIALS

Table 6.

Reference Designator	Description	Part Number	Supplier
C1, C4, C17, C18	0.1 µF ceramic capacitor, 50 V, X7R 0603	GRM188R71H104JA93D	Murata
C10	0.0047 µF ceramic capacitor, 50 V, X7R 1206	CC1206KRX7R9BB472	Yageo
C11	0.001 µF ceramic capacitor, 50 V, NP0 1206	12061A102JAT2A	AVX
C2	10 µF ceramic capacitor, 25 V, X5R 0805	GRM21BR61E106KA73L	Murata
C3, C12	1 µF ceramic capacitor, 25 V, X7R 0603	GRM188R71A105KA61D	Murata
C5, C6, C7	22 µF ceramic capacitor, 25 V, X5R 0805	GRT21BR61E226ME13L	Murata
C8	300 pF ceramic capacitor, 50 V, C0G (NP0) 0603	GRM1885C1H301JA01D	Murata
C9, C16	0.1 µF ceramic capacitor, 25 V, X7R 1206	CC1206KRX7R9BB104	Yageo
D1	Diode, ultrafast rectifier	US1M-E3/61T	Vishay
D2	Diode, SMT ultrafast power rectifier	MURA140T3G	Murata
D3	Diode, ultrafast plastic rectifier, 1 A	ES1D-E3/61T	Vishay
P17	10-pin system demonstration platform (SDP)	8-215079-0	TE Connectivity LTD
P17 (alternate)	WR-MM female connector	690367181072	Wurth Electronics
Q1	Transistor, HEXFET power MOSFET	IRLML0060TRPBF	Infineon
Q2	Transistor, N-channel HEXFET power MOSFET	IRLML2030TRPBF	Infineon
R1	2 Ω resistor, 1206	ERJ-8RQF2R0V	Panasonic
R10	20 Ω resistor, 0603	P0603E20R0BBT	Vishay
R11	20 kΩ resistor, 0603	ERJ-3EKF2002V	Panasonic
R12	0.1 Ω resistor, 0603	ERJ-3RSFR10V	Panasonic
R13, R19	10 kΩ resistor, 0603	ERJ-3EKF1002V	Panasonic
R14	20 kΩ resistor, 1206	ERJ-8ENF2002V	Panasonic
R15	10 Ω resistor, 1206	ERJ-8ENF10R0V	Panasonic
R16	0 Ω resistor, 0603	ERJ-3GEY0R00V	Panasonic
R18, R20	1 MΩ resistor, 0603	ERJ-3EKF1004V	Panasonic
R2, R9, R25	1 Ω resistor, 1206	ERJ-8RQF1R0V	Panasonic
R21	3.48 kΩ resistor, 0603	ERJ-3EKF3481V	Panasonic
R22	6.98 kΩ resistor, 0603	ERJ-3EKF6981V	Panasonic
R23, R24	1.82 kΩ resistor, 1206	RC1206FR-071K82L	Yageo
R26	20 kΩ resistor, 0603	ERJ-3GEYJ203V	Panasonic
R3	100 Ω resistor, 1206	ERJ-8ENF1000V	Panasonic
R4, R5	30.1 kΩ resistor, 0603	ERJ-3EKF3012V	Panasonic
R6, R17	Not installed	Not applicable	Not applicable
R7	100 Ω resistor, 0603	ERJ-3EKF1000V	Panasonic
R8	49.9 Ω resistor, 0603	ERJ-3EKF49R9V	Panasonic
T1	Sumida 13 µH primary 1:2 transformer	12322-T235	Sumida
U1	Isolated IGBT gate driver	ADuM4138BRWZ	Analog Devices, Inc.

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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