ANALOG DEVICES

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DC-DC Optimizer PCB Testing Report

Project Ref #: AND020

TITLE	DOC. NO.	REV.
DC-DC-Optimizer PCB Testing Report	RE-14116	2.0

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REVISION HISTORY

Revision	Description	Date	Author
0.1	Draft	09-24-2018	Y.Wong
1.0	Added additional efficiency tests	03-06-19	G. Fichera
2.0	Added logo and legal disclaimer	06-08-2021	

TABLE OF CONTENTS

1 Purpose

The purpose of this document is to describe the testing report of DC-DC Optimizer PCB for Analog Device Inc. It shall include:

- General Procedure of all input requirements
- Output (i.e. test results) to verify the design
- The results of all verification activities shall meet the stated acceptance criteria as defined in this document

2 Related Documents

2.1 Documents

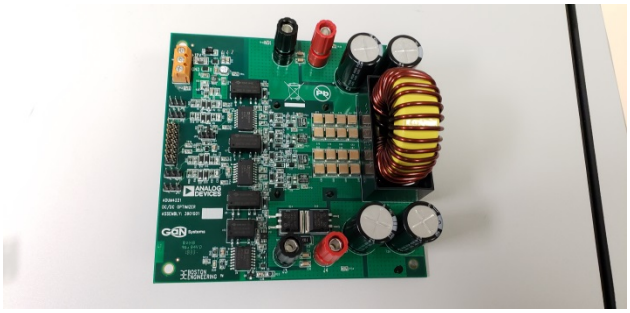
- ADUM4220 DC/DC Power Stage w/ GaN Transistors HW Description V02, Analog Device

3 Test Equipment

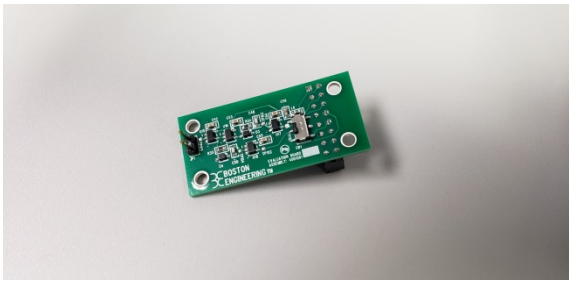
- Digital Multi-Meter Model # FLUKE-87-5 or equivalent
- Tektronix Oscilloscope Model # DPO3034
- 12V Bench Power Supply
- 30V Bench Power Supply 20A
- Equivalent Resistor Load 5ohm, 500W
- Equivalent Resistor Load 1.25ohm, 500W

4 PCB

- DC-DC Optimizer PCB



- Dead Band PCB



5 Testing

5.1 Power Supply Check

Test Setup:

- Connect 12V Power supply and connect to J6 Pin1(+), Pin2(-)
- Turn On Power Supply, verify the fan is operating
- Use DMM to measure and verify following voltage
    - o +3.3V (Between TP14 and TP13)
    - o +6V_S1 (Between TP1 and TP2)
    - o -4V_S1 (Between TP3 and PT2)
    - o +6V_S2 (Between TP4 and TP5)
    - o -4V_S2 (Between TP6 and PT5)
    - o +6V_ISO (Between TP7 and TP8)
    - o -4V_ISO (Between TP9 and PT8)
    - o +5V_ISO (Between TP10 and TP11)
    - o +2.5V_VREF (Between TP12 and PT11)

Test Results

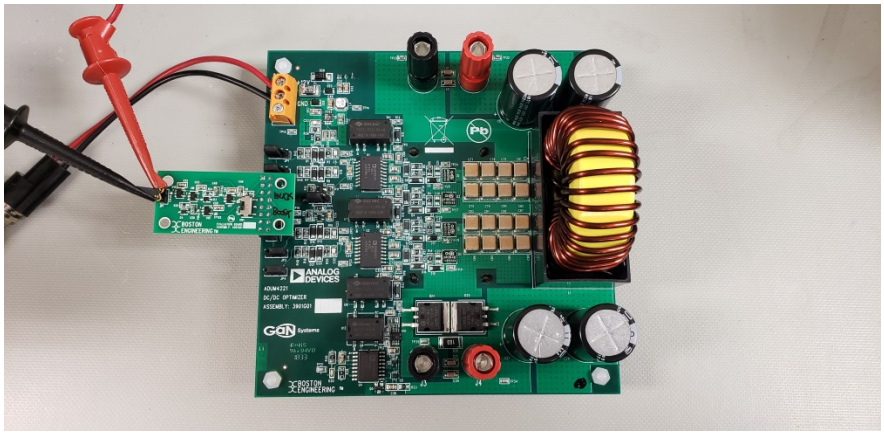
- *Specification Requirements (Pass/Fail Criteria)*

	Unit	Min	Typ	Max	Measurement Results	Pass/ Fail	Comment
+3.3V Supply							
Output voltage	V	3.201	3.300	3.399	**3.332**	☒ ☐	
+6V_S1 Supply							
Output voltage	V	5.8	6.2	6.6	**6.20**	☒ ☐	
-4V_S1 Supply							
Output voltage	V	-4.2	-3.8	-3.4	**-3.65**	☒ ☐	
+6V_S2 Supply							
Output voltage	V	5.8	6.2	6.6	**6.19**	☒ ☐	
-4V_S2 Supply							
Output voltage	V	-4.2	-3.8	-3.4	**-3.65**	☒ ☐	
+6V_ISO Supply							
Output voltage	V	5.8	6.2	6.6	**6.27**	☒ ☐	
-4V_ISO Supply							
Output voltage	V	-4.2	-3.8	-3.4	**-3.57**	☒ ☐	
+5V_ISO Supply							
Output voltage	V	4.75	5.00	5.25	**4.99**	☒ ☐	
+2.5V_VREF							
Output voltage	V	+2.497	2.500	+2.503	**2.502**	☒ ☐	

5.2 DeadBand Timing

Test Setup:

- Connect 12V Power supply and connect to J6 Pin1(+), Pin2(-)
- Connect DeadBand PCB to DC-DC Optimizer PCB connector J5

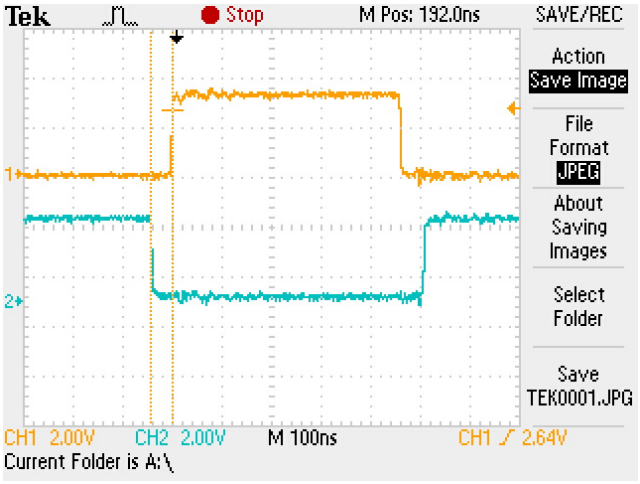


- Connect Function Generator to DeadBand PCB JP1
- Set the frequency to 1.00MHz, Square Wave, 50% duty cycle, 0-3.3V Pulse
- Turn On Power Supply
- Use oscilloscope to probe TP101 and TP102 on DeadBand PCB

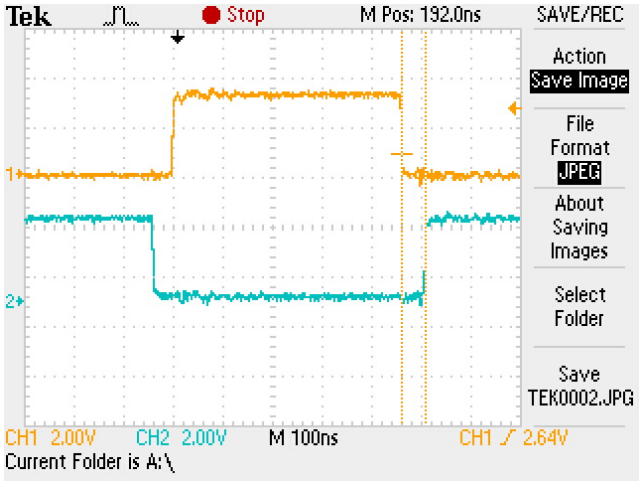
Test Results

Channel 1: TP101

Channel 2: TP102



DeadBand time ~ 40ns



DeadBand time ~ 40ns

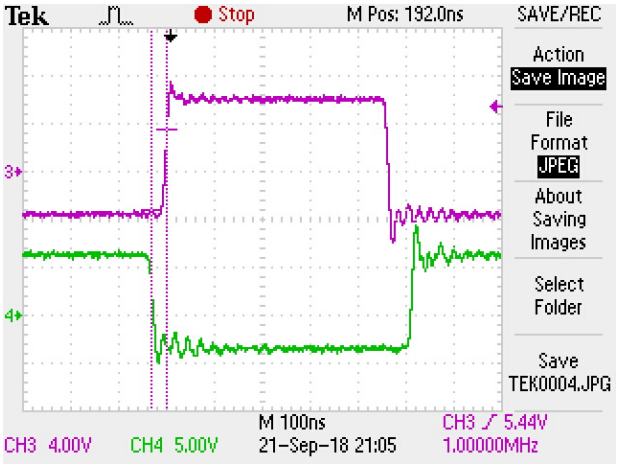
5.3 Driver Signal

Test Setup:

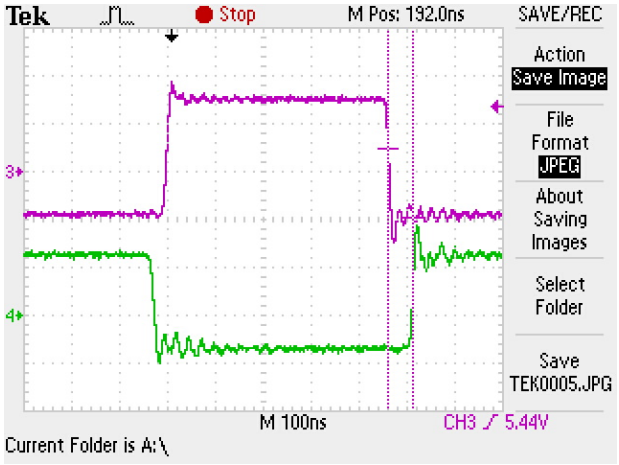
- Connect 12V Power supply and connect to J6 Pin1(+), Pin2(-)
- Connect DeadBand PCB to DC-DC Optimizer PCB connector J5
- Jumper setting on DC-DC Optimizer PCB
    - JP1: Jumper 1-2 (Boost Mode)
    - JP2: Jumper 1-2 (Boost Mode)
    - JP3: Jumper 2-3 (Boost Mode)
    - JP4: Jumper 2-3 (Boost Mode)
    - JP5: Jumper 1-2 (Driver Enable)
- Set SW1 switch on DeadBand PCB downward (Boost Operation)
- Connect Function Generator to DeadBand PCB JP1
- Set the frequency to 1.00MHz, Square Wave, 50% duty cycle, 0-3.3V Pulse
- Turn on Power Supply
- Use oscilloscope to probe TP17, TP18, differential probe across TP28, TP29 and differential probe across TP30, TP31

Test Results

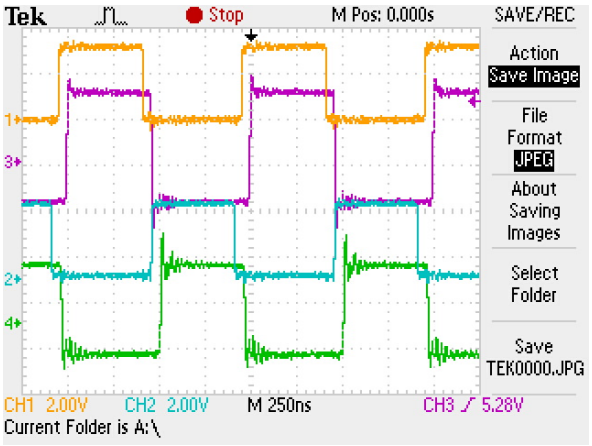
Channel 1: TP17
Channel 2: TP18
Channel 3: Differential probe across TP28, TP29
Channel 4: Differential probe across TP30, TP31



DeadBand: ~ 30ns



DeadBand: ~ 50ns



Overall Input and Output Scope Probe

5.4 Boost Power Supply

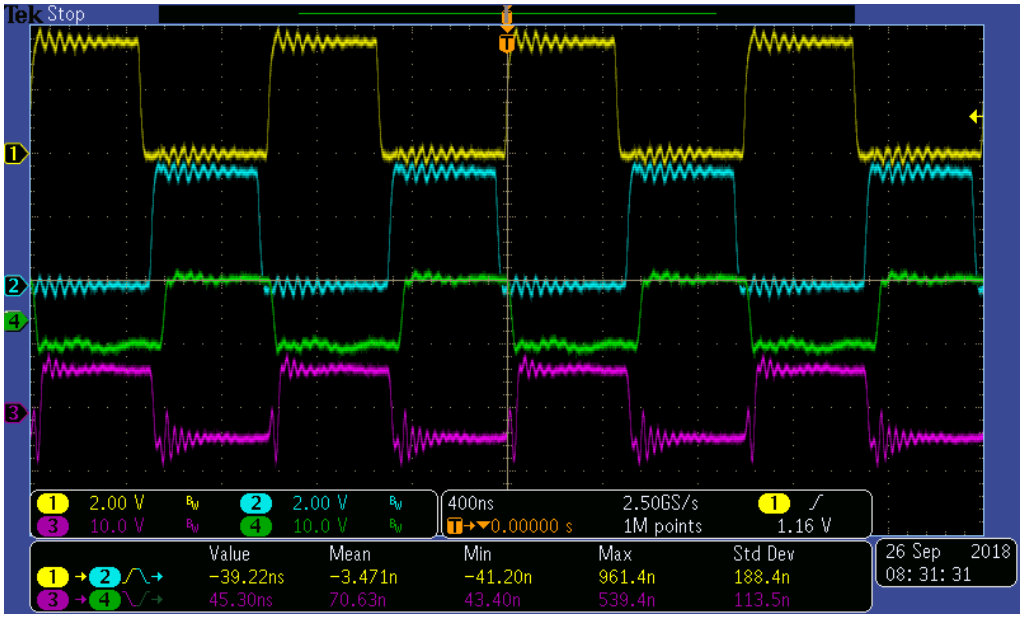
Test Setup:

- Connect 12V Power supply and connect to J6 Pin1(+), Pin2(-)
- Connect DeadBand PCB to DC-DC Optimizer PCB connector J5
- Jumper setting on DC-DC Optimizer PCB
    - JP1: Jumper 1-2 (Boost Mode)
    - JP2: Jumper 1-2 (Boost Mode)
    - JP3: Jumper 2-3 (Boost Mode)
    - JP4: Jumper 2-3 (Boost Mode)
    - JP5: Jumper 1-2 (Driver Enable)
- Set SW1 switch on DeadBand PCB downward (Boost Operation)
- Connect Function Generator to DeadBand PCB JP1
- Set the frequency to 1.00MHz, Square Wave, 50% duty cycle, 0-3.3V Pulse
- Connect other power supply and set to 25V input (at least 20A) to J1 and J2
- Connect ~ 5 ohm load, 500W across J3 and J4
- Turn on both power supply
- Use DMM measure across J3 and J4
- Adjust the duty cycle the DBUS_OUT read ~ 50V

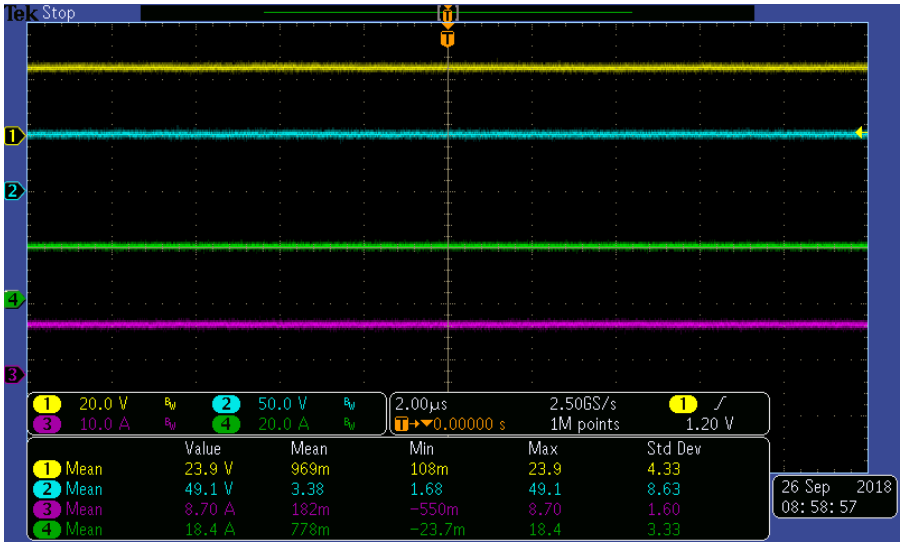
Test Results

Full Load

Channel 1: TP17
Channel 2: TP18
Channel 3: Differential probe across TP28, TP29
Channel 4: Differential probe across TP30, TP3



Efficiency
Channel 1: Voltage Input
Channel 2: Voltage Output
Channel 3: Current Output
Channel 4: Current Intput



Efficiency = (49.1V x 8.70A) / (23.9V x 18.4A) x 100% = 97.13%

5.5 Buck Power Supply

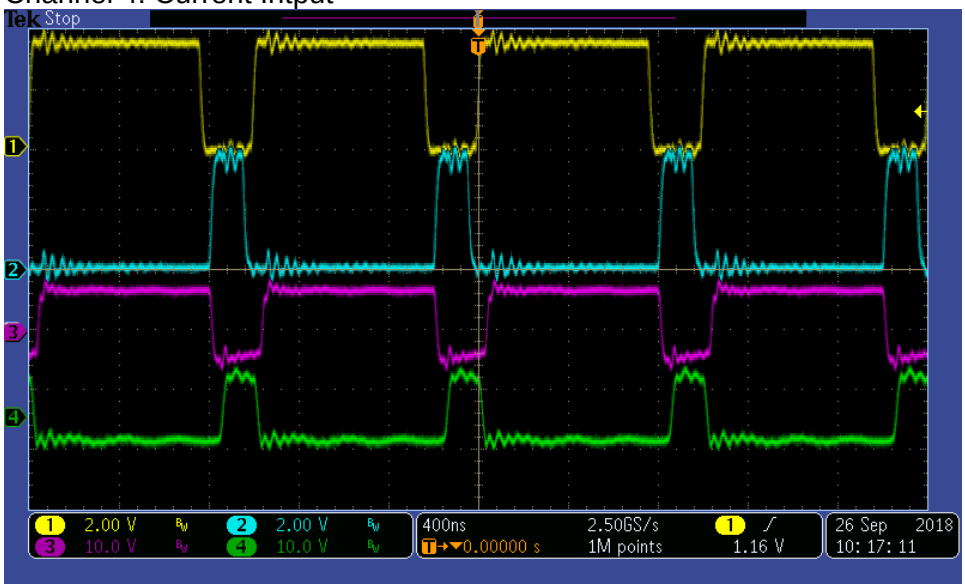
Test Setup:

- Connect 12V Power supply and connect to J6 Pin1(+), Pin2(-)
- Connect DeadBand PCB to DC-DC Optimizer PCB connector J5
- Jumper setting on DC-DC Optimizer PCB
    - JP1: Jumper 2-3 (Buck Mode)
    - JP2: Jumper 2-3 (Buck Mode)
    - JP3: Jumper 1-2 (Buck t Mode)
    - JP4: Jumper 1-2 (Buck Mode)
    - JP5: Jumper 1-2 (Driver Enable)
- Set SW1 switch on DeadBand PCB upward (Buck Operation)
- Connect Function Generator to DeadBand PCB JP1
- Set the frequency to 1.00MHz, Square Wave, 50% duty cycle, 0-3.3V Pulse
- Connect other power supply and set to 30V input (at least 20A) to J1 and J2
- Connect ~1 ohm load, 500W across J3 and J4
- Turn on both power supply
- Use DMM measure across J3 and J4
- The Power Supply should be around 15V
- Adjust the duty cycle the DBUS_OUT read ~ 20V

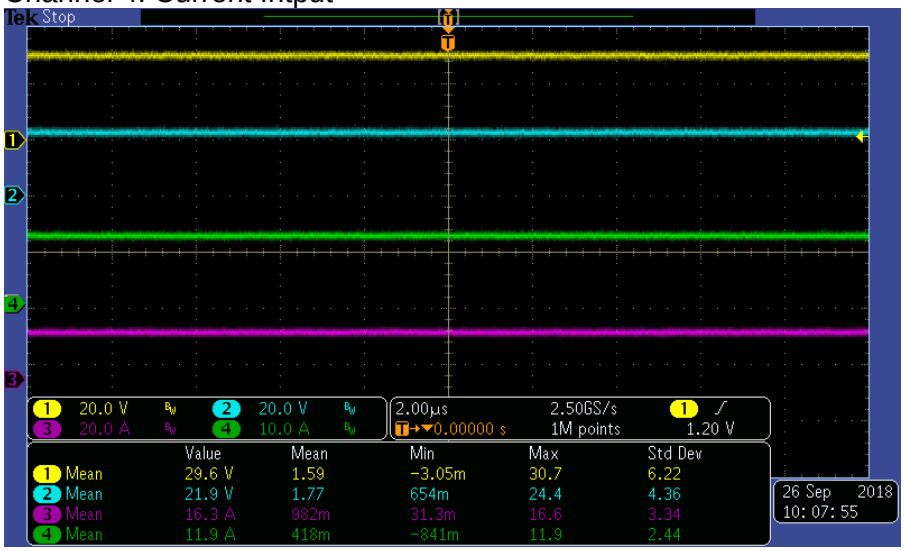
Test Results

Full Load

Channel 1: Voltage Input
Channel 2: Voltage Output
Channel 3: Current Output
Channel 4: Current Intput



Efficiency
Channel 1: Voltage Input
Channel 2: Voltage Output
Channel 3: Current Output
Channel 4: Current Intput



Efficiency = (29.6V x 11.9A) / (21.9V x 16.3A) = 98.7%

5.6 OverVoltage Protection

Test Setup:

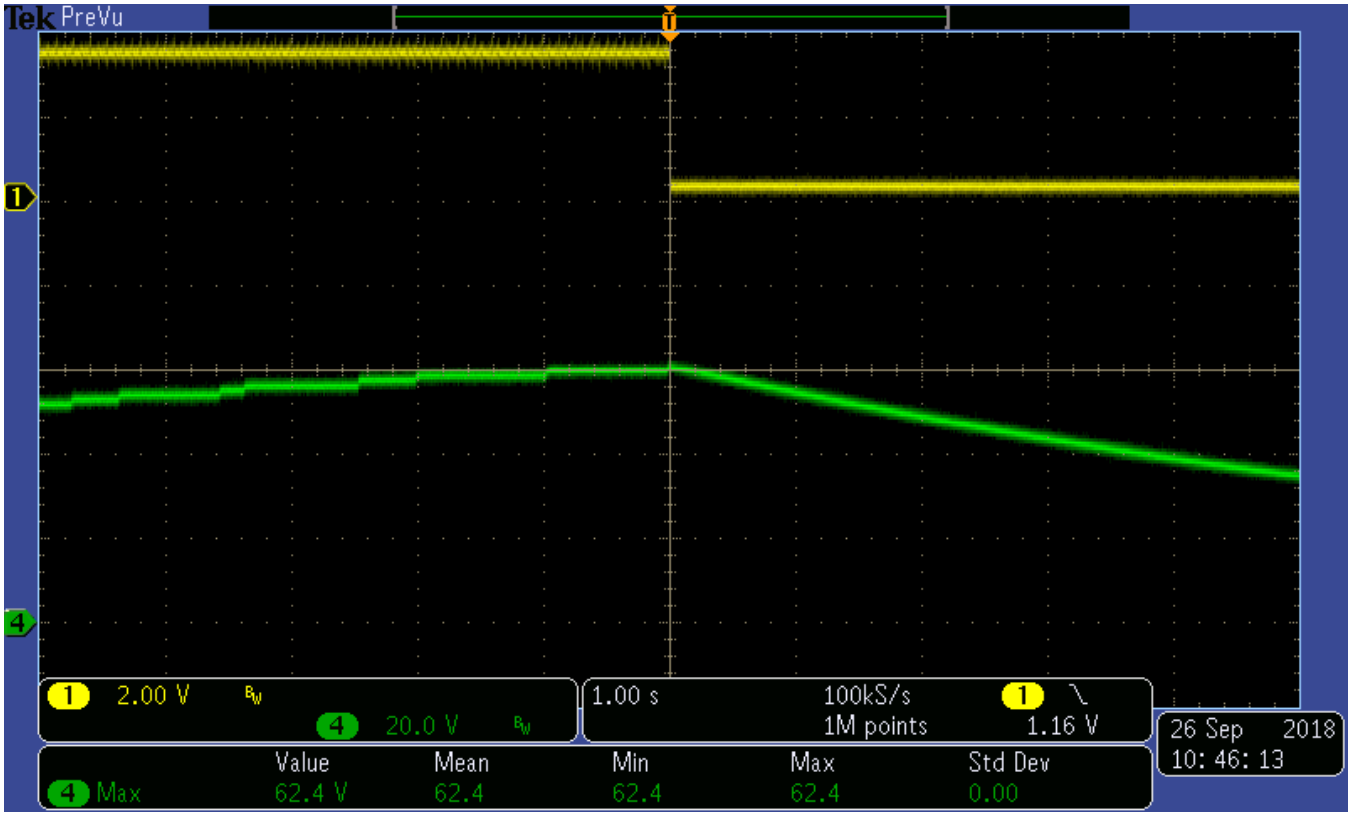
- Connect 12V Power supply and connect to J6 Pin1(+), Pin2(-)
- Connect DeadBand PCB to DC-DC Optimizer PCB connector J5
- Jumper setting on DC-DC Optimizer PCB
    - JP1: Jumper 1-2 (Boost Mode)
    - JP2: Jumper 1-2 (Boost Mode)
    - JP3: Jumper 2-3 (Boost Mode)
    - JP4: Jumper 2-3 (Boost Mode)
    - JP5: Jumper 1-2 (Driver Enable)
- Set SW1 switch on DeadBand PCB downward (Boost Operation)
- Connect Function Generator to DeadBand PCB JP1
- Set the frequency to 1.00MHz, Square Wave, 50% duty cycle, 0-3.3V Pulse
- Connect other power supply and set to 25V input (at least 20A) to J1 and J2
- Do not connect load
- Turn on both power supply
- Use DMM measure across J3 and J4
- Adjust the duty cycle until the DBUS_OUT read ~ 60V
- Slightly adjust duty cycle to increase DBUS_OUT until the overvoltage LED turn on
- The overvoltage trip is recorded around ~ 64V
- Verify the driver is disabled and latched, DCBUS_OUT is discharging to zero
- Turn off the function generator
- Connect TP14 (+3.3V) to TP21 (OVL_RESET) to reset the trip
- Verify Overvoltage LED turn off

Test Results

- *Specification Requirements (Pass/Fail Criteria)*

	Unit	Min	Typ	Max	Measurement Results	Pass/ Fail	Comment
OverVoltage							
OverVoltage Trip	V	55.00	60.00	65.00	**62.4**	☒ ☐	
Red LED On During Trip						☒ ☐	
Output Voltage Discharge						☒ ☐	
Reset Logic							
Red LED Off After Trip						☒ ☐	
Output Voltage Regulate Again (Test Output <50V)						☒ ☐	

OverVoltage Trip
Channel 1: /VOL, TP20
Channel 2: Voltage Output



5.7 Additional Efficiency Measurements

Measurement	Equipment Used	Rated Accuracy
Input Current	Fluke 8808A	+/-0.2%
Output Current	Fluke 8808A	+/-0.2%
Input Voltage	Fluke 8840A	+/-0.01%
Output Voltage	Fluke 777III	+/-0.3%

Note: added 1nF capacitor in C10, C11, C20, C21 locations.

FREQ (MHz)	Duty Cycle	RL (Ω)	VIN (V)	IN (A)	VOUT (V)	IOUT (A)	PIN (W)	POUT (W)	EFF. %
0.1	50%	10	70.289	1.74085	34.5	3.4314	122.363	118.383	96.75%
0.2	50%	10	70.296	1.70527	34.3	3.4054	119.874	116.805	97.44%
0.3	50%	10	70.342	1.68019	34	3.3804	118.188	114.934	97.25%
0.4	50%	10	70.4	1.65733	33.7	3.3550	116.676	113.064	96.90%
0.5	50%	10	70.264	1.63128	33.4	3.3204	114.620	110.901	96.76%
0.75	50%	10	70.266	1.57704	32.7	3.2532	110.812	106.380	96.00%
1	50%	10	70.23	1.52531	32.11	3.1850	107.123	102.270	95.47%

Previous tests without gate capacitance:

FREQ (MHz)	D.C. %	RL (Ω)	VIN (V)	IN (A)	VOUT (V)	IOUT (A)	PIN (W)	POUT (W)	EFF. %
0.5	50%	10	70.083	1.46827	31.27	3.0884	102.9008	96.574268	93.85%
0.75	50%	10	70.22	1.47097	31.35	3.0975	103.2915	97.106625	94.01%
1	50%	10	70.22	1.51525	31.81	3.1424	106.4009	99.959744	93.95%
1.25	50%	10	70.259	1.47324	31.37	3.0985	103.5084	97.199945	93.91%
1.5	50%	10	70.277	1.42413	30.71	3.0346	100.0836	93.192566	93.11%
FREQ (MHz)	D.C. %	RL (Ω)	VIN (V)	IN (A)	VOUT (V)	IOUT (A)	PIN (W)	POUT (W)	EFF. %
0.5	58%	10	70.243	1.85627	35	3.4636	130.39	121.226	92.97%
0.75	58%	10	70.288	1.77543	34.2	3.3835	124.7914	115.7157	92.73%
1	58%	10	70.268	1.94953	36	3.5616	136.9896	128.2176	93.60%
1.25	58%	10	70.26	1.9639	36.2	3.5847	137.9836	129.76614	94.04%
1.5	58%	10	70.27	1.94117	36	3.5585	136.406	128.106	93.92%
FREQ (MHz)	D.C. %	RL (Ω)	VIN (V)	IN (A)	VOUT (V)	IOUT (A)	PIN (W)	POUT (W)	EFF. %
0.5	45%	10	70.136	1.22019	28.59	2.8243	85.57925	80.746737	94.35%
0.75	45%	10	70.172	1.23417	28.75	2.8408	86.60418	81.673	94.31%
1	45%	10	70.235	1.22497	28.57	2.8249	86.03577	80.707393	93.81%
1.25	45%	10	70.255	1.18567	28	2.7682	83.29925	77.5096	93.05%
1.5	45%	10	70.257	1.15926	27.58	2.726	81.44613	75.18308	92.31%