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SINGLE EVENT EFFECTS TEST REPORT ADUM7442

May 2016

Radiation Test Report	
Product:	ADuM7442S
Effective LET:	80 MeV-cm^2/mg
Fluence:	1E7 Ions/cm^2
Die Type:	ADUM7442IC1, ADUM7442IC2_AS
Facilities:	Lawrence Berkeley National Laboratories
Tested:	March 2016

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Colo. Springs, CO 80919
(719) 531-0800

Single Event Effects (SEE) Test Report for the Analog Devices ADuM7442S 1kV RMS Quad-Channel Digital Isolators

Customer PO: 45533851

Aeroflex RAD Job Number: 15-0728

Part Type Tested: Analog Devices ADuM7442S 1kV Quad-Channel Digital Isolators

Part Markings: None

Quantity of Parts for Testing: Five parts for single event latch-up (SEL) testing, four parts for single event transient (SET) testing, one control, five spares.

Referenced Test Standard(s): ASTM F1192 and EIA/JESD57

Electrical Test Conditions: Supply current was recorded before, during, and after heavy ion exposure and monitored for any change at one second intervals.

Bias Conditions: All devices-under-test (DUTs) were biased during heavy ion irradiation using custom bias boards using the bias conditions listed in Section 2.3. The ADuM744xS Characterization/Evaluation Board was provided by Analog Devices for SEL Testing. A custom DUT board was designed for SET testing. Details of the custom DUT boards are shown in Appendix B.

Test Software / Hardware: Custom VISA control and monitor software was used for all test operations. The test setups are shown in Figure 2-1 and Figure 2-3, while the test equipment and calibration dates are shown in Appendix C, Table C-1.

Ion Energy and LET Ranges: Multiple ions from the 10 MeV/n ion beam with normal incidence linear energy transfers (LETs) of up to approximately 80 MeV·cm^2/mg were available for testing.

Heavy Ion Flux and Maximum Fluence Levels: Testing was conducted with ion fluxes between approximately 10^4 and 10^5 ions/cm^2/sec. For SEL testing, the beam was shut off when the fluence reached 10^7 ions/cm^2. For SET testing, the beam was shut off when the fluence reached 10^6 ions/cm^2.

Facility and Radiation Source: Lawrence Berkeley National Laboratories (LBNL) Berkeley, CA using the 88" Cyclotron and the 10 MeV/n cocktail.

Irradiation Temperature: For SEL testing, the devices were tested at 125˚C ±5 ˚C. For SET testing, the devices were tested at ambient temperature.

RESULTS:

No latchup or other destructive SEE was observed on the ADuM7442S to the highest level tested: LET ≤ 80 MeV·cm^2/mg, 125°C, VDD1 = +5.5V, VDD2 = +5.5V, and 4 samples.

The ADuM7442S has a typical dropout length of 5 clock cycles and a maximum dropout length of 32 clock cycles with a 10 MHz input. Dropouts occur on all outputs. The LET threshold is ~4 MeV·cm^2/mg with a saturation cross-section of $1.5\text{x}10^{-4}$ cm^2/upset.

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1.0. Introduction and Test Objectives

It is well known that heavy ion exposure can cause temporary or permanent damage in electronic devices. The damage can occur through various mechanisms including SEL, single event burnout (SEB) and single event gate rupture (SEGR). These SEEs can lead to system performance issues including degradation, disruption and destruction. Additionally, Single Event Transient (SET) effects, while not destructive in nature, can also have deleterious effects on systems. This test report details the SEL testing performed on the Analog Devices ADuM7442S 1kV Quad-Channel Digital Isolators. The two test standards used to guide this testing were ASTM F1192 and EIA/JESD57.

The Analog Devices ADuM7442S 1kV Quad-Channel Digital Isolators described in this test report was irradiated at LBNL. The 10 MeV/n beam was used to provide a sufficient range in silicon while meeting the LET requirements.

All DUTs were de-processed prior to testing and all exposures took place from the top surface providing a distance to the active layer in Silicon of approximately 5 to 10 µm. A sample of a de-processed DUT is shown in Appendix A.

The objective of SEL testing was to determine the current latch-up threshold in the device under worst case temperature and voltage conditions up to an LET of 80 $MeV{\cdot}cm^2/mg$. For the SEL testing, the devices were irradiated to a maximum fluence of 10^7 $ions/cm^2$ at a temperature of 125°C.

The objective of the SET test was to determine the upset rate for the DUT at a given LET and to also provide some statistics regarding the nature (magnitude and duration) of these transients. The transient cross section of the DUT as a function of LET was generated.

2.0. Radiation Test Circuit, Setup, Parameters, Conditions, and Procedures

2.1. SEL Test Setup

The Analog Devices ADuM7442S 1kV Quad-Channel Digital Isolators were tested on ADuM744xS Characterization/Evaluation Boards which were provided by Analog Devices.

The SEE test setup for the ADuM7442S is shown in Figure 2-1. Each ADuM7442S was mounted on an ADuM744xS Characterization/Evaluation Board. The Keithley 2410 Source Meter provided the VDD1 voltage and measured the associated current. The Keithley 2420 Source Meter provided the VDD2 voltage and measured the associated current. The Instek AFG-2125 Generator provided a 10 MHz, 0 to 5 volt square-wave input signal that was split between the four input channels to the ADuM7442. The Housekeeping Power Supply provided +/-5 volts and 24 volts for the Temperature Controller Distribution Board and the Heater Board attached on the backside of the DUT boards during SEL testing. The PicoScope 6404D Oscilloscope monitored the four outputs of the ADuM7442. The Shutter Status Monitor recorded the beam shutter position. The laptop personal computer (PC) controlled the test equipment and executed the GUI for functional testing of the component.

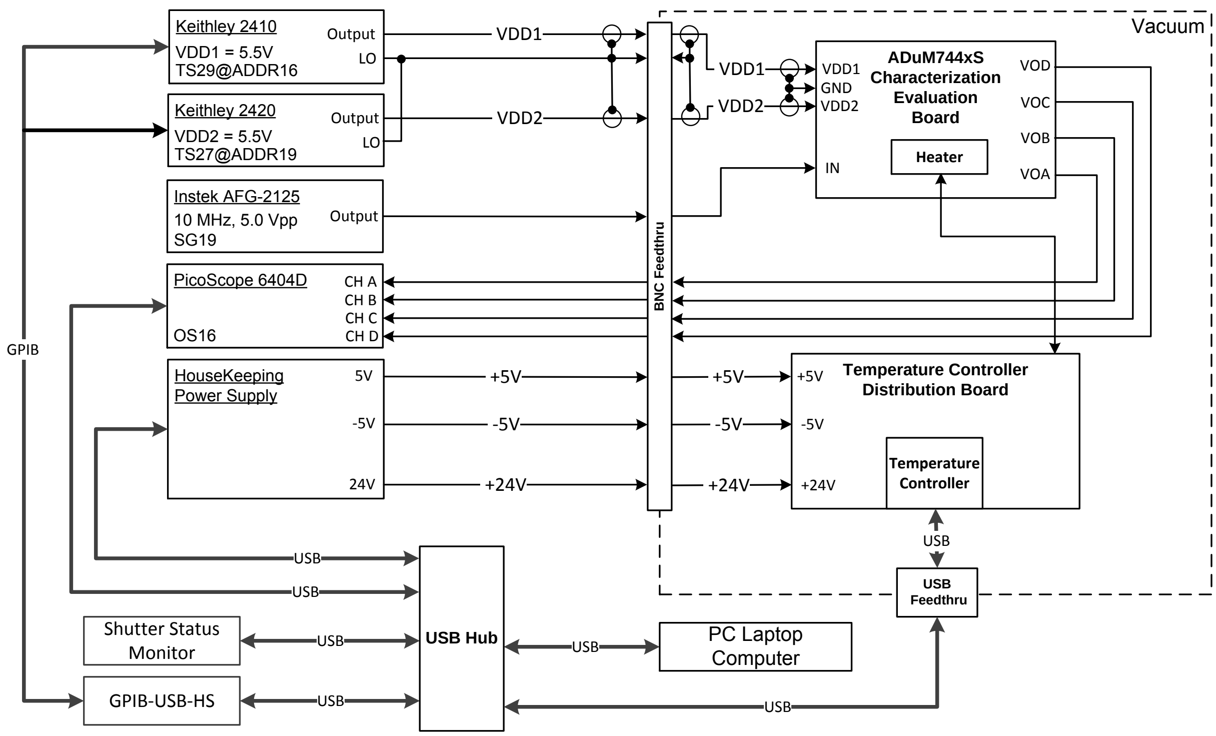

Figure 2-1. ADuM7442S SEL Test Setup.

NOTE: The Shutter Status Monitor monitors the beam shutter signal provided by the facility. It is simply a TTL level signal used to indicate when, in time, the shutter is open and the parts are being exposed and as such provides a reference time signal for the data logging.

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2.2. SET Test Setup

For SET testing, the Analog Devices ADuM7442S 1kV Quad-Channel Digital Isolators described in this test report was irradiated at LBNL using the custom ADuM7442S Test Board.

The DUT test circuit for the ADuM7442S was configured as shown in Figure 2-2. This circuit can be configured such that GND1 and GND2 are at different potentials. However, for this test GND1 and GND2 were tied together so they have the same potential. Only one DUT is installed on the test board at a given time, the choice depends on whether the GND2 side (DUT1 position) or the GND1 side (DUT2 position) of the DUT is to be at a higher GND potential. A second ADuM7442S is used to isolate the potentially high voltage from the test input and output signals, although for this test the grounds were at the same potential so high voltage was applied. Two 74LVC1G17 Schmitt Trigger Buffers are used to provide proper signal levels for the 10 MHz test signal to inputs of the ADuM7442S.

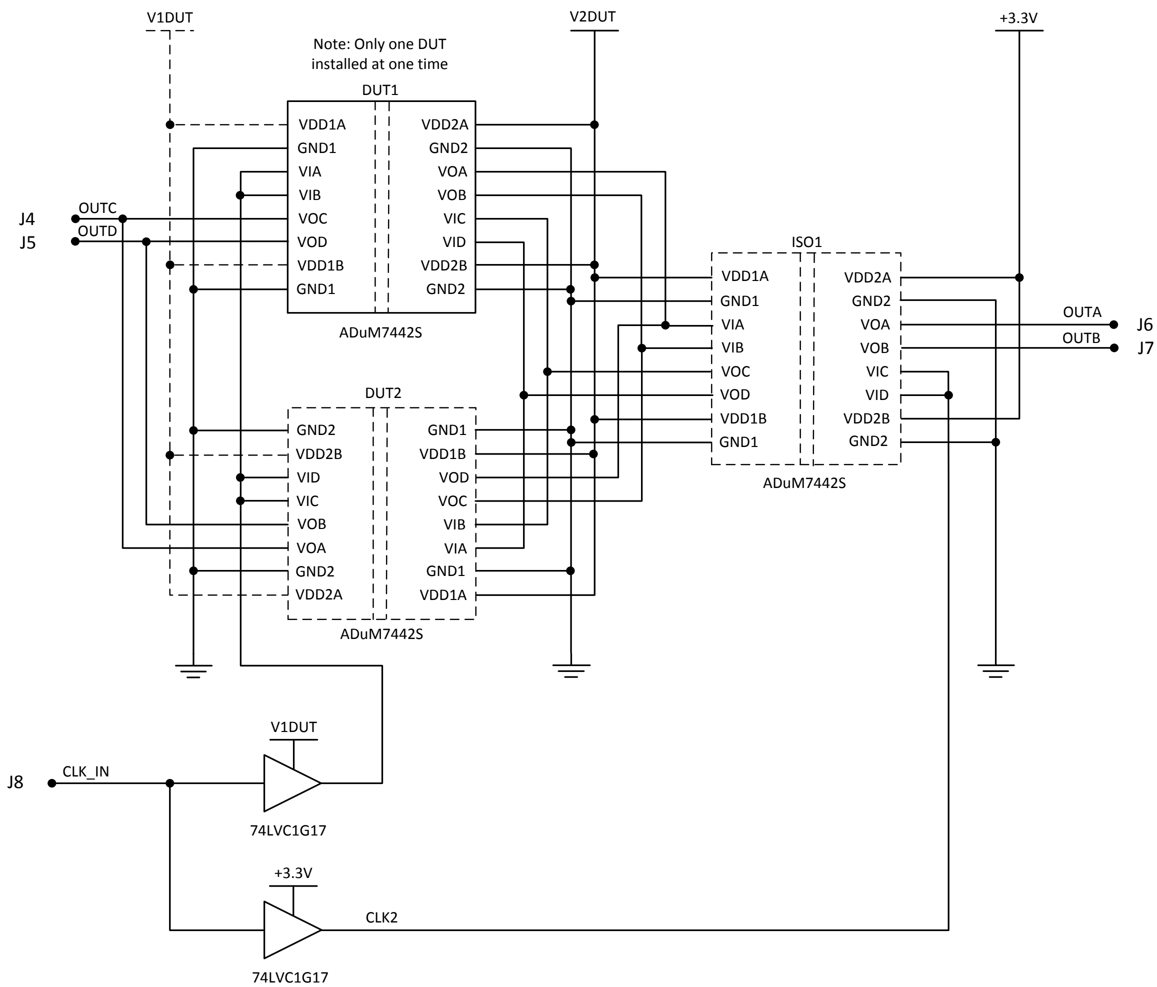

Figure 2-2. Analog Devices ADuM7442S DUT SEE Test Circuit.

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The SET test setup for the ADuM7442S is shown in Figure 2-3. The Keithley 2420 Source Meter provides the V1DUT voltage and measures the associated current. The Keithley 2425C Source Meter provides the V2DUT voltage and measures the associated current. The Housekeeping Power Supply provides ± 5 volts and +24 volts to the ADUm7442S Test Board. The Instek AFG-2125 Generator provides a 10 MHz, 0 to 5 volt square-wave input signal. The PicoScope 6404D Oscilloscope monitors and records the four outputs of the ADuM7442S. The Agilent 34970A Data Acquisition Unit with the Agilent 34901A Multiplexer Plug-in provides the capability to measure the ± 5 volts, V1DUT, +3.3 volts, and V2DUT voltages at the ADuM7442S Test Board. The Shutter Status Monitor records the beam shutter position. The laptop personal computer (PC) controls the test equipment and collects the oscilloscope data.

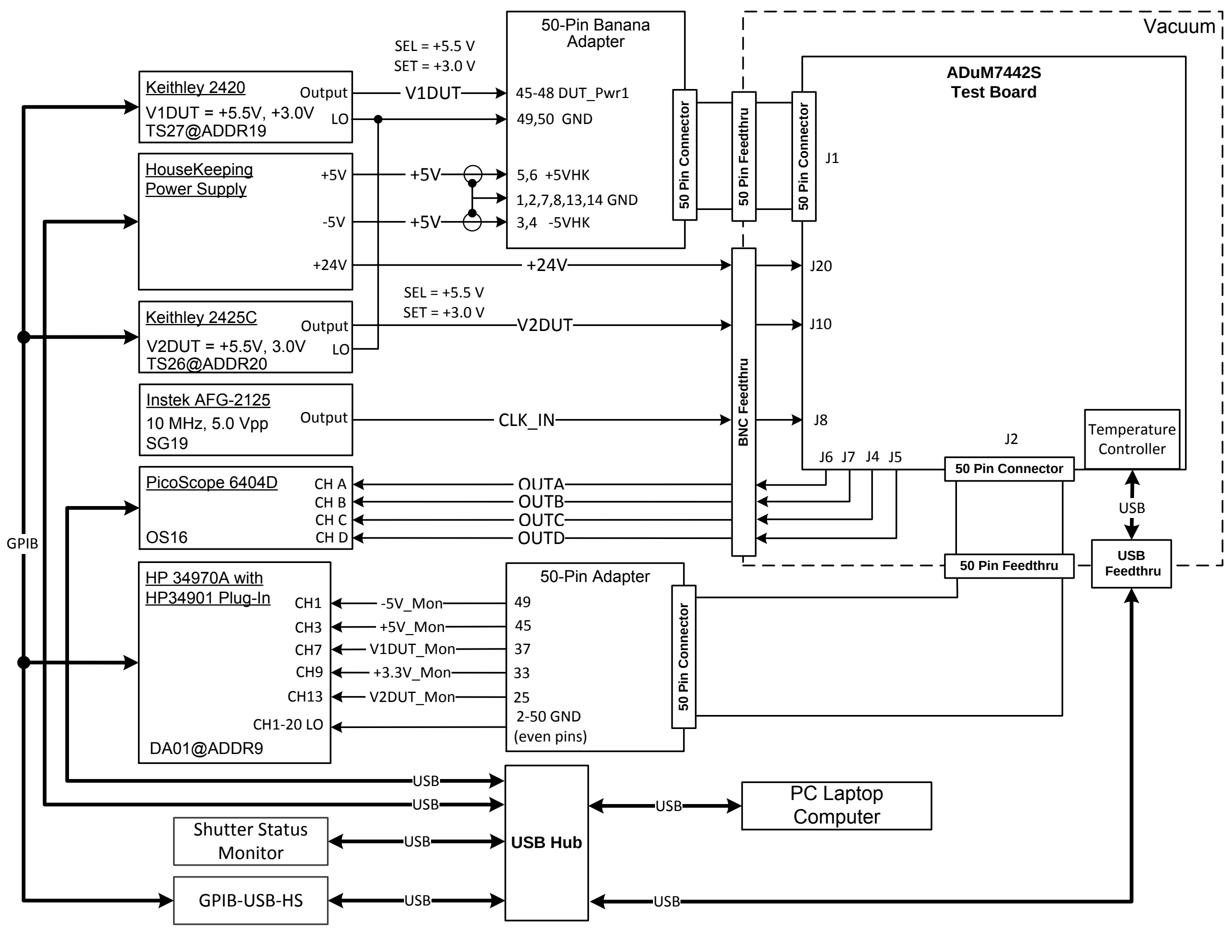

Figure 2-2. Analog Devices ADuM7442S SEE Test Setup.

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2.3. Test Parameters

Parameters measured during SEL testing (at approximately 1 second intervals):

1. The DUT temperature
2. The VDD1 current
3. The VDD2 current
4. Beam Shutter Status

Parameters measured during SET testing (at approximately 1 second intervals):

1. The DUT temperature
2. The V1DUT voltage at the DUT
3. The V1DUT current
4. The V2DUT voltage at the DUT.
5. The V2DUT current
6. The +3.3V voltage at the test board
7. The +5V voltage at the test board
8. The -5V voltage at the test board
9. Beam shutter status
10. Out A signal
11. Out B signal
12. Out C signal
13. Out D signal

The supply voltage, DUT temperature, and ion fluence for the SEL and SET testing were as follows:

	SEL	**SET**
DUT Temperature	125°C	Ambient
VDD1	+5.5V	+3.0V
VDD2	+5.5V	+3.0V
Max. fluence	10^7 ions/cm^2	10^6 ions/cm^2
CLK_IN Signal	10MHz, 0-5V Square-Wave	10MHz, 0-5V Square-Wave*

* CLK_IN signal voltage levels are translated to 0-V1DUT on the test board.

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2.4. Test Conditions

The signals monitored during the test were routed to the control room (approximately 20-feet away) using shielded coaxial cable. Table 2-1 lists the ions, angles, and LETs used to characterize the SEE response of the ADuM7442S devices.

Table 2-1. Ions Used for SEL Characterization

Ion	Angle (Degrees)	LET (MeV·cm^2/mg)
Argon	0	9.7
Copper	0	21.2
Copper	30	24.5
Krypton	0	30.9
Silver	0	48.2
Xenon	0	58.8
Xenon	43	80.4

2.5 SEL Test Procedure

During the heavy ion exposure, the supply currents of the ADuM7442S were monitored and recorded at approximately 1-second intervals. The current limit on the power supplies were set to 100 mA.

The following general SEL test procedure was followed:

1. Power up the selected DUT and wait for it to attain the desired test temperature.
2. Select the desired ion and incident angle for the desired LET.
3. Verify the ADuM7442S is functioning properly.
4. Turn on the ion beam, observe/monitor/log device current.
5. If no latch up occurs and the fluence reaches 10^7 ions/cm^2, shut off the beam and verify device functionality.
6. Select the desired ion and incident angle that gives a higher LET value up to 80 MeV·cm^2/mg and repeat from step 3.
7. If no latch up occurs up to an LET of 80 MeV·cm^2/mg, select the next DUT and repeat from step 1.

If a latch up occurs during a run, then the following procedure is followed:

8. Shut off the beam, cycle DUT power and check the currents for a destructive latch.
9. If the latch is not destructive and the DUT is still functional, select an ion and/or incident angle combination that gives a lower LET value and repeat from step 3.
10. If the latch is destructive, select the next DUT and repeat step 1 using an ion and/or incident angle combination that give a lower LET value.

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2.6 SET Test Procedure

During the heavy ion exposure the supply currents of the ADuM7442S were monitored and recorded at approximately 1-second intervals. The current limit on the power supplies were set to 100 mA. Two SET tests were performed with the DUT installed in the DUT1 position and two SET tests were performed with the DUT installed in the DUT2 position.

The following general SET test procedure was used:

1. Power up the DUT.
2. Select the desired ion and desired angle of incidence.
3. Turn on the ion beam while observing, monitoring and logging the power supply currents and recording the pulse counts per 1 sec intervals.
4. Turn off the beam when either the fluence reaches 10^6 ions/cm^2 or a statistically significant number of events have been recorded (i.e. 100 or possibly less at low flux).
5. Repeat the procedure beginning at step 2 until the DUT has been irradiated across the desired range of LETs (2 MeV-cm^2/mg to 80 MeV-cm^2/mg).
6. Test the remaining DUTs.

During heavy ion exposure the outputs of the DUT were monitored for proper operation and transient events using the oscilloscope. The oscilloscope was triggered on transients occurring on channels A and C on two DUTS and channels B and D on two DUTS.

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3.0. SEE Test Results

The Analog Devices ADuM7442S 1kV Quad-Channel Digital Isolators was tested for single event effects at the LBNL Cyclotron Facility using their 88-Inch Cyclotron and the 10 MeV/n cocktail on December 3, 2015 and March 31, 2016.

3.1. SEL Test Results

During SEL testing, the power supplies were set to the following voltages: VDD1 = +5.5V, VDD2 = +5.5V. The DUT temperature was controlled to 125°C (±5 °C) for DUT serial numbers 2, 3, 4, and 13. After troubleshooting the test setup when installing DUT serial number 3, it was discovered that the temperature setting for DUT serial number 1 was actually 113°C. Table 3-1 lists the run and test conditions as well as the result of the run. With the SEL test conditions, at no point did any of the five DUTs experience a latch-up condition.

Table 3-1. ADuM7442S SEL Run Log.

Run	SN	Ion	Effective LET (MeV·cm^2/mg)	Effective Fluence (ion/cm^2)	Temp (°C)	Results
131	1	Cu	21.2	1.01E+07	113	No Latch-up
132	1	Kr	30.9	1.00E+07	113	No Latch-up
133	1	Ag	48.2	1.01E+07	113	No Latch-up
134	1	Xe	58.8	1.00E+07	113	No Latch-up
135	1	Xe@43°	80.4	1.00E+07	113	No Latch-up
136	3	Kr	30.9	1.01E+07	125	No Latch-up
137	3	Xe	58.8	1.01E+07	125	No Latch-up
138	3	Xe@43°	80.4	1.00E+07	125	No Latch-up
139	2	Xe@43°	80.4	1.00E+07	125	No Latch-up
140	4	Xe@43°	80.4	1.00E+07	125	No Latch-up
23	13	Xe@43°	80.4	1.02E+07	125	No Latch-up

Note: Runs 131 through 140 occurred on December 3, 2015; Run 23 occurred on March 31, 2016.

The nominal VDD1 current at 125°C was approximately 21.8 mA. The nominal VDD2 current at 125°C was approximately 20.2 mA. Appendix E illustrates the SEL current plots. Figure 3-1 illustrates a representative SEL current plot for VDD1 and Figure 3-2 illustrates a representative SEL current plot for VDD2.

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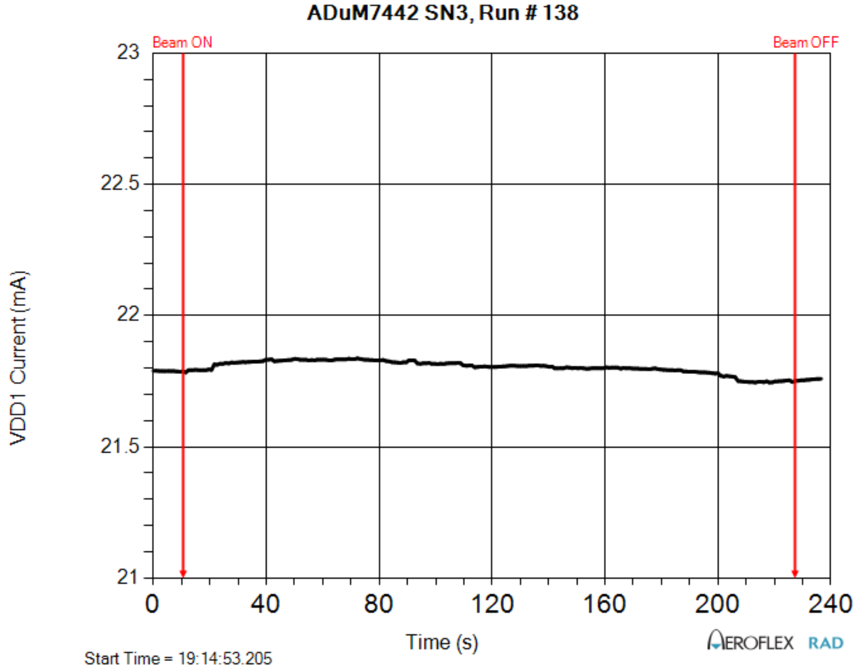

Figure 3-1. ADuM7442 SN3, Run #138, DUT VDD1 Current (mA).

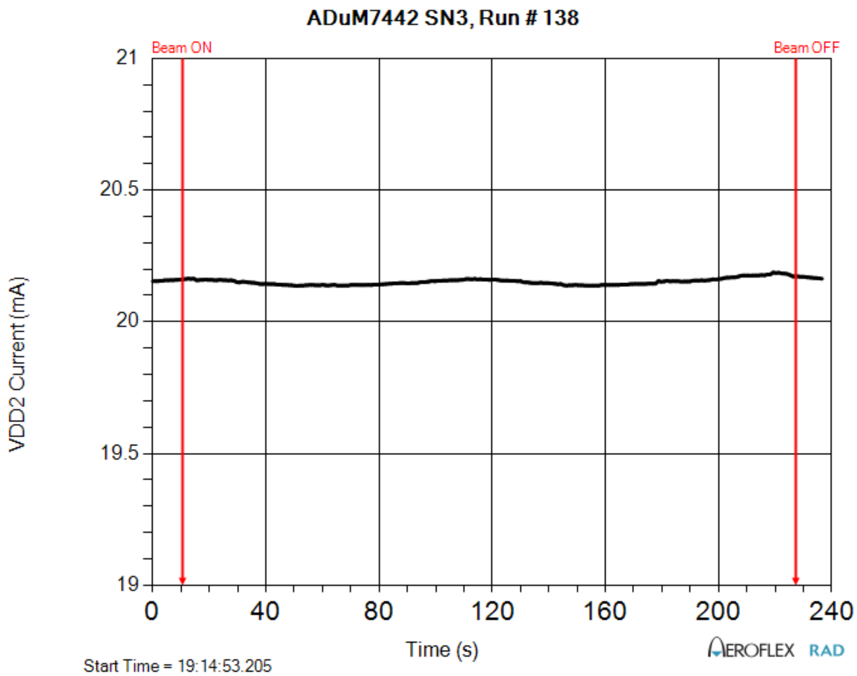

Figure 3-2. ADuM7442 SN3, Run #138, DUT VDD2 Current (mA).

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3.2. SET Test Results

The ADuM7442S was configured such that all four inputs were presented with an in-phase 10 MHz clock signal. Under nominal conditions, all four outputs were identical and input to the 4 channel Picoscope for evaluation. The period of a single cycle of the clock being shorter than 85 ns or greater than 115 ns was used to trigger the Picoscope which was in Rapid Trigger mode. In this mode the Picoscope records all four channels when a trigger occurred on the selected channel. Only one channel was used at a time to trigger the Picoscope. Up to 100 events were recorded per run. Table 3-2 lists all runs with the serial number, ion, angle, LET, trigger source, fluence, number of events, and cross-section. Figure 3-3 shows the upset cross-section as a function of LET. A Weibull curve with parameters Shape=3, Width=32, Saturation=1.5×10^{-4}, and Onset=4 is plotted for reference.

Figures 3-3 through 3-9 show some of the typical waveforms recorded during testing. Generally speaking any channel could dropout with the output going high or low during the dropout.

The following observations were made:

1. Dropouts were observed on one, two, three, or all four channels.
2. Dropouts where the output went to the low rail were observed on all channels.
3. Dropouts where the output went to the high rail were observed on all channels.
4. Dropouts where one channel went to the high rail and one went to the low rail were observed.
5. Typical dropouts (~80%) lasted about 5-6 clock cycles (500ns).
6. The maximum dropout last 32 clock cycles (3.2 μs) with approximately an order of magnitude smaller cross-section than the shorter variety.

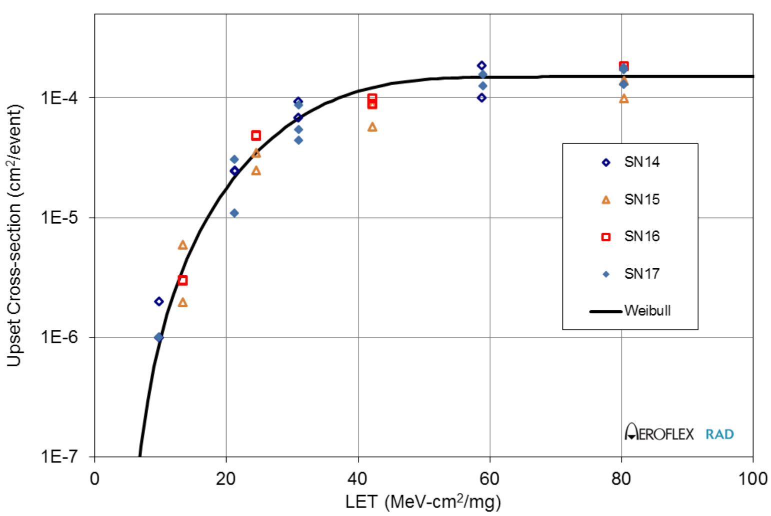

Figure 3-3. Upset Cross-section vs. LET for the ADuM7442S.

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Table 3-2. ADuM7442S SET Run Log.

Run#	DUT S/N	Ion	Angle (degrees)	LET (MeV-cm^2/mg)	Trigger Source	Fluence (ion/cm^2)	Number of Upsets	Cross-section (upsets/cm^2)	Comments
24	17	Xe	43	80.4	A	7.75E+05	100	1.29E-04	
25	17	Xe	43	80.4	C	5.62E+05	100	1.78E-04	
26	17	Xe	43	80.4	C	5.73E+05	100	1.75E-04	
27	17	Xe	43	80.4	B	7.75E+05	100	1.29E-04	
28	17	Xe	43	80.4	D	5.81E+05	100	1.72E-04	
29	17	Xe	0	58.8	A	7.93E+05	100	1.26E-04	
30	17	Xe	0	58.8	C	6.36E+05	100	1.57E-04	
31	17	Kr	0	30.9	A	1.08E+06	59	5.46E-05	Flux was high; data used
32	17	Kr	0	30.9	A	1.01E+06	44	4.36E-05	
33	17	Kr	0	30.9	C	5.78E+06	50	8.65E-06	
34	17	Ar	0	9.7	A	1.01E+06	0	0.00E+00	
35	17	Ar	0	9.7	C		0		No beam; facility issue.
36	17	Ar	0	9.7	C	1.01E+06	1	9.90E-07	
37	17	Cu	0	21.2	A	9.26E+05	10	1.08E-05	
38	17	Cu	0	21.2	C	3.29E+05	10	3.04E-05	
39	16	Cu	30	24.5	B	5.16E+05	25	4.84E-05	
40	16	Cu	30	24.5	D	5.09E+05	25	4.91E-05	
41	16	Ar	43	13.3	B	1.01E+06	3	2.97E-06	
42	16	Ar	43	13.3	D	1.01E+06	3	2.97E-06	
43	16	Kr	43	42.2	B	1.01E+06	90	8.91E-05	
44	16	Kr	43	42.2	D	1.00E+06	99	9.90E-05	
45	16	Xe	43	80.4	B	6.79E+05	100	1.47E-04	
46	16	Xe	43	80.4	D	5.45E+05	100	1.83E-04	
47	15	Xe	43	80.4	A	7.22E+05	100	1.39E-04	
48	15	Xe	43	80.4	C	1.01E+06	100	9.90E-05	
49	15	Kr	43	42.2	A	1.01E+06	89	8.81E-05	
50	15	Kr	43	42.2	C	1.01E+06	58	5.74E-05	
51	15	Ar	43	13.3	A	1.01E+06	6	5.94E-06	
52	15	Ar	43	13.3	C	1.01E+06	2	1.98E-06	
53	15	Cu	30	24.5	A	7.17E+05	25	3.49E-05	
54	15	Cu	30	24.5	C	1.01E+06	25	2.48E-05	
55	14	Cu	0	21.2	B	4.06E+05	10	2.46E-05	
56	14	Cu	0	21.2	D	4.01E+05	10	2.49E-05	
57	14	Ar	0	9.7	B	1.01E+06	2	1.98E-06	
58	14	Ar	0	9.7	D	1.01E+06	1	9.90E-07	
59	14	Kr	0	30.9	B	1.01E+06	94	9.31E-05	
60	14	Kr	0	30.9	D	1.01E+06	69	6.83E-05	
61	14	Xe	0	58.8	B	5.36E+05	100	1.87E-04	
62	14	Xe	0	58.8	D	1.01E+06	100	9.90E-05	

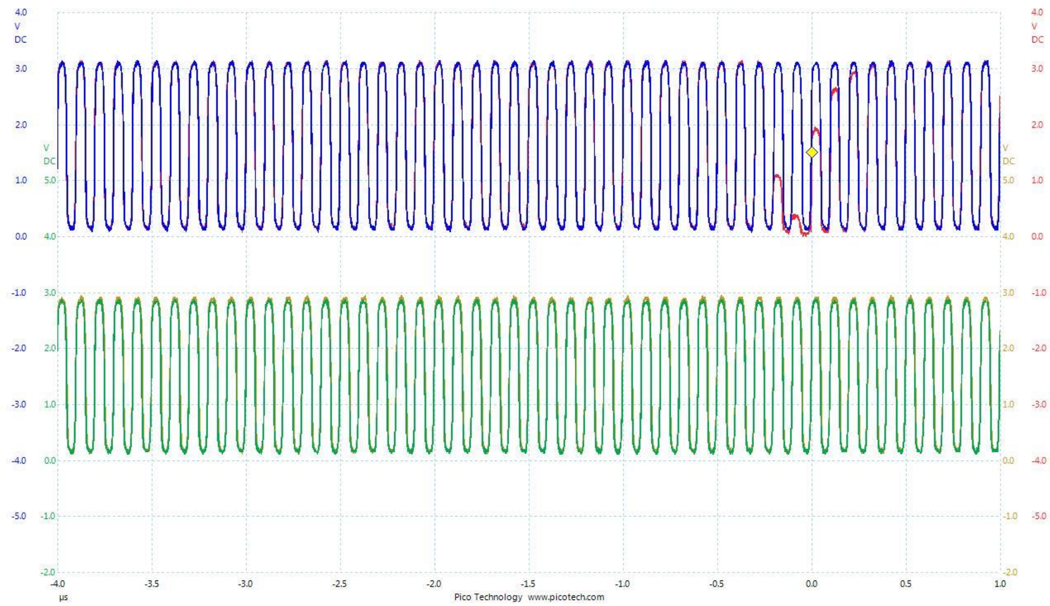

Figure 3-4. ADuM7442 SN17, Run #027, Frame 14 – Single Transient on Output B.

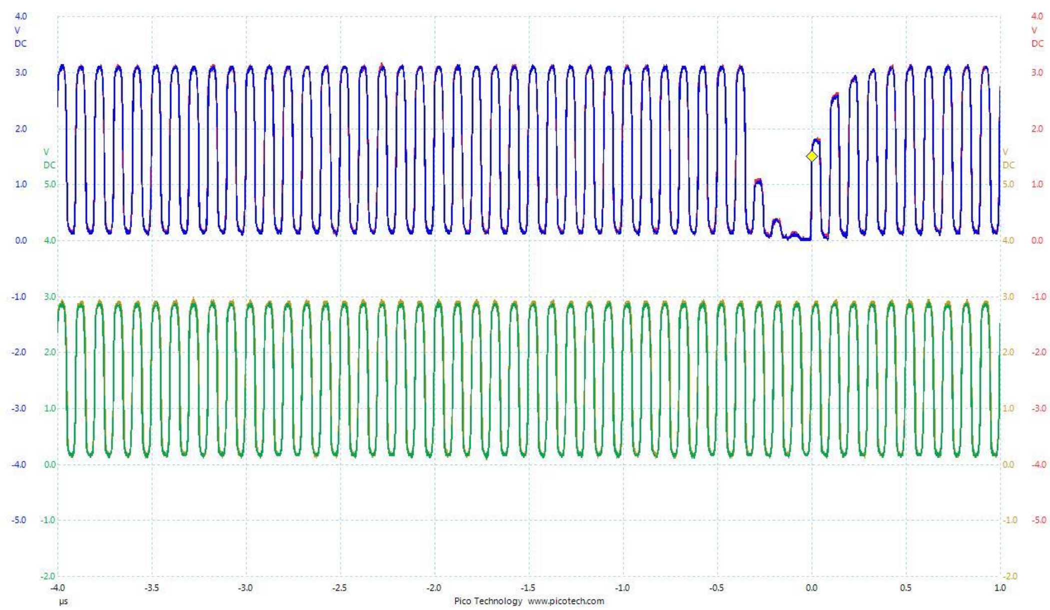

Figure 3-5. ADuM7442 SN17, Run #027, Frame 93 – In-Phase Transients on Outputs A & B.

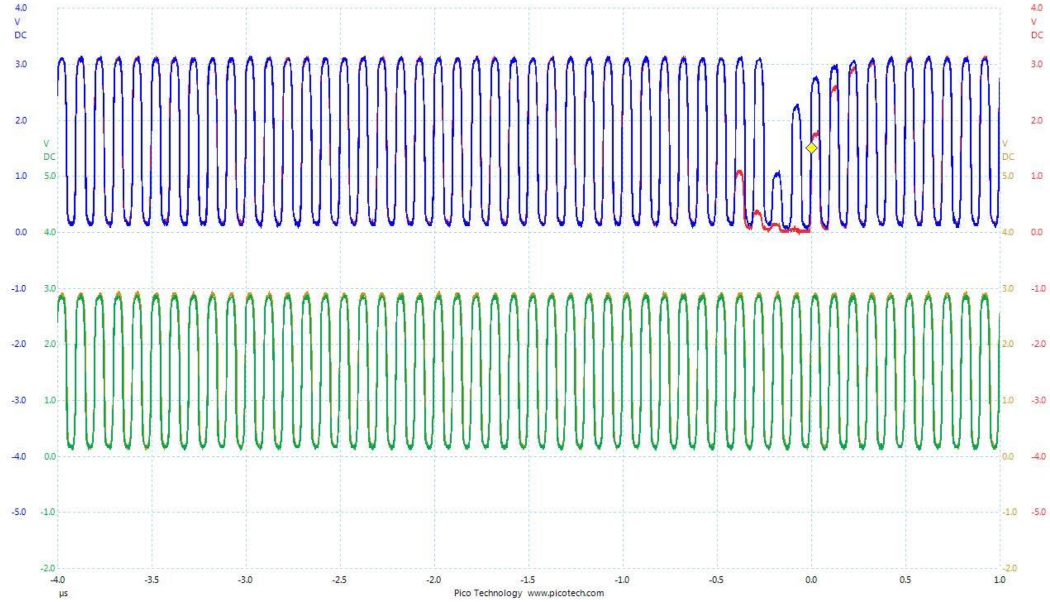

Figure 3-6. ADuM7442 SN17, Run #027, Frame 76 – Different Transients on Outputs A & B.

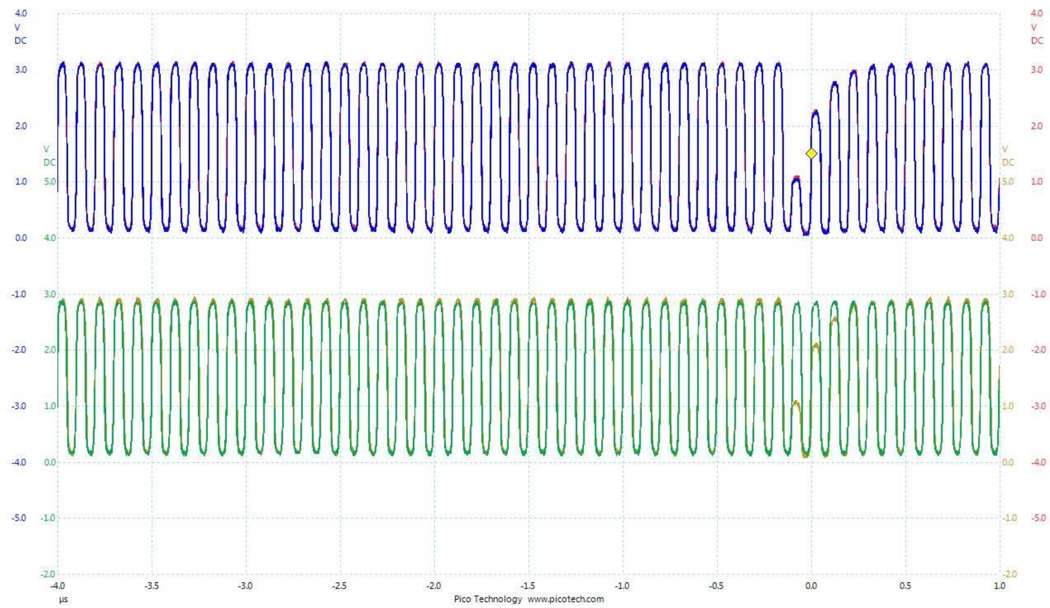

Figure 3-7. ADuM7442 SN17, Run #027, Frame 27 – In-Phase Transients on Outputs A, B & C.

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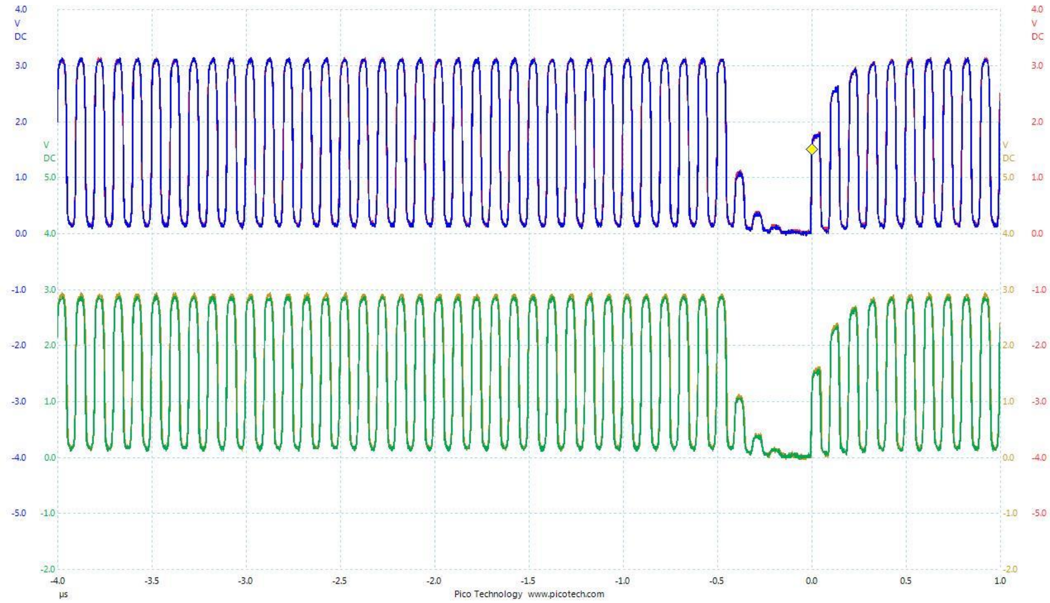

Figure 3-8. ADuM7442 SN17, Run #027, Frame 9 – In-Phase Transients on Outputs A, B, C & D.

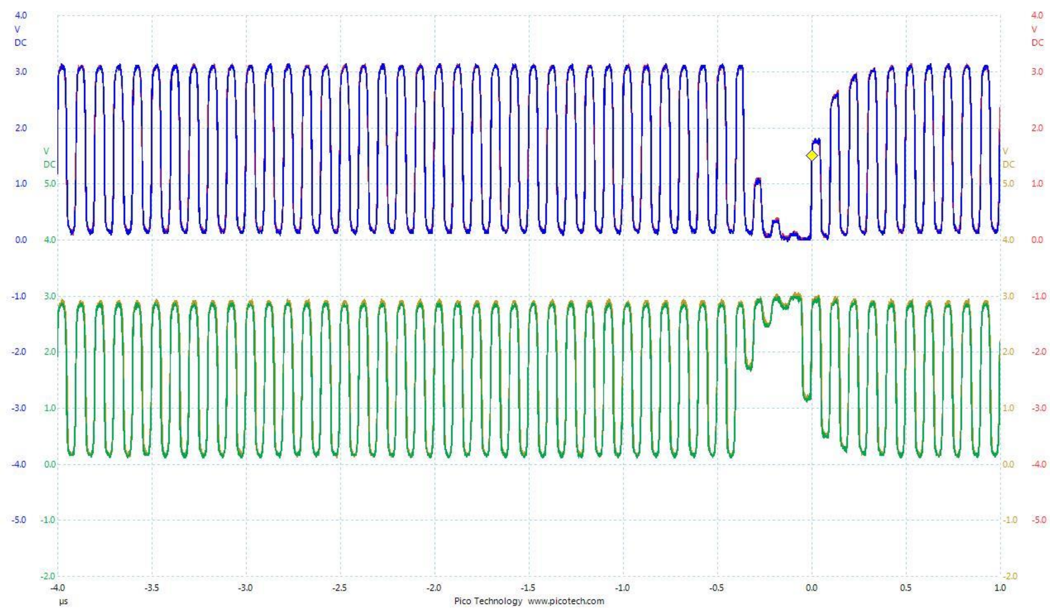

Figure 3-9. ADuM7442 SN17, Run #027, Frame 23 – Out of Phase Transients on Outputs A & B, C & D.

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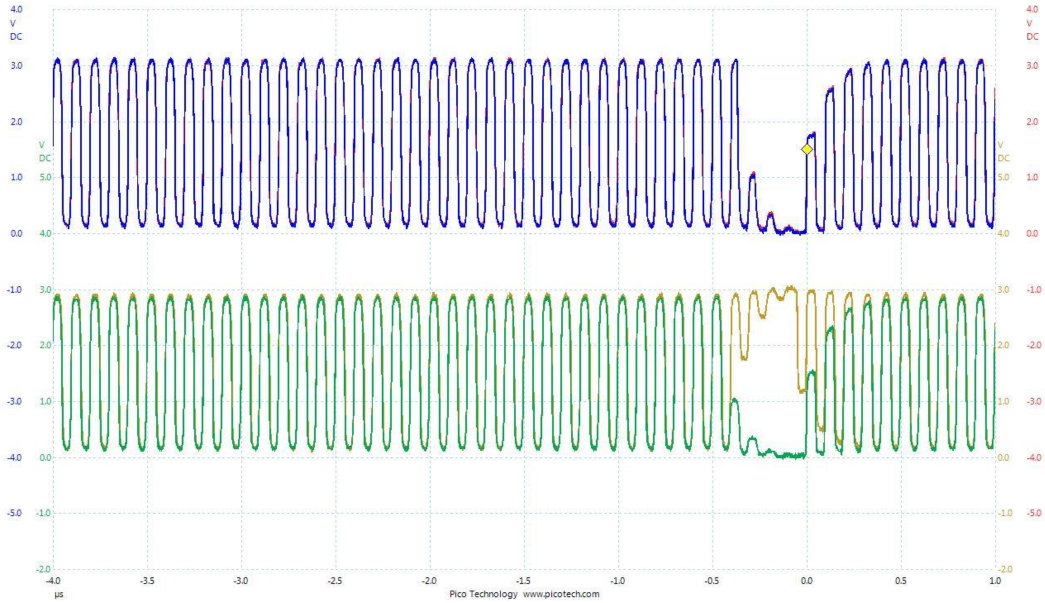

Figure 3-10. ADuM7442 SN17, Run #027, Frame 47 – In-Phase Transients on Outputs A & B, Out of Phase Transients on Outputs C & D.

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4.0 Summary/Conclusions

The SEL testing for the Analog Devices ADuM7442S 1kV Quad-Channel Digital Isolators described in this test report was performed at the LBNL Cyclotron Facility using their 88-Inch Cyclotron and the 10 MeV/n cocktail on December 3, 2015 and March 31, 2016.

No latch-up or other destructive SEE was observed to the highest level tested: LET ≤ 80 MeV·cm^2/mg, 125°C, VDD1 = +5.5V, VDD2 = +5.5V, and 4 samples. Another sample was tested with no latch-up or other destructive SEE observed at an LET 80 MeV·cm^2/mg, 113°C, VDD1 = +5.5V, and VDD2 = +5.5V.

The ADuM7442S has a maximum dropout length of 32 clock cycles with a 10 MHz input. Dropouts occur on all outputs. The LET threshold is ~4 MeV·cm^2/mg with a saturation cross-section of 1.5×10^{-4} cm^2/upset.

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Appendix A: Photographs of a sample device-under-test without the lid to show the various components in the package

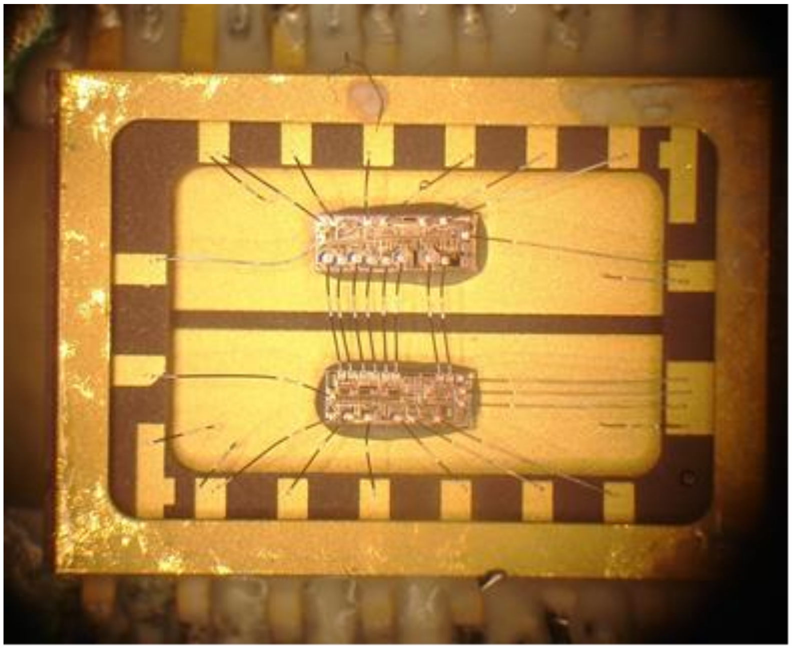

Figure A-1. Delidded Analog Devices ADuM7442S 1kV RMS Quad-Channel Digital Isolators

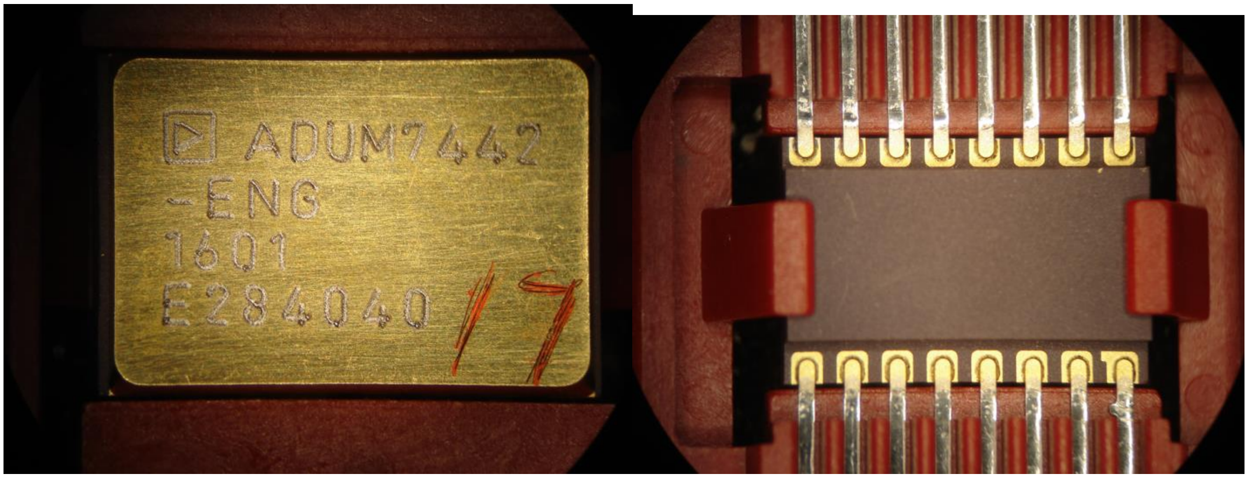

Figure A-2. As Received Analog Devices, ADuM7442S 1kV RMS Quad-Channel Digital Isolators

Appendix B: Photograph of the Test Boards and Electrical Schematics.

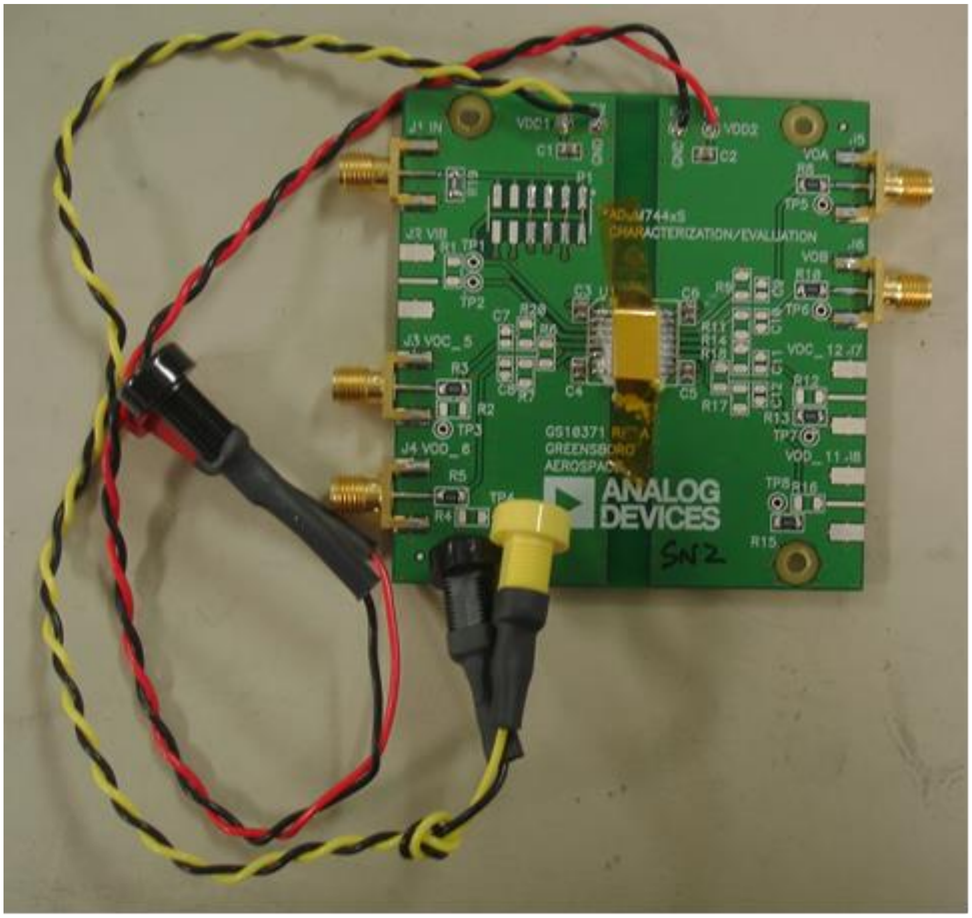

Figure B-1. Photo of the Analog Devices ADuM744xS Characterization/Evaluation Board for SEL Testing

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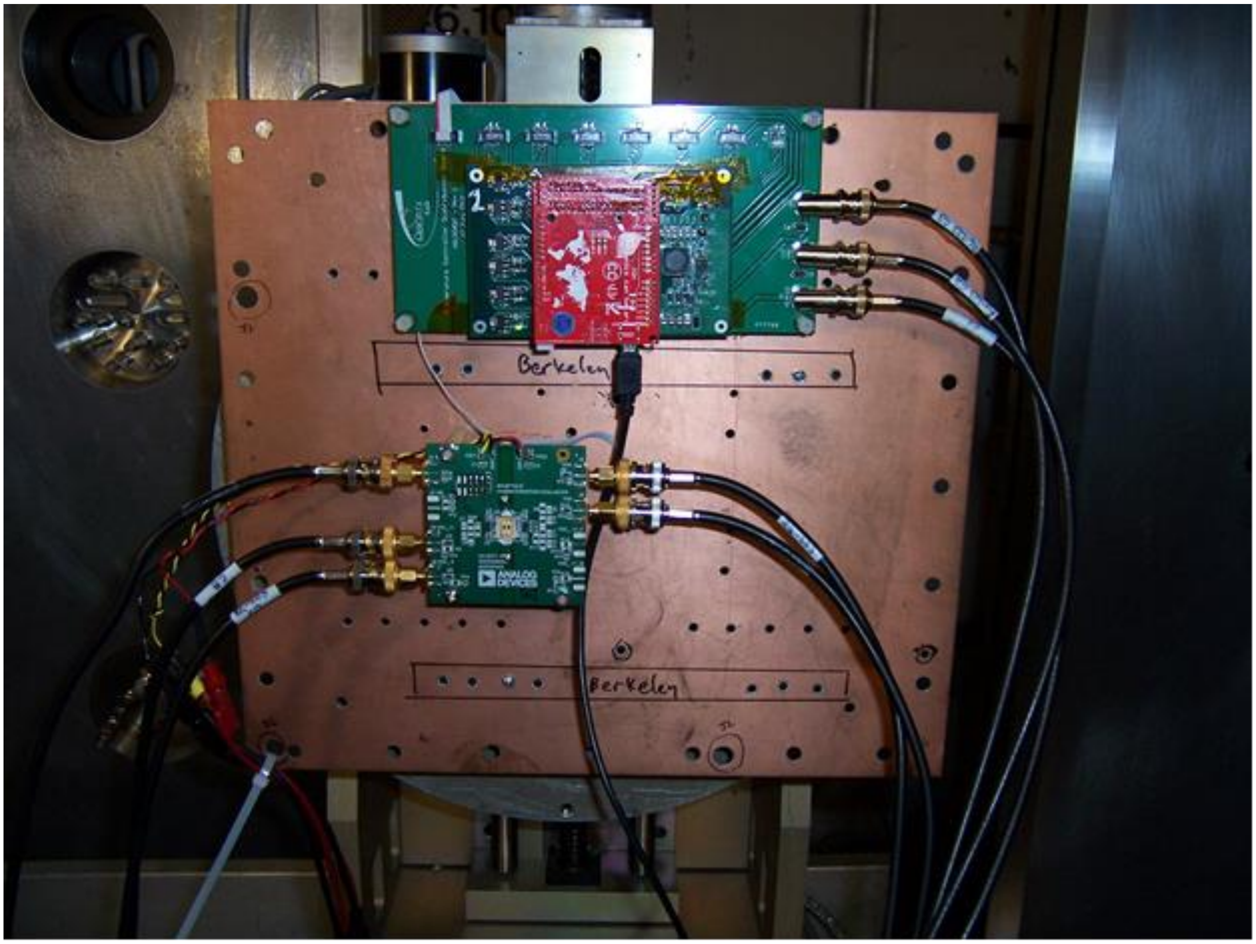

Figure B-2. Photo of the ADuM7442S SEL Test Setup in the Vacuum Chamber

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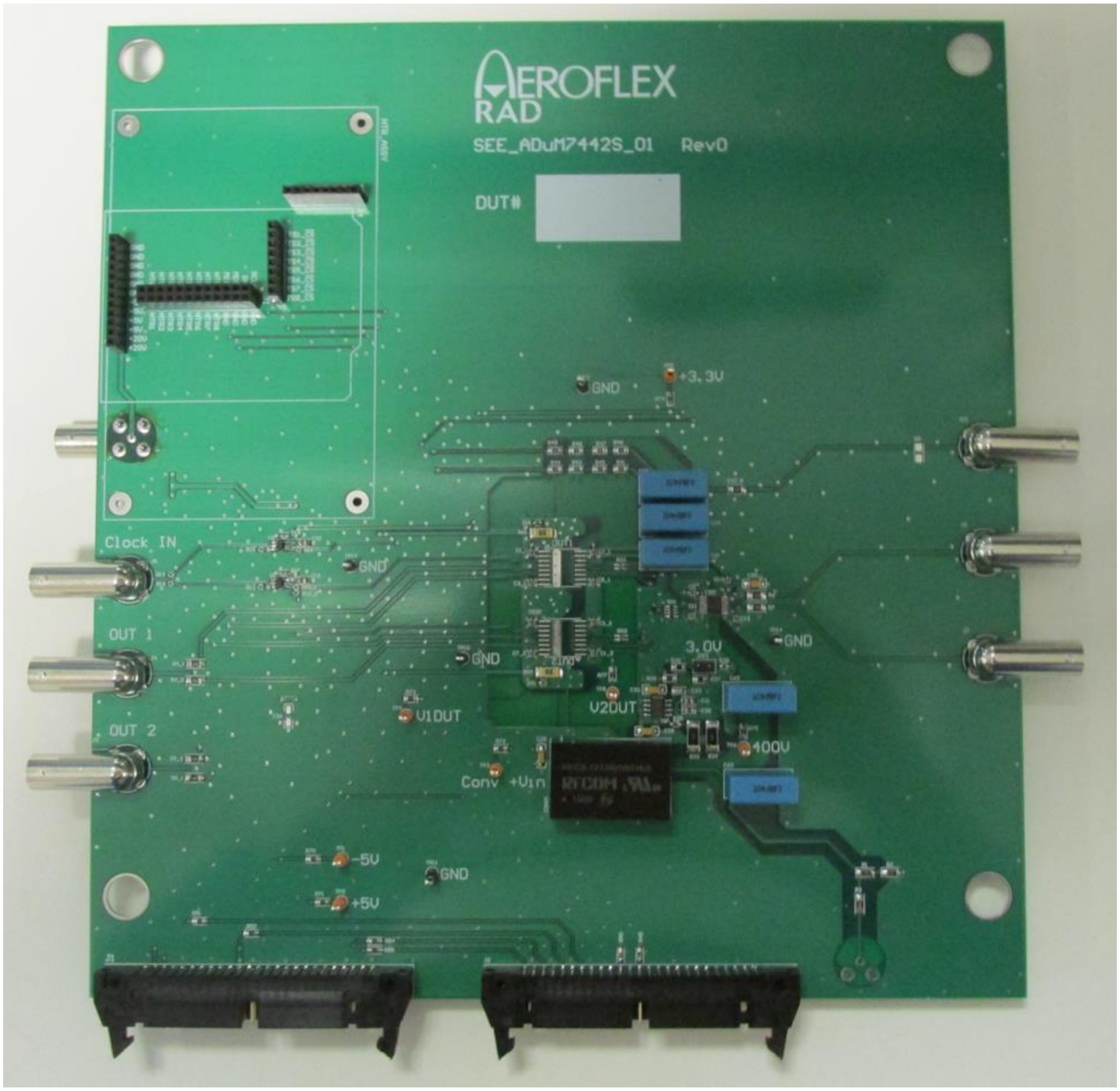

Figure B-3. Photo of ADuM7442S Test Board for SET Testing

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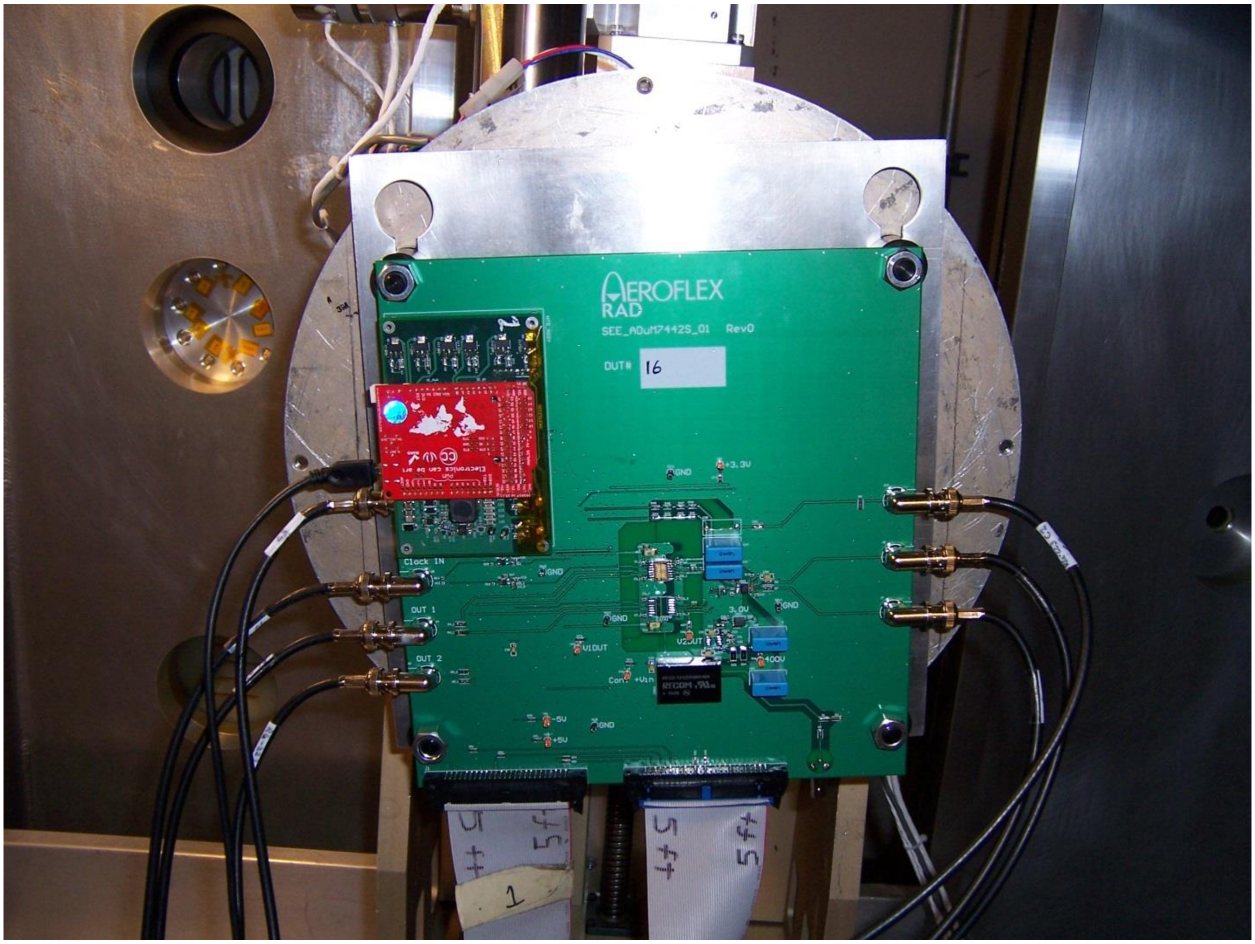

Figure B-4. Photo of the ADuM7442S SET Test Setup in the Vacuum Chamber

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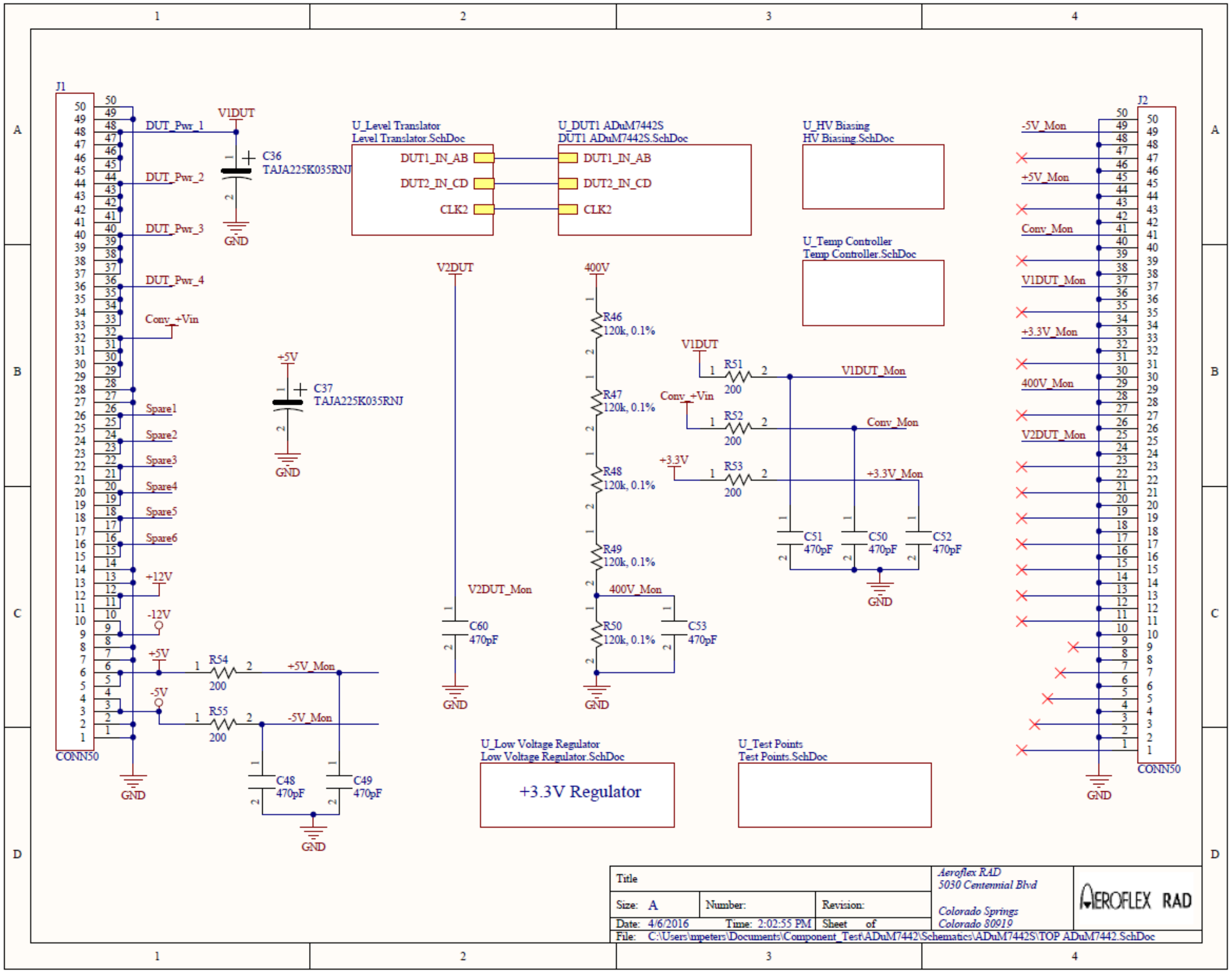

Figure B-5. ADuM7442S Test Board Top Level Schematic (1 of 8)

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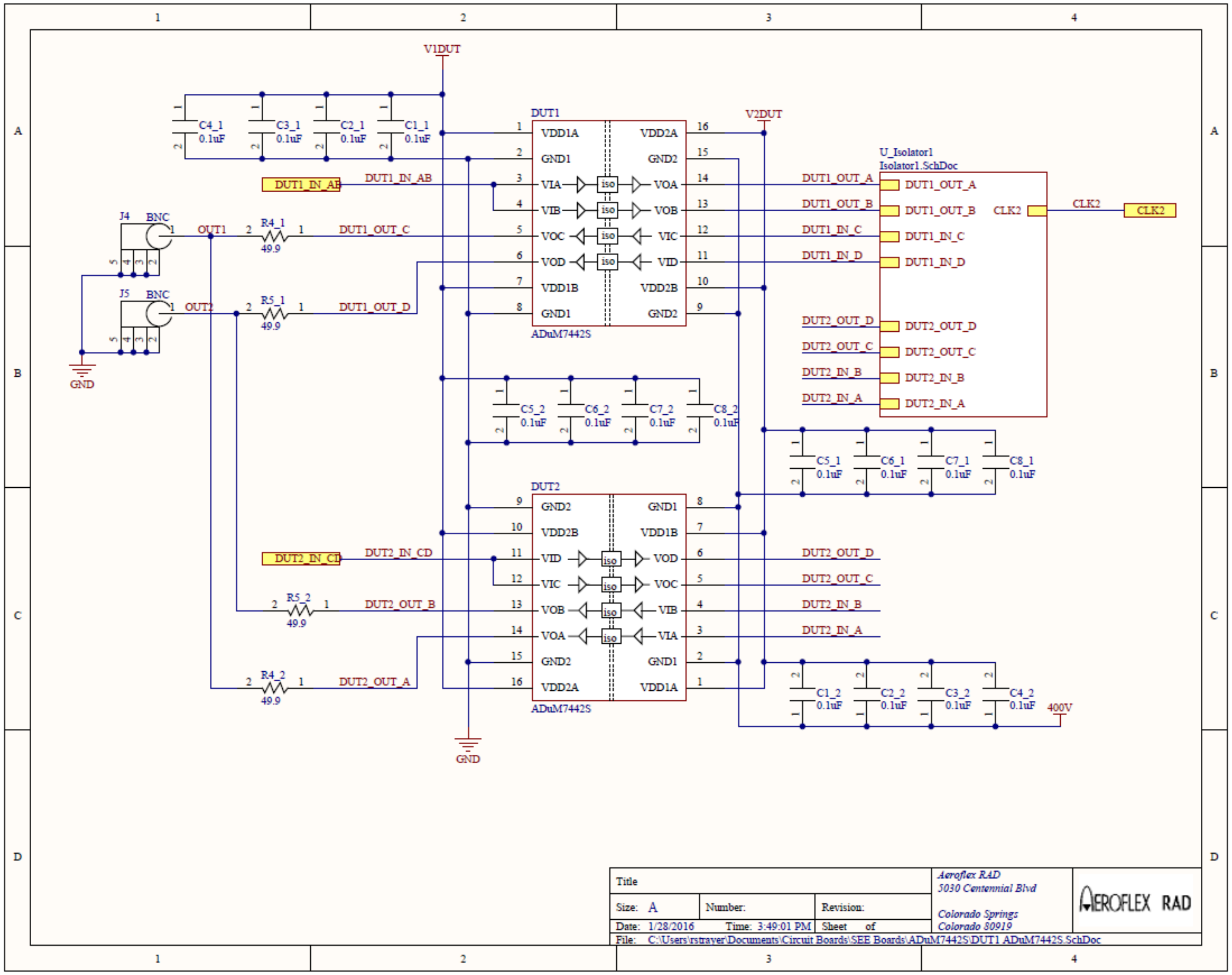

Figure B-6. ADuM7442S DUT Circuit (2 of 8)

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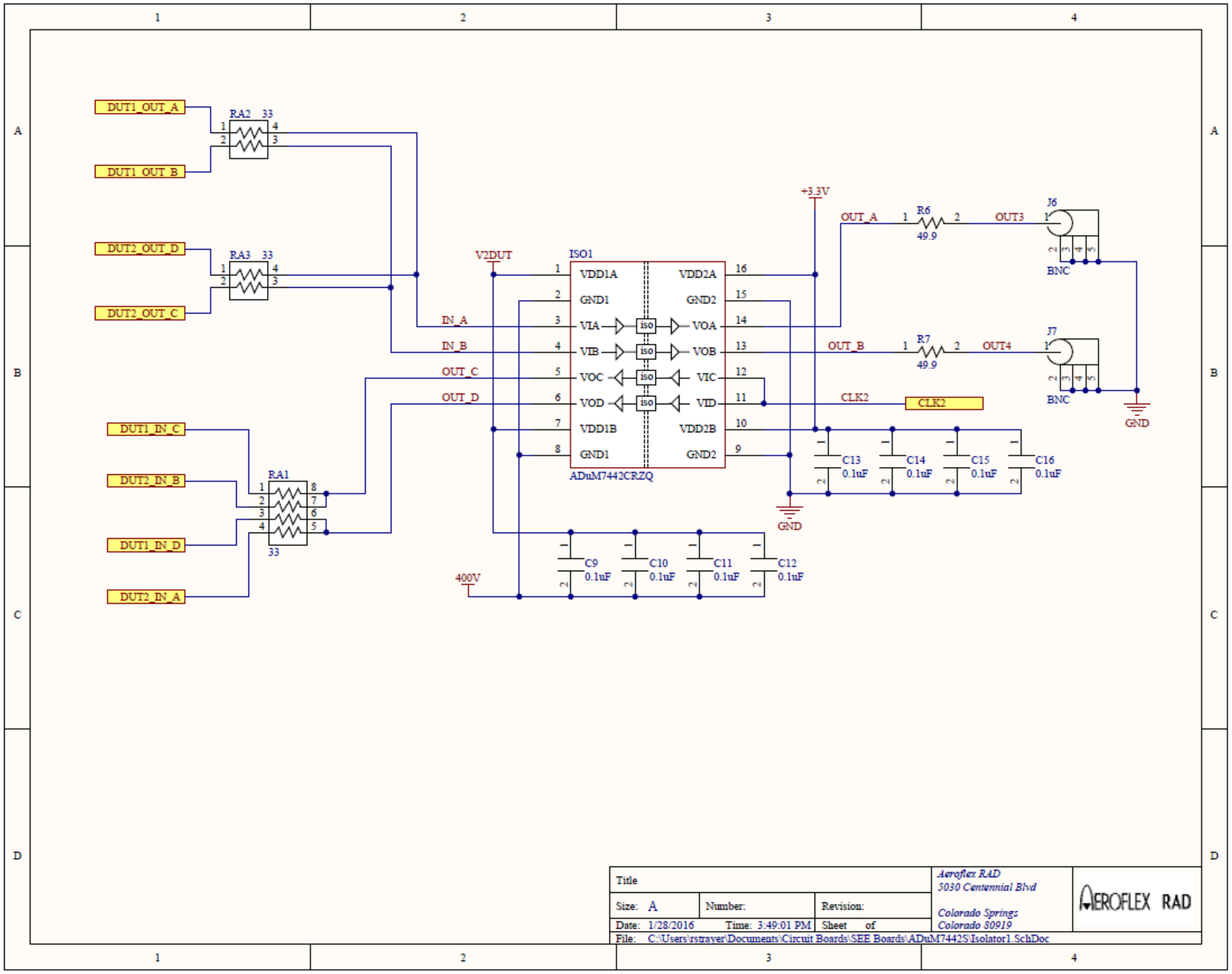

Figure B-7. ADuM7442S Isolators Circuit (3 of 8)

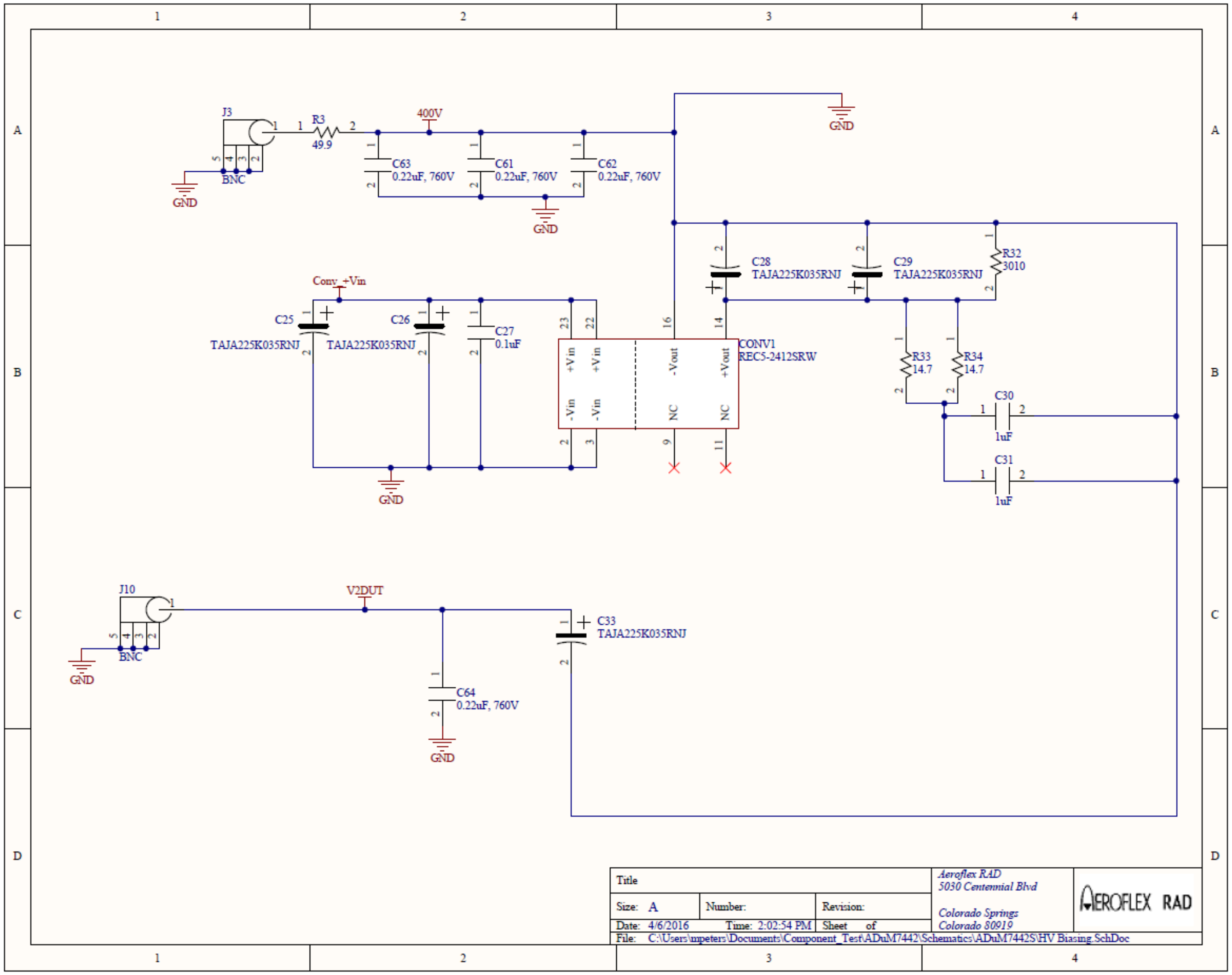

Figure B-8. High Voltage Biasing Circuit (4 of 8)

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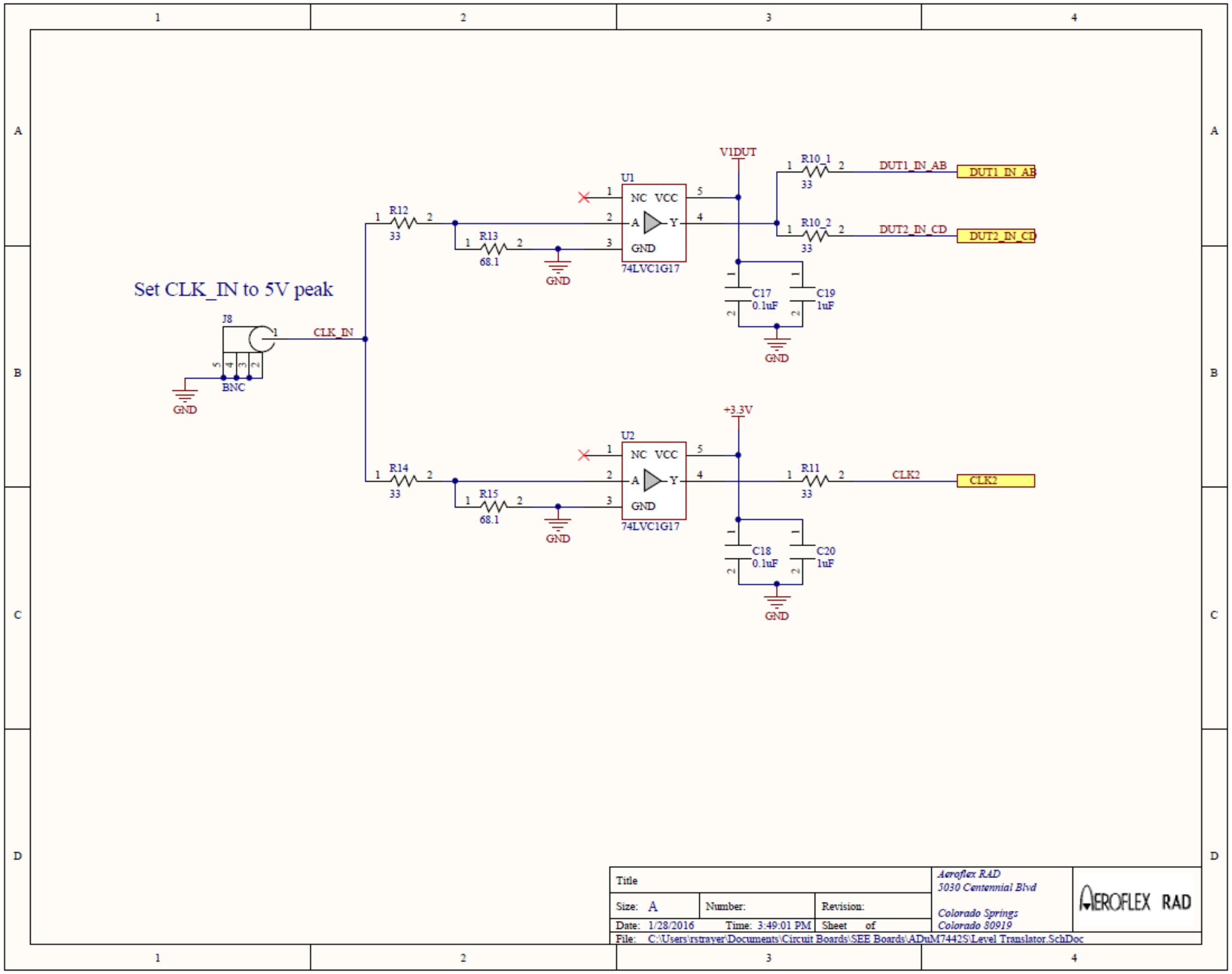

Figure B-9. Clock Input Level Translator Circuit (5 of 8)

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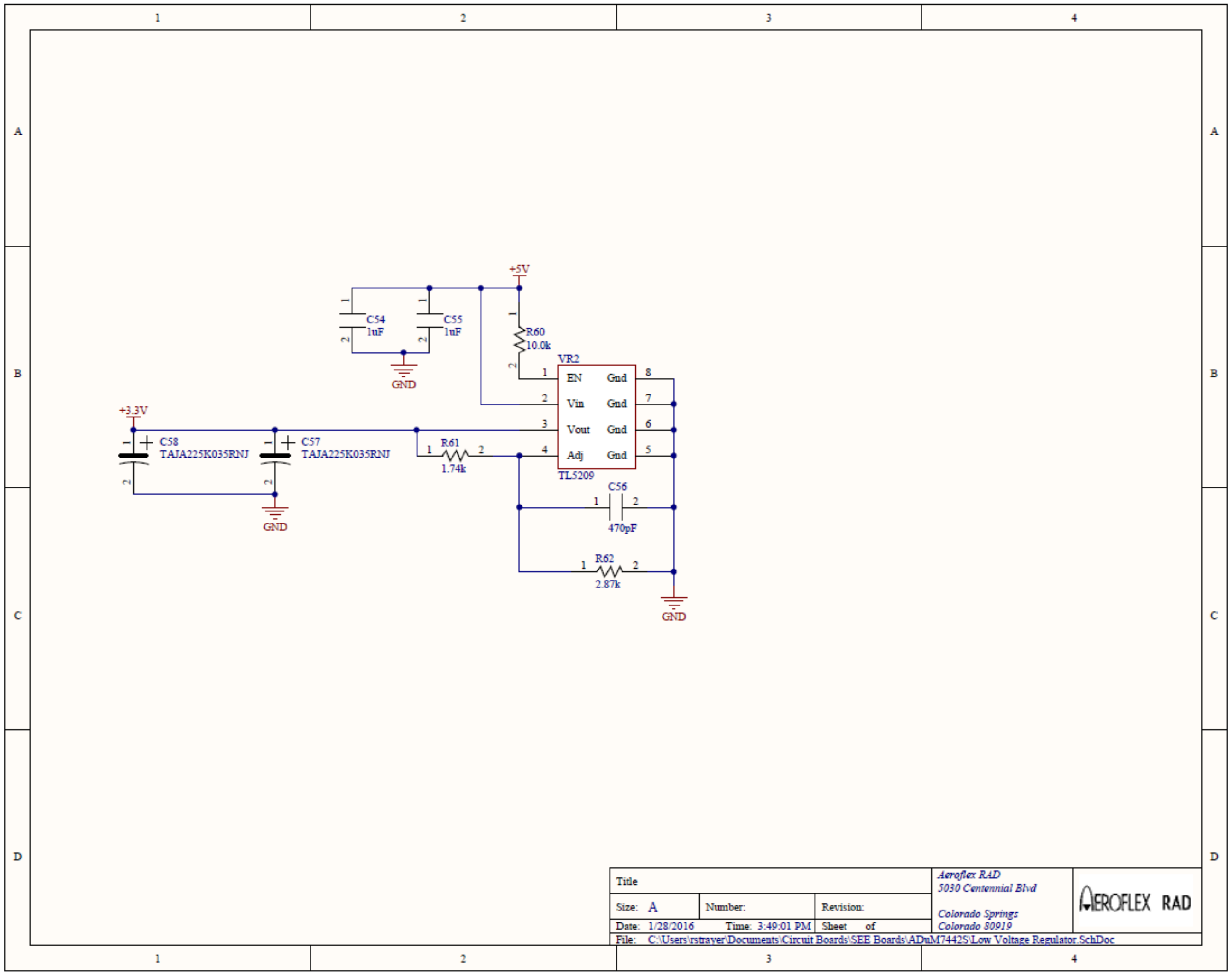

Figure B-10. +3.3 Volt Regulator Circuit (6 of 8)

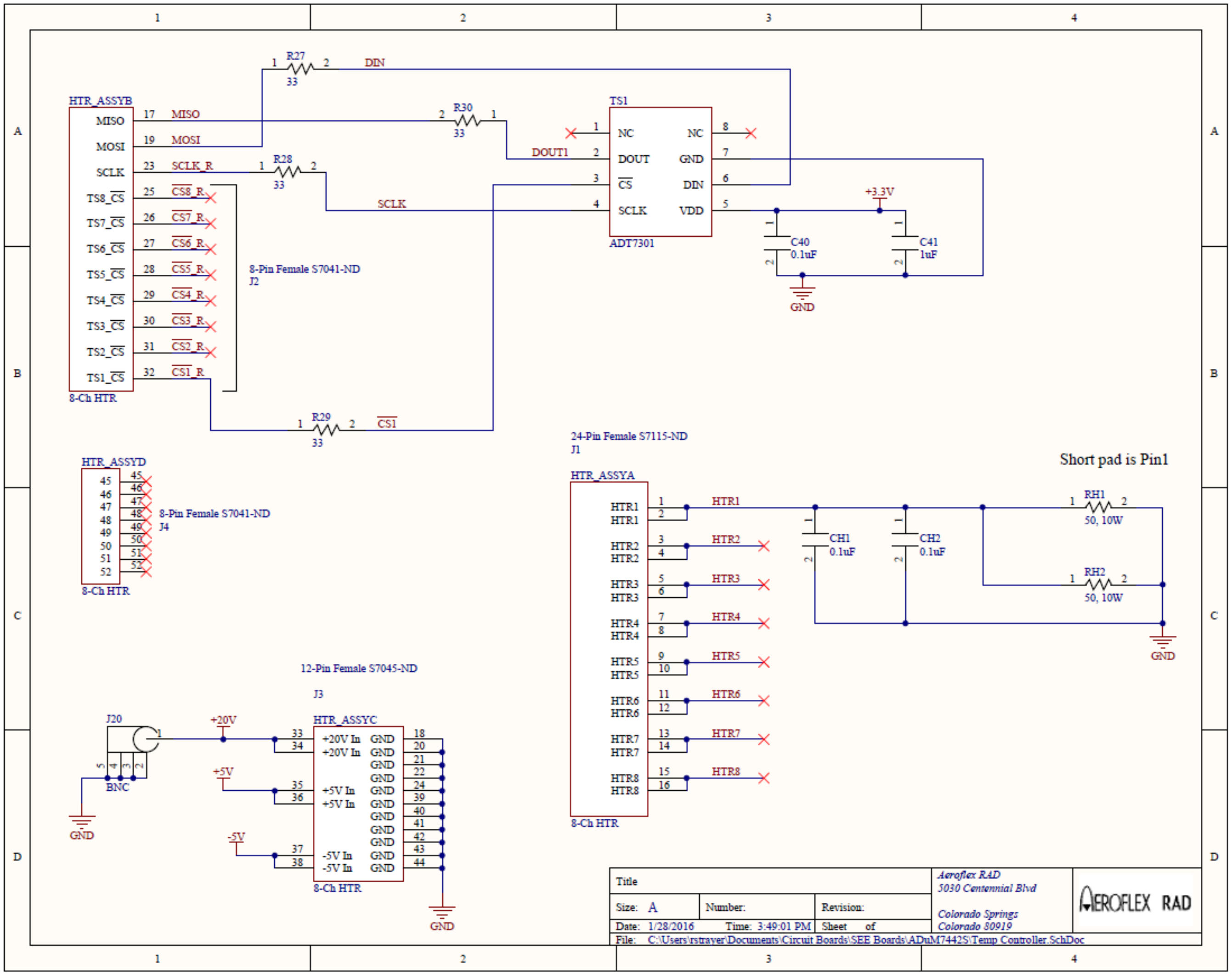

Figure B-11. Temperature Controller Circuit (7 of 8)

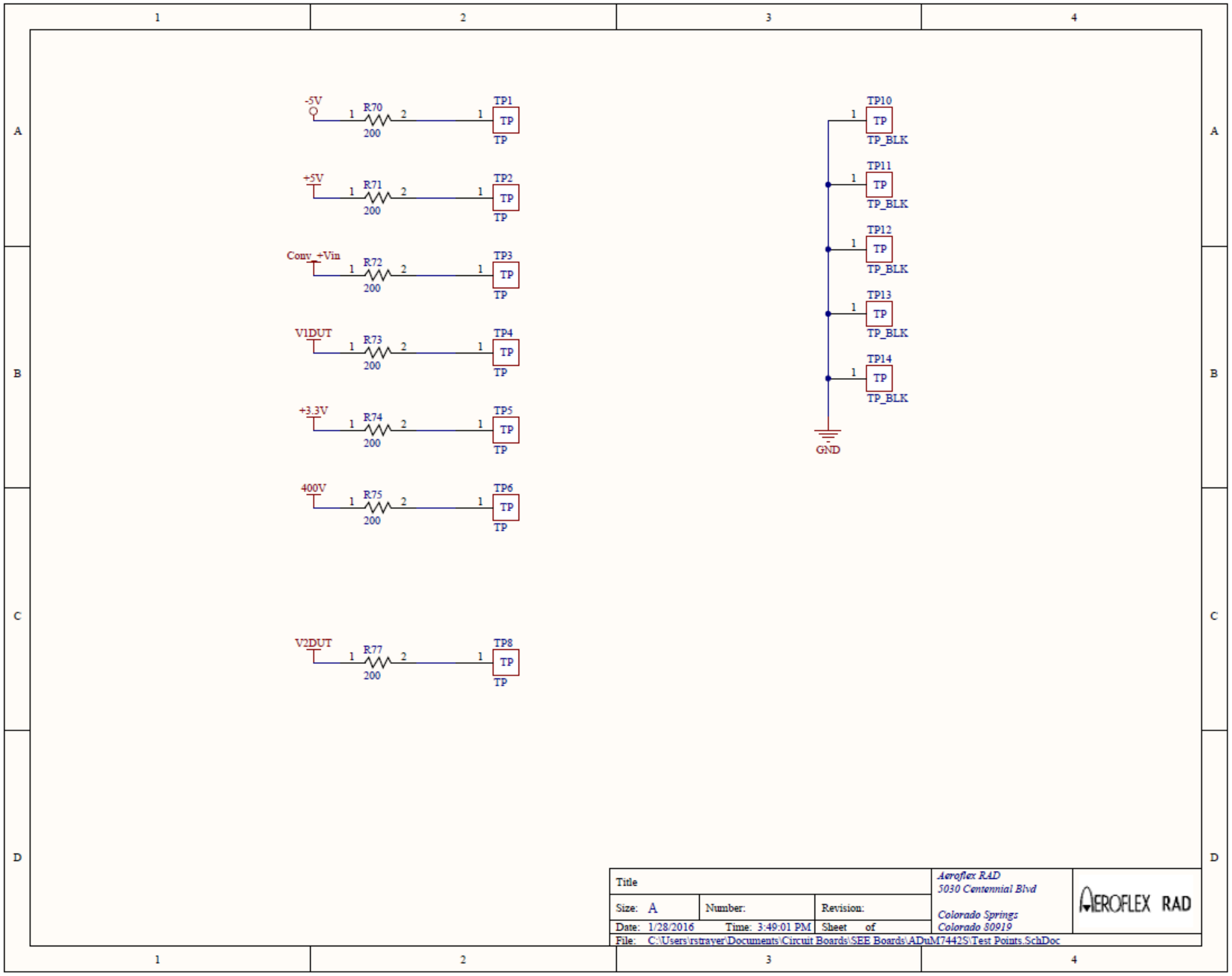

Figure B-12. Test Points (8 of 8)

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Appendix C: Electrical Test Parameters and Equipment List:

Table C-1 lists the equipment used during the testing as well as the calibration dates and the date the calibration is due.

Table C-1. Test Equipment List and Calibration Dates.

Equipment	Entity Number	Calibration Date	Calibration Due	Purpose
Keithley 2410 Source Meter	TS29	04/07/2015	04/07/2016	VDD1 Power Supply and Current Measurement
Keithley 2420 Source Meter	TS27	04/15/2015	04/15/2016	VDD2 and V1DUT Power Supply and Current Measurement
Keithley 2425 Source Meter	TS26	06/05/2015	06/05/2016	V2DUT Power Supply and Current Measurement
Instek AFG-2125 Generator	SG19	11/17/2015	11/17/2016	Clock Input Test Signal
PicoScope 6404D Oscilloscope	OS16	04/29/2015	04/29/2016	Measure Test Output Signals
Agilent 34970A Data Aquistion Unit	DA01	08/25/2015	08/25/2016	DUT Voltage Measurements
Agilent 34901A Multiplexer	MP01	08/25/2015	08/25/2016	DUT Voltage Measurements
Fluke 115 True RMS Multimeter	HM17	07/01/2015	07/01/2016	Voltage Measurements
Housekeeping Power Supply		NA	NA	+/-5 Volt and +24 Volt Power Supplies
Fluke 51II Thermometer	TM03	07/31/2015	07/31/2016	Sensor Temperature Calibration
Thermocouple	TC17	02/04/2016	02/04/2017	Sensor Temperature Calibration

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Appendix D: Single Event Effects Apparatus

The single event effects testing discussed in this test report was performed at the Lawrence Berkeley National Laboratories Cyclotron Facility using their 88-Inch Cyclotron. For the single event transient testing performed at LBNL the devices were placed in the Cave 4B vacuum chamber aligned with the heavy ion beam line. The test platter in the vacuum chamber has full horizontal and vertical alignment capabilities along with 2-dimensional rotation, allowing for a variety of effective LETs for each ion. For SEE testing Lawrence Berkeley Laboratories provides the dosimetry via a local control computer running a Lab View based program. Each ion is calibrated just prior to use using five photomultiplier tubes (PMTs). Figure 2-1 shows an illustration of the LBL facility; including the location of Cave 4B, where the heavy ion SEE testing takes place. Table 2-1 shows the beam characteristics available at Berkeley.

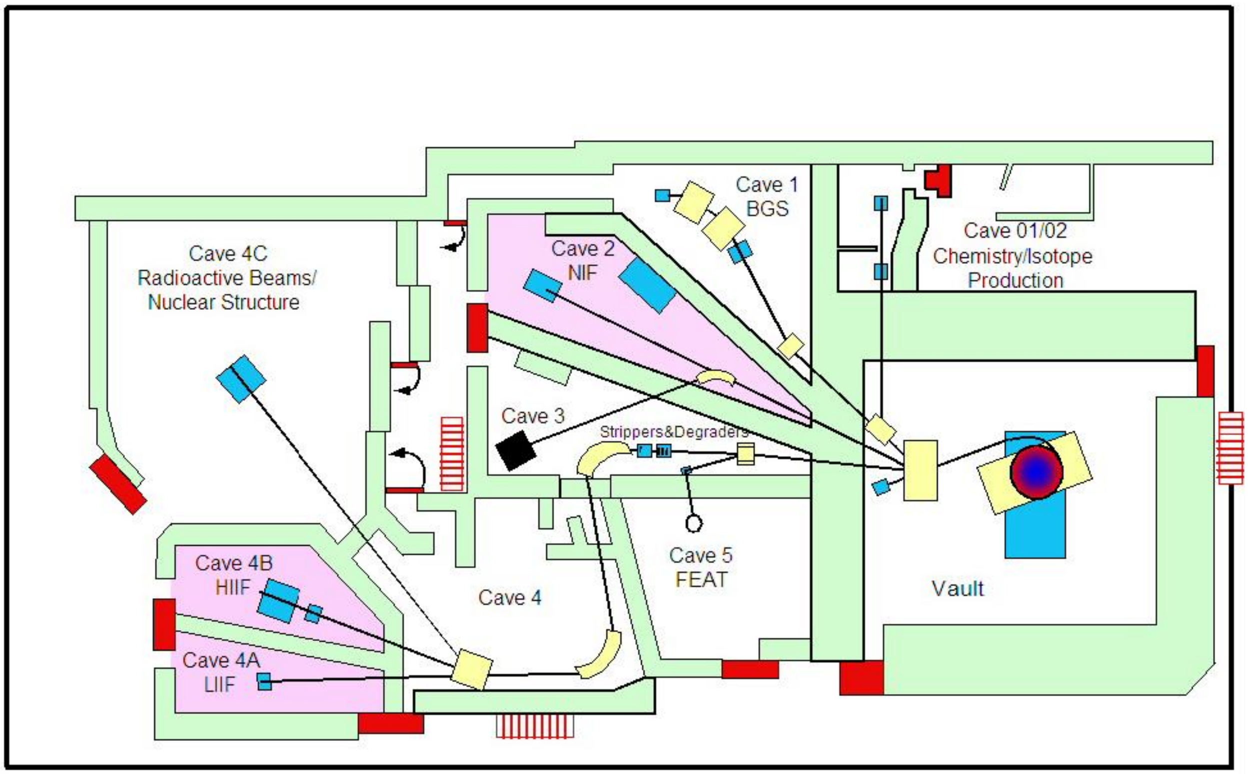

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Table D-1. Typical ions and LETs that may be used during SEE testing.

Ion	Cocktail (MeV/nuc)	Energy (MeV)	Z	A	Chg. State	% Nat. Abund.	LET 0° (MeV/(mg/cm^2))	LET 60° (MeV/(mg/cm^2))	Range (µm)	Method
B	4.5	44.90	5	10	+2	19.9	1.65	3.30	78.5	MIVOC
N	4.5	67.44	7	15	+3	0.37	3.08	6.16	67.8	Gas
Ne	4.5	89.95	10	20	+4	90.48	5.77	11.54	53.1	Gas
Si[1]	4.5	139.61	14	29	+6	4.67	9.28	18.56	52.4	Gas
Ar	4.5	180.00	18	40	+8	99.6	14.32	28.64	48.3	Gas
V	4.5	221.00	23	51	+10	99.75	21.68	43.36	42.5	Probe
Cu	4.5	301.79	29	63	+13	69.17	29.33	58.66	45.6	Probe
Kr	4.5	387.08	36	84	+17	17.3	38.96	77.92	48.0	Gas
Y	4.5	409.58	39	89	+18	100	45.58	91.16	45.8	Probe
Ag	4.5	499.50	47	109	+22	48.161	58.18	116.36	46.3	Probe
Xe	4.5	602.90	54	136	+27	8.9	68.84	137.68	48.3	Gas
Tb	4.5	724.17	65	159	+32	100	77.52	155.04	52.4	Probe
Ta	4.5	805.02	73	181	+36	99.988	87.15	174.30	53.0	Probe
Bi	4.5	904.16	83	209	+41	100	99.74	199.48	52.9	Oven
B	10	108.01	5	11	+3	80.1	0.89	1.78	305.7	MIVOC
O	10	183.47	8	18	+5	0.2	2.19	4.38	226.4	Gas
Ne	10	216.28	10	22	+6	9.25	3.49	6.98	174.6	Gas
Si[1]	10	291.77	14	29	+8	4.67	6.09	12.18	141.7	Gas
Ar	10	400.00	18	40	+11	99.6	9.74	19.48	130.1	Gas
V	10	508.27	23	51	+14	99.75	14.59	29.18	113.4	Probe
Cu	10	659.19	29	65	+18	30.83	21.17	42.34	108.0	Probe
Kr	10	906.45	36	84	+24	57	30.23	60.46	113.1	Gas
Y	10	928.49	39	89	+25	100	34.73	69.46	102.2	Probe
Ag	10	1039.42	47	107	+29	51.839	48.15	96.30	90.0	Probe
Xe	10	1232.55	54	124	+34	0.1	58.78	117.56	90.0	Gas
N	16	233.75	7	14	+5	99.63	1.16	2.32	505.9	Gas
O	16	277.33	8	17	+6	0.04	1.54	3.08	462.4	Gas
Ne	16	321.00	10	20	+7	90.48	2.39	4.78	347.9	Gas
Si[1]	16	452.10	14	29	+10	4.67	4.56	9.12	274.3	Gas
Cl	16	539.51	17	35	+12	75.77	6.61	13.22	233.6	Natural
Ar	16	642.36	18	40	+14	99.600	7.27	14.54	255.6	Gas
V	16	832.84	23	51	+18	99.750	10.90	21.80	225.8	Probe
Cu	16	1007.34	29	63	+22	69.17	16.53	33.06	190.3	Probe
Kr	16	1225.54	36	78	+27	0.35	24.98	49.96	165.4	Gas
Xe	16	1954.71	54	124	+43	0.1	49.29	98.58	147.9	Gas
N	30	425.45	7	15	+7	0.37	0.76	1.52	1370.0	Gas
O	30	490.22	8	17	+8	0.04	0.98	1.96	1220.0	Gas
Ne	30	620.00	10	21	+10	0.27	1.48	2.96	1040.0	Gas
Ar	30	1046.11	18	36	+17	0.337	4.87	9.74	578.1	Gas

[1]By Special request

Appendix E: SEL Current Plots

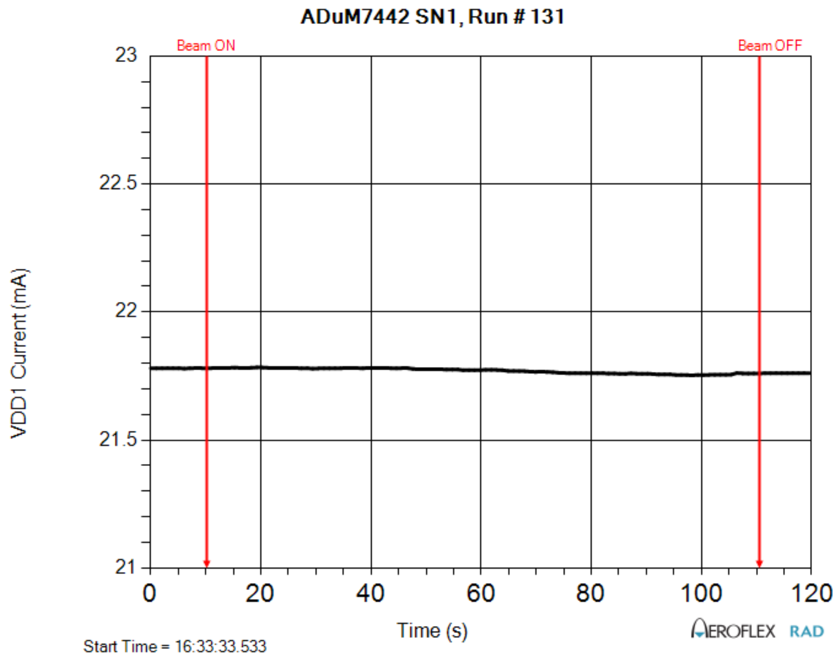

Figure E-1. ADuM7442 SN1, Run #131, DUT VDD1 Current (mA).

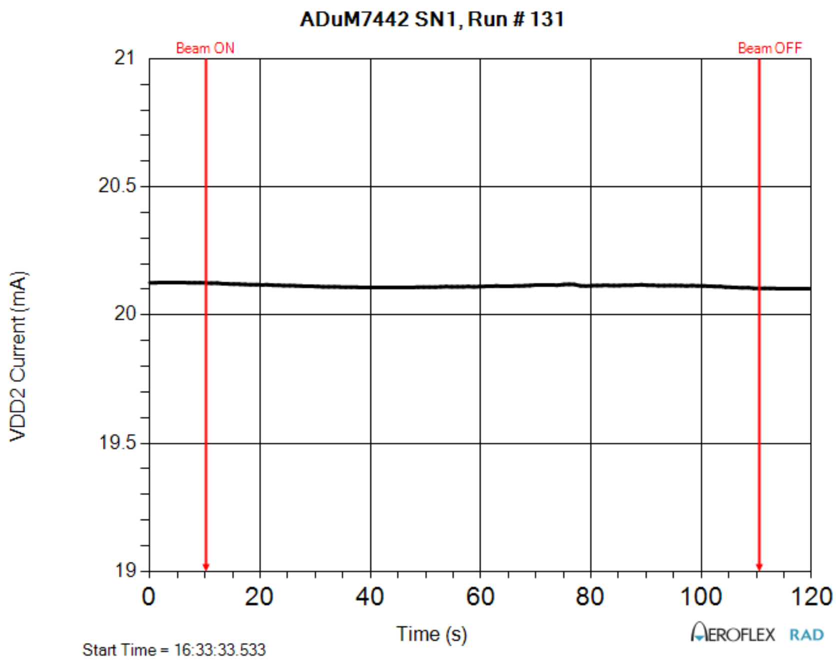

Figure E-2. ADuM7442 SN1, Run #131, DUT VDD2 Current (mA).

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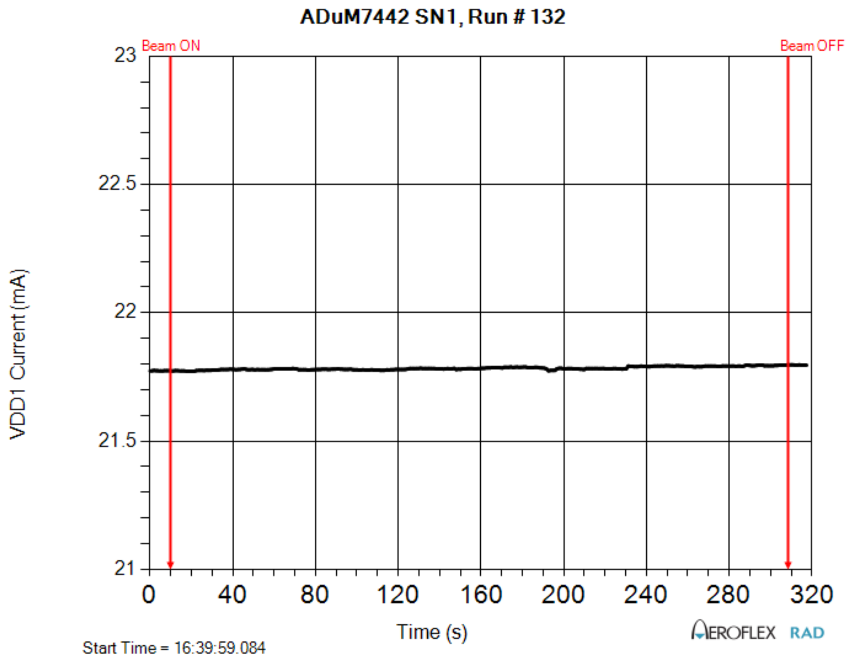

Figure E-3. ADuM7442 SN1, Run #132, DUT VDD1 Current (mA).

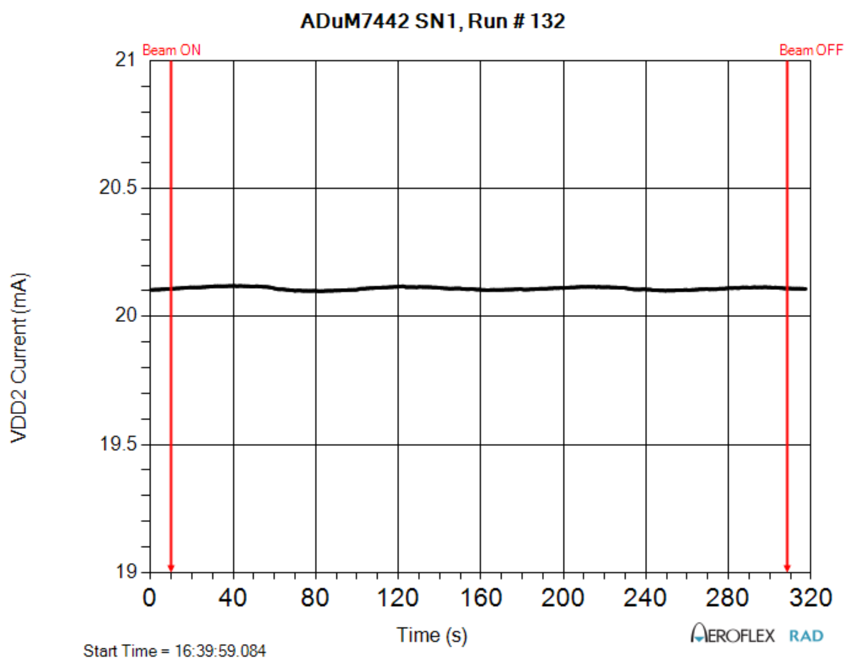

Figure E-4. ADuM7442 SN1, Run #132, DUT VDD2 Current (mA).

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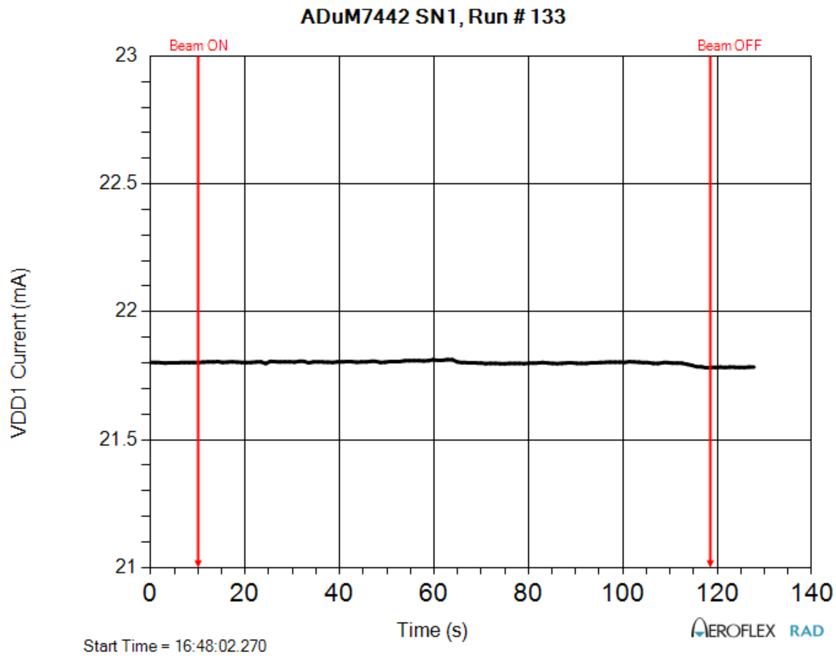

Figure E-5. ADuM7442 SN1, Run #133, DUT VDD1 Current (mA).

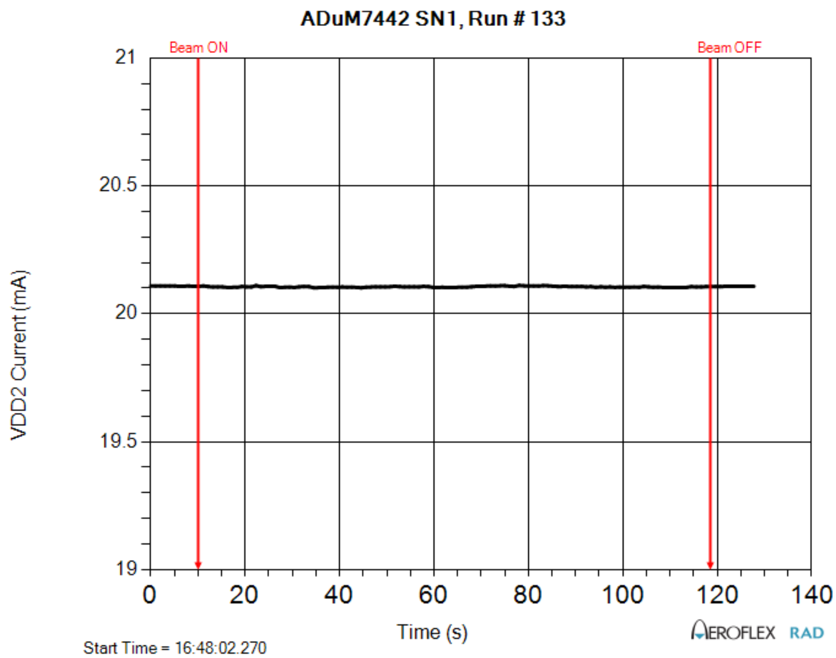

Figure E-6. ADuM7442 SN1, Run #133, DUT VDD2 Current (mA).

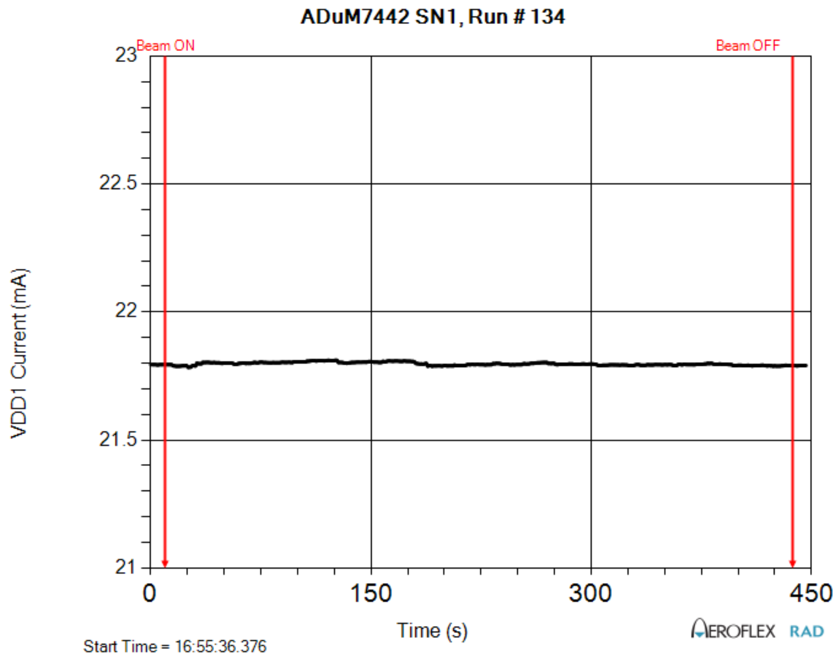

Figure E-7. ADuM7442 SN1, Run #134, DUT VDD1 Current (mA).

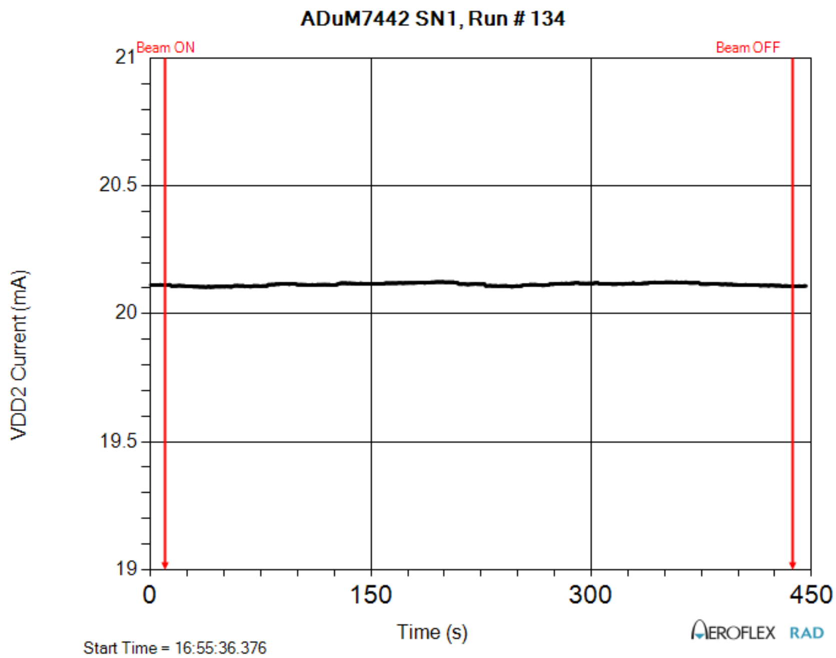

Figure E-8. ADuM7442 SN1, Run #134, DUT VDD2 Current (mA).

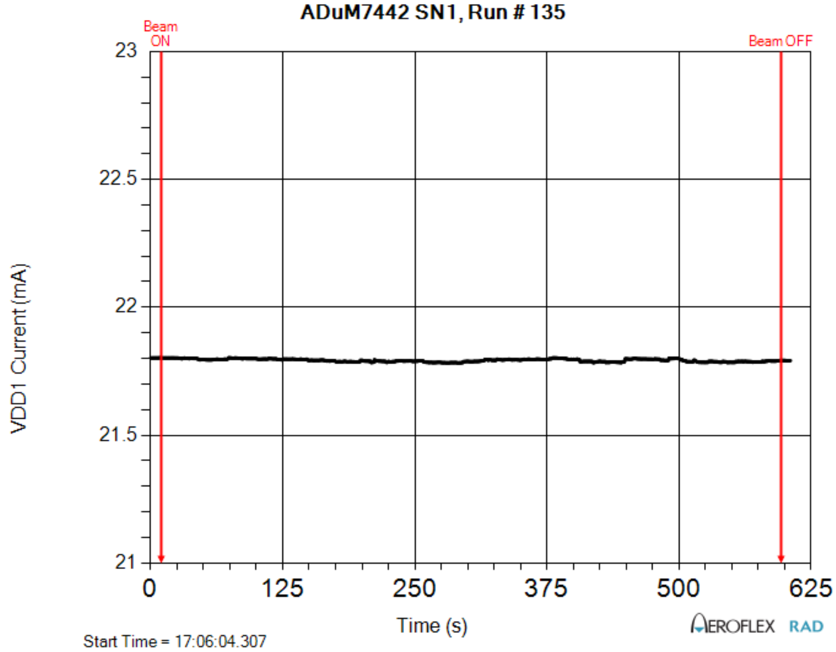

Figure E-9. ADuM7442 SN1, Run #135, DUT VDD1 Current (mA).

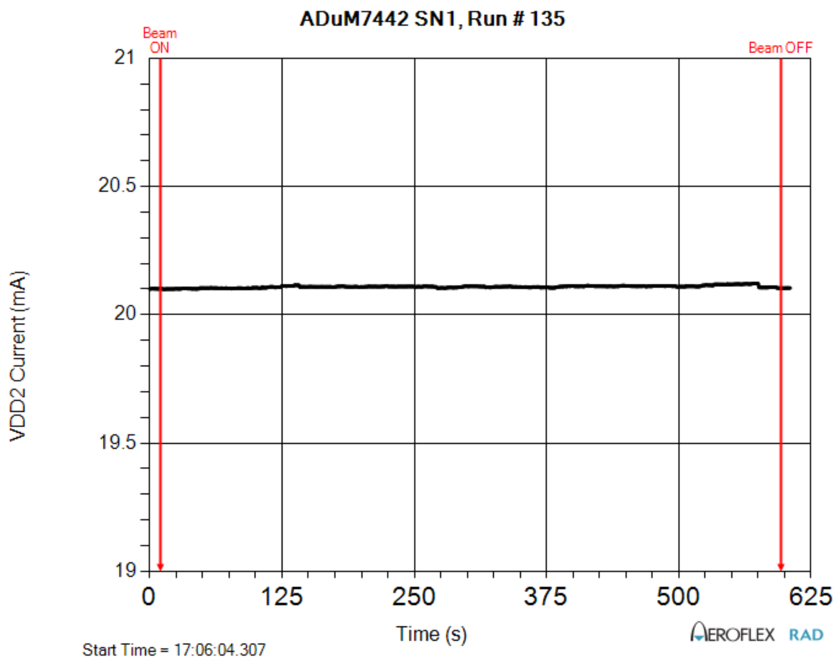

Figure E-10. ADuM7442 SN1, Run #135, DUT VDD2 Current (mA).

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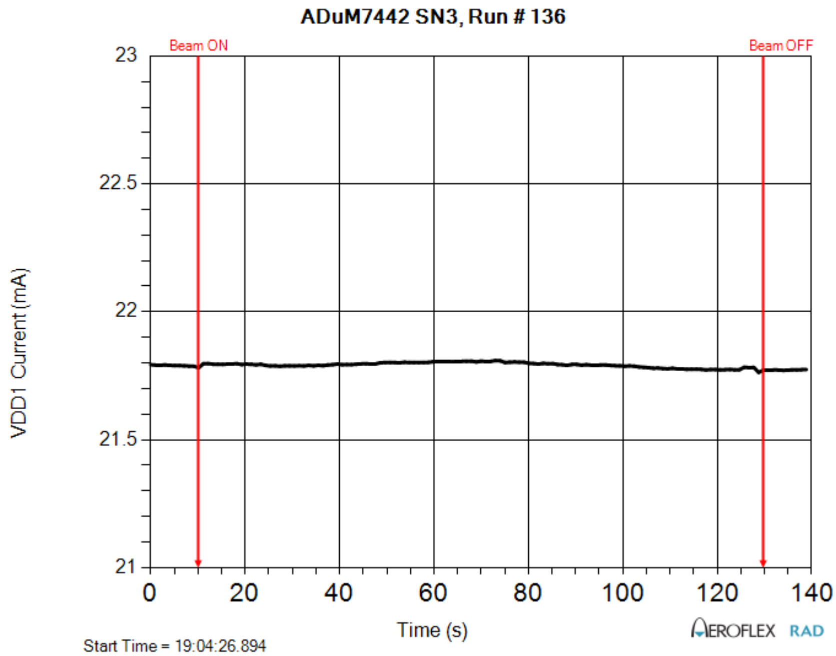

Figure E-11. ADuM7442 SN3, Run #136, DUT VDD1 Current (mA).

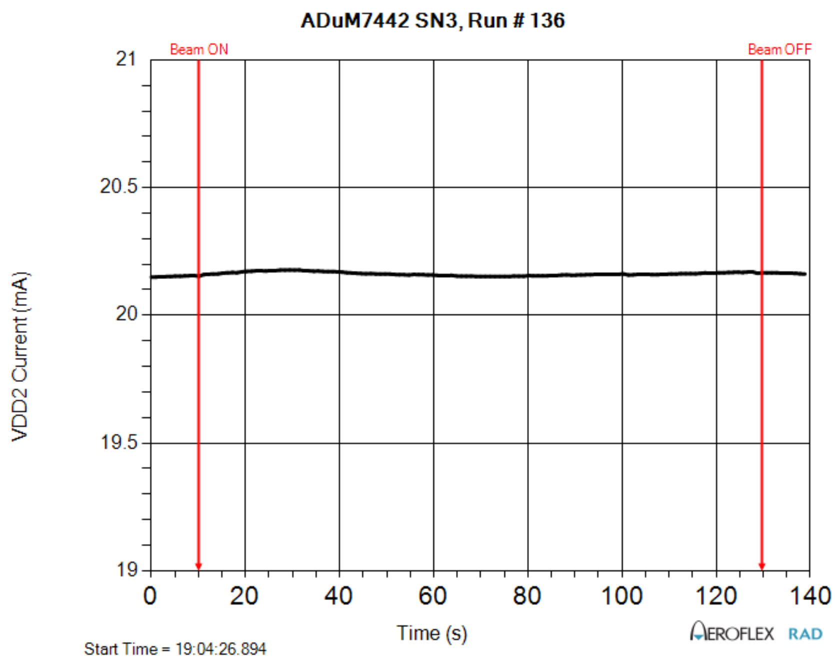

Figure E-12. ADuM7442 SN3, Run #136, DUT VDD2 Current (mA).

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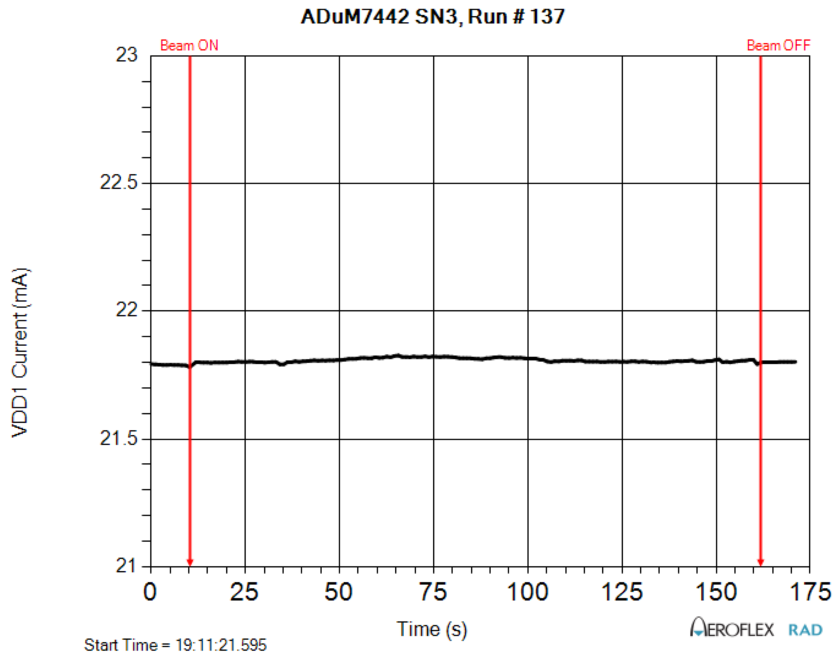

Figure E-13. ADuM7442 SN3, Run #137, DUT VDD1 Current (mA).

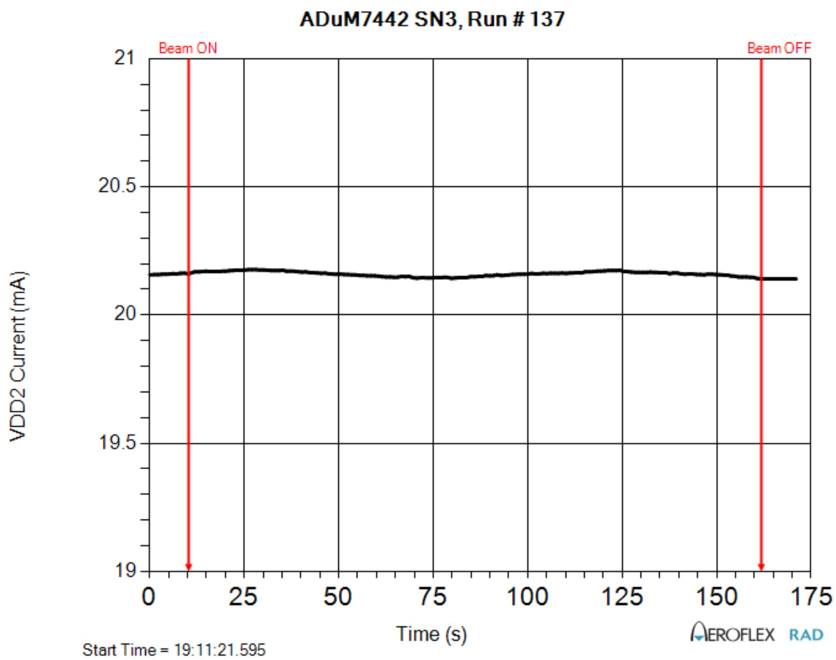

Figure E-14. ADuM7442 SN3, Run #137, DUT VDD2 Current (mA).

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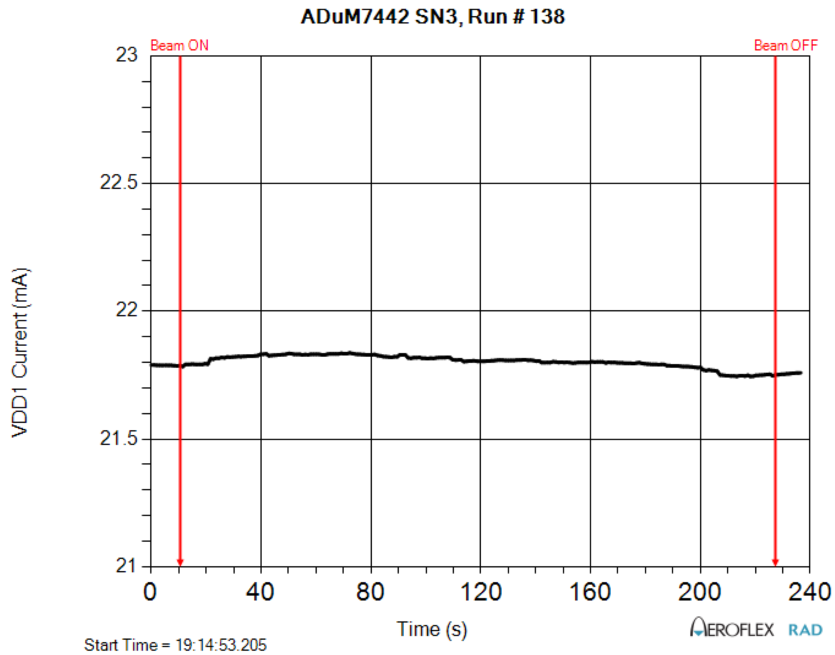

Figure E-15. ADuM7442 SN3, Run #138, DUT VDD1 Current (mA).

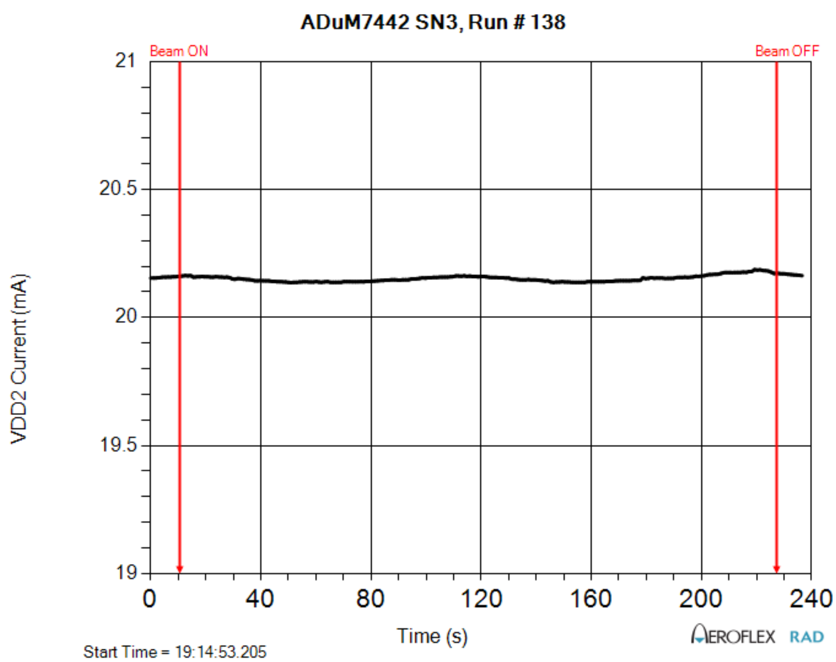

Figure E-16. ADuM7442 SN3, Run #138, DUT VDD2 Current (mA).

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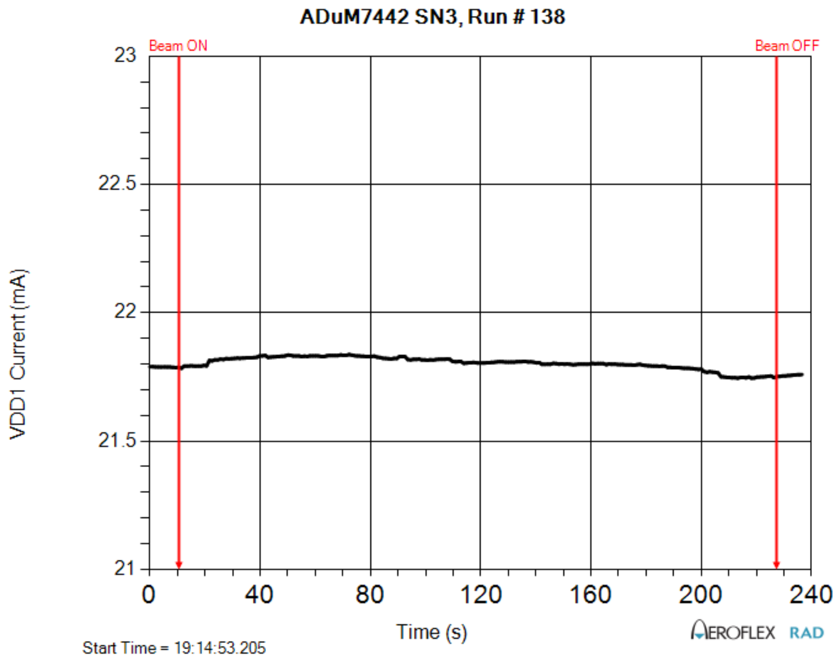

Figure E-17. ADuM7442 SN3, Run #139, DUT VDD1 Current (mA).

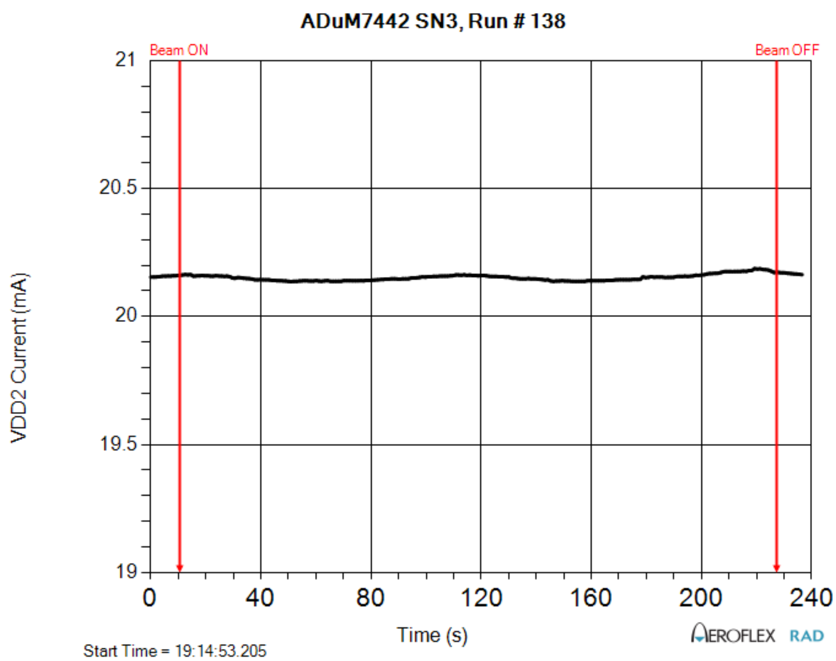

Figure E-18. ADuM7442 SN3, Run #139, DUT VDD2 Current (mA).

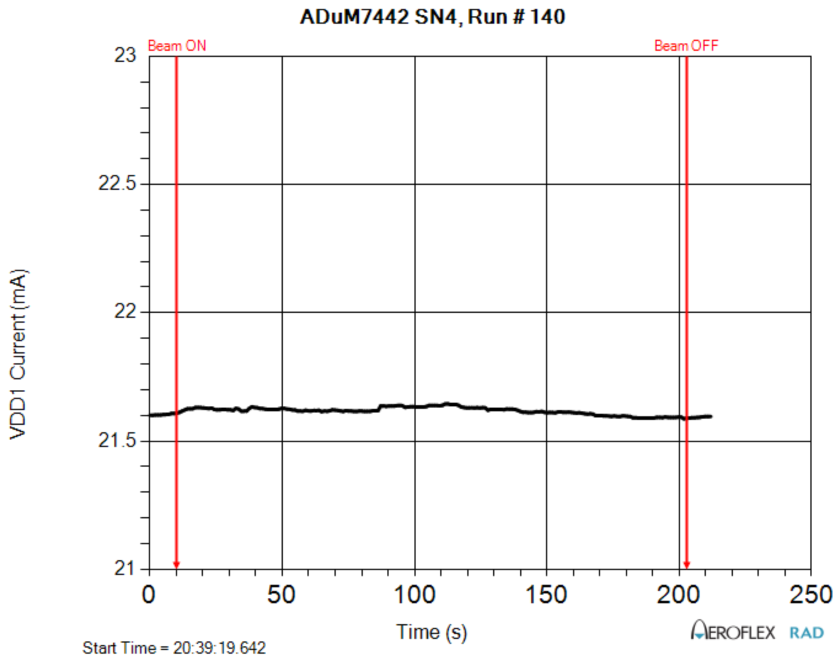

Figure E-19. ADuM7442 SN4, Run #140, DUT VDD1 Current (mA).

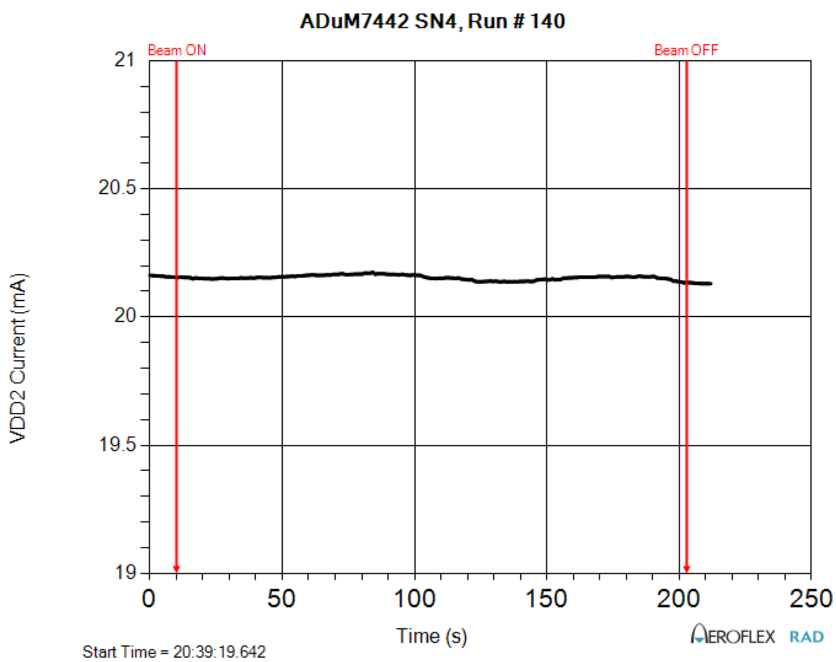

Figure E-20. ADuM7442 SN4, Run #140, DUT VDD2 Current (mA).

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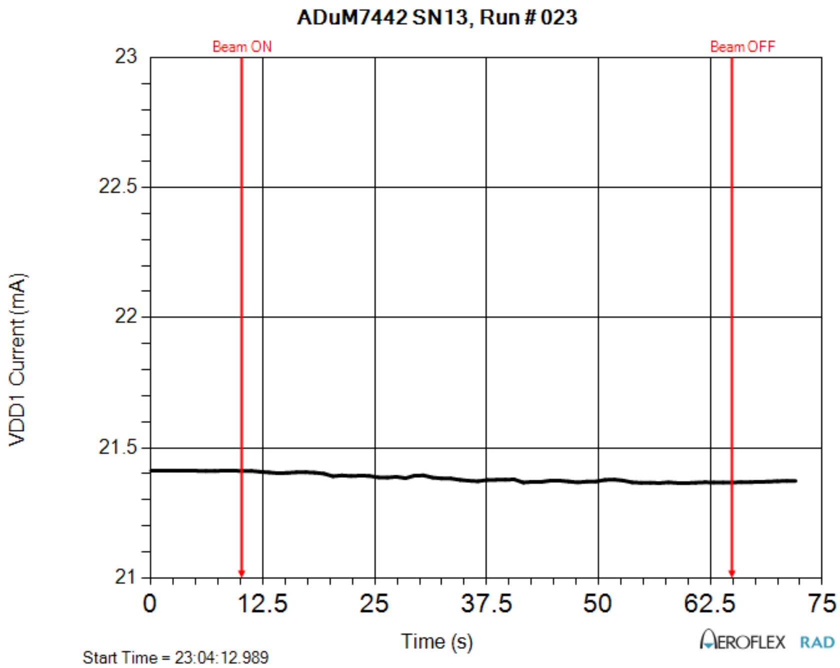

Figure E-21. ADuM7442 SN13, Run #23, DUT VDD1 Current (mA).

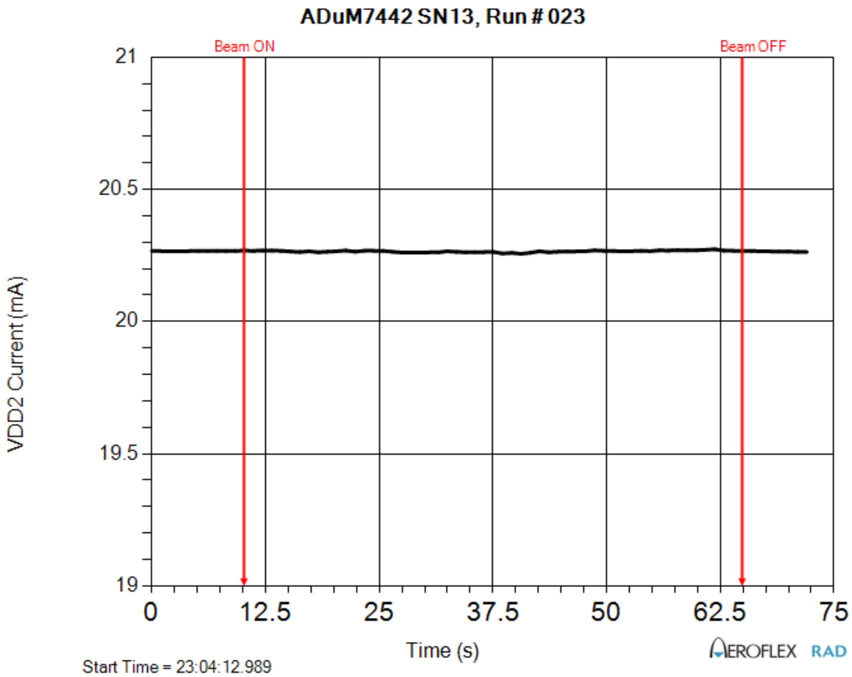

Figure E-22. ADuM7442 SN13, Run #23, DUT VDD2 Current (mA).