New Features in the ADV601 Video Codec Family

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OVERVIEW

The ADV601JS12, ADV601LC and ADV611 and ADV612 video codecs contain all the features of the original ADV601. They also have new features, described below that will make the chips easier to design with and will shorten the development cycle. ADV601JS12 chips will function in ADV601 designs with no hardware or software changes. Existing bills of materials can list the ADV601JS12 as a suitable substitute for the ADV601 to simplify purchasing and inventory. New designs will be easier to get up and running if the ADV601JS12 is specified because the ease-of-use features reduce the hardware and software design effort. The ADV601LC, ADV611 and ADV612 do not have a DSP serial port as do the ADV601 and ADV601JS12. The additional DSP serial port modes described below are only meaningful for the chips with DSP serial ports, namely the ADV601 and ADV601JS12.

DIFFERENCES BETWEEN THE ADV601, ADV601LC, ADV611 AND ADV612

Table I provides a summary of the key differences between the original ADV601 and the three parts that have followed.

USE CREF PIN TO STALL VIDEO INTERFACE

The CREF pin is a VCLK qualifier. In "Broadside Phillips" mode and Grayscale mode, new pixels arrive at 13.5 MHz, while VCLK is 27 MHz. CREF asserted (high) tells the ADV601 which VCLKs have a valid pixel and which ones do not. In the original chip CREF was not functional in either CCIR 656 mode or Multiplexed Philips mode. In the ADV601JS12 this restriction is removed and CREF can be used to stall, or throttle, the raw video interface when in CCIR 656 mode or Multiplexed Philips mode.

This feature can be used to operate the video interface at less than real-time speeds. If the external system is not ready to source or sink raw video, deassert CREF and the ADV601 will pause and wait until CREF is asserted before accepting or emitting raw video. It can also be used to synchronize ADV601 raw video with an external sync in CCIR 656 decode mode. Start up with CREF deasserted. When it is time for the first video field to start, assert CREF and keep it asserted.

To assure compatibly with systems designed for the ADV601, the CREF stall on CCIR-656 and Multiplexed Philips the ADV601 powers up with CREF Stall mode

Table I.

	ADV601JS	ADV601JST12	ADV601LC	ADV611JST	ADV612BST
Bits per Pixel	20	20	16	16	16
Bits per Component	10	10	8	8	8
DSP Serial Port	Yes	Yes	No	No	No
Package	160 PQFP	160 PQFP	120 TQFP	120 TQFP	Identical to ADV611JST
Pin Assignments	Unique	Same as ADV601JS	Unique	98% Similar to ADV601LC	Identical to ADV611JST
Temperature Range	0°C to +70°C	0°C to +70°C	0°C to +70°C	0°C to +70°C	−25°C to +85°C
θ_{JA}	31°C/W	31°C/W	35°C/W	35°C/W	35°C/W
θ_{JC}	7.5°C/W	7.5°C/W	5°C/W	5°C/W	5°C/W
Field Rate Reduction	Software	Hardware	Hardware	Hardware	Hardware
Stall Mode	No	Yes	Yes	Yes	Yes
Field Size Limit	No	Yes	Yes	Yes	Yes
Field Size Register	No	Yes	Yes	Yes	Yes
Field Bit Polarity Control	No	Yes	Yes	Yes	Yes
Evaluation Board	Videolab	Videolab	Videopipe	CCTV Pipe	CCTV Pipe
Target Applications	Professional	Professional	Consumer	CCTV	Industrial CCTV

disabled. To use the feature, set Bit 15 (Video Stall Enable) in the Mode Control Register.

FIELD REVERSAL DEFEAT BIT IN MODE CONTROL REGISTER NUMBER 2

During ADV601 development it was noticed that the decoded raw video would occasionally go "field reversed." The TV monitor would display Field 2's video when it should have displayed Field 1's video. The visual effect watching the TV monitor is odd. The video looks almost right, but close examination will show excessive jaggedness on edges, particularly diagonal edges. Field reversal happened whenever the host CPU dropped a single compressed video field, or put them out of order through various software errors. The problem was not so much an ADV601 decode problem as a host CPU data loss problem. Nevertheless, the ADV601 was modified to prevent field reversal, even if caused by data loss.

The ADV601 now compares the Field 1, Field 2 bits in the compressed video bit stream against the video sync. If the chip finds it is about to play Field 2, when it ought to be playing Field 1, (or vice versa) it gets back in step by skipping a field. The chip outputs one field of solid gray to get back in step and then proceeds to play the compressed video field. This improvement works well, for playback of 50/60 field-per-second interlaced video. It prevents field reversal at all times.

However, the field reversal logic makes many of the simplest special effects very difficult. Consider the ordinary case of "freeze field" video. To freeze a single image the receiver decodes the same compressed video field over and over again. In this case, the ADV601 will see a field header that always reads Field 1, Field 1, Field 1. Half the time the chip will decide it ought to have Field 2, and output a gray field. The visual effect is a flicker at the field rate, and half the video lines show gray. The Videopipe software overcomes this problem by altering the field bit in software at the field rate. The field reversal defeat feature accomplishes the same task with less code. Set Bit 11 (ignore field bit) in the new Mode Control Register Number 2. This is much easier to program than a subroutine to search through the compressed bitstream, find and alter the field headers.

Best video performance on "straight" 50/60 Hz interlaced video will still be obtained with field reversal defeat OFF, but for freeze field, field doubling, or field rate reduction, the field rate flicker can be removed by turning field reversal defeat ON.

To ensure computability with systems designed for the ADV601, field reversal defeat powers up OFF.

FIELD BASED CROPPING

VSTART and VEND should be thought of as working on the frame level. For example, if VSTART = 10 and VEND = 240, the first nine lines of Field 1 will be blacked out and the last three lines of Field 1, along with all of Field 2, will be blacked out. If the VSTART and VEND registers can be changed on the fly during the vertical blanking interval, the cropping will work for each field. The ideal place to change these is in response to the STATS_RDY interrupt.

To make the cropping registers easier to program, a new simpler cropping mode was added. If Bit 14 (New Cropping Mode Enable) in the Mode Control Register is set, the VSTART and VEND registers are now field based. For example, if VSTART = 10 and VEND = 240, the first nine lines of Field 1 and 2 will be blacked out and the last three lines of Field 1 and 2. There is no longer any need to reprogram VSTART and VEND on each STATS_RDY interrupt.

To ensure compatibility with the ADV601, the chip powers up with the New Cropping Mode bit OFF, and VSTART and VEND are frame-based.

HARDWARE FIELD RATE REDUCTION

In many cases a full 50 or 60 field-per-second output is not necessary, or fields must be discarded to meet bit rate targets. For example, you must discard some fields to get the bit rate down to 128 Kbps. The ADV601 max compression ratio is only 350:1, so 500 Kbps is the minimum possible bit rate if all fields are transmitted. To achieve 128 Kbps, three fields out of every four must be discarded. Field rate reduction is programmed in Mode Control Register Number 2. Program the number of fields to discard. Zero means send all fields, 1 means send 1 out of 2, 2 means send 1 out of 3 and so on. Remember, if you select field rate reduction on encode, you will want to enable field reversal defeat upon decode to avoid a field rate flicker in the playback video.

To ensure compatibility with the ADV601, the chip powers up with field rate reduction set to zero (off).

PROGRAMMABLE FIELD PIN POLARITY

The FIELD signal is normally LOW for Field 1 and HIGH for Field 2. To accommodate video encoders or decoders that require the opposite polarity, you can reverse the polarity of the field signal by setting Bit 3 in Mode Control Register 2.

To ensure computability with systems designed for the ADV601, field polarity reverse powers up OFF.

GREATER TOLERANCE FOR PIXEL-PER-LINE CHANGES

ADV601 data sheet Table I (ADV601 Field Rates and Sizes) specifies Total Region Horizontal, which is the total number of pixels (both active *and* blanked) per video line. The original ADV601 would not tolerate any variation in pixel count from line to line. This caused difficulty interfacing to some video decoders. The ADV601JS12 will function properly so long as the line length variations are held to less than 5%. For instance, the ADV601

requires exactly 858 pixels per line in standard NTSC mode. The ADV601JS12 will function properly as long as each line contains more than 815 and less than 900 pixels. To take advantage of this feature, put the ADV601JS12 into CCIR 656 SLAVE mode. The part will still observe the SAV and EAV codes embedded in the raw video, so it is not necessary to drive the sync pins.

NEW BITS IN MODE CONTROL REGISTER NUMBER 1
Mode Control Register:
Indirect Address 0x0 (WRITE Only)

Bits	Function	Reset
15	Video Stall Mode Enable	0
14	New Cropping Mode Enable	0

In the ADV601, Bits 15 and 14 in the Mode Control Register are reserved for future expansion. In the ADV601JS12 they enable the Video Stall Mode and the New Cropping Mode. To insure compatibility with the ADV601, the chip powers up with Bits 14 and 15 OFF.

NEW MODE CONTROL REGISTER (MCR2)
This register contains bits to support the new features of the ADV601JS12.

Mode Control Register Number 2
Indirect Address 0x9 (RD/WR)

Bits	Function	Reset
15–12	Reserved, Always Write with 0	0
11	Field Reversal Defeat Bit (DECODE)	0
10	Reserved, Always Write with 1	0
9	Reserved, Always Write with 1	0
8:4	Field Rate Reduction (ENCODE)	0
3	Field Pin Polarity	0
2:0	Reserved, Always Write with 0	0

NEW BIN WIDTH REGISTER, COMPRESSED FIELD SIZE LIMIT RD/WR
Max Compressed Field Size MSB (16 MSBs)
Indirect Register Address 8

Bits	Function	Reset
15:0	LONGWORD_COUNT <19:4>	0xffff

Maximum LONGWORD Register: A 16-bit register will contain a programmable Maximum LONGWORD count. This register will reset to 0xffff, and a *Bit in the DSP Port Mode Control Register must be set HI* to enable this feature. The implementation of this feature is as follows:

When the high 16-bit LONGWORD count reaches the MAX, the QUANTIZER will zero out all remaining samples in the field. Upon the start of the next field, the QUANTIZER will go back to using the programmed Reciprocal Bin Widths. This will cause some overshoot of the target Maximum, but only by a few LONGWORDS.

Note: The internal compressed field size register is 20 bits wide. The 16 bits written to Register 8 the most significant bits. Writing information to Register 8 sets the internal register to 16.

TWO NEW STATISTICS REGISTERS, COMPRESSED VIDEO FIELD SIZE
Max Compressed Field Size MSB (16 MSBs)
Indirect (Read) Register Address 0xB3 (RD)

Bits	Function	Reset
15:0	LONGWORD_COUNT<19:4>	0

Max Compressed Field Size LSB (4 LSBs)
Indirect Address 0xB4 (RD)

Bits	Function	Reset
3:0	LONGWORD_COUNT<3:0>	0

The compressed field size registers allow the user to read the field size of the most recently compressed field. Size is scaled in 32-bit long words. For example, if the register contains "1" it means the field is one long word (4 bytes) long. This feature is useful in straight feedback bin width calculators. The data is valid after STATS_RDY interrupt occurs.

DSP PORT TRANSMITS COMPRESSED VIDEO FIELD SIZE REGISTERS (ADV601JST12 ONLY)
The DSP port will power up in standard mode, which transmits the original set of statistics registers in accordance with Figure 41 in the ADV601 data sheet. This insures computability with existing ADV601 applications.

If the DSP port is placed in enhanced mode, via the DSP Port Mode Control Register, the ADV601 will transmit the two compressed video field size registers after transmitting 52 original statistics. The MSB Compressed Field Size Register will be transmitted before the LSB register. Enhanced mode is used by sophisticated bin width calculators that use both statistics and compressed field size.

If the DSP port is placed in field-size-only mode via the DSP Port Mode Control Register, the DSP port will output only the compression ratio and the Compressed Video Field Size Registers. None of the original field statistics registers will be transmitted. The transmission

will be initiated at LCODE time, not STATS_RDY time. The serial stream will consist of three 16-bit words: Compression Ratio followed by MSB and LSB Compressed Video Field Size Registers. Field-size-only mode is used by straight feedback bin width calculators which do not use the other statistics. The compressed field size count is only known to the ADV601 at LCODE time (time the last video field is read out of the compressed data port). Field-size-only mode gives a feedback bin width calculator the freshest data, since the chip makes the transmission as soon as the field size is available, rather than waiting for STATS_RDY time to occur.

NEW DSP PORT MODE CONTROL REGISTER
DSP Port Mode Control Register
Indirect Address 0x7 (RD/WR)

Bits	Function	Reset Value
4	Compressed Field Size Limit Enable	0
1	DSP Port Field Size Only Mode	0
0	DSP Port Enhanced Mode	0