

Fast Display D/A Converter

FEATURES Dealitcher 10-Bit Resolution & Accuracy Monotonic High Speed Settling to ±1/2LSB 40ns - 1LSB Step 200ns - Full Scale Step Linearity ±1/2LSB Coaxial Cable Connector Output Schottky TTL Register Included

ON Graphic Displays Deflection Character Generator: High Speed D/A System

DESCRIPTION

The DAC-10DF is a 10-bit D/A converter tha settling, virtually glitch free, voltage output. These features make it a particularly good choice for use in CRT display sys tems. It is also well suited for other applications requiring high speed, glitchless operation, such as character generators, high speed test equipment, and very high speed A/D converters. A coaxial cable output is used to ensure that the DAC-10DF's high speed output signal is received exactly as transmitted. With a model 50 output amplifier, the output will settle to within ±1/2LSB in 40ns for 1LSB input change. Monotonicity is assured from +5°C to +45°C. Schottky TTL is used for the input register to increase speed and decrease time skew. Decreased register skew and a new deglitching circuit combine to practically eliminate the undesirable glitches which would otherwise occur at the major carry and other major transitions of the converter.

OUTPUT OPTIONS

The DAC-10DF is available with either a model 48K or a model 50K output amplifier. Both offer the same selection of output ranges, ±2.5V, ±5.0V, or ±10.0V. In either case, the amplifier's output is wired to a board mounted Microdot RF connector. The fast, high current output of the model 50 makes it suitable for driving a terminated 50 to 100Ω coaxial cable. Its 100mAoutput capability permits the high slew rates needed for good pulse transmission over a coaxial cable. The model 48K is a lower power amplifier, offering lower power supply current requirements. It may be used for driving higher impedance cables that don't require a high current source.

TIMING

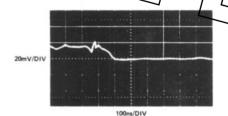
The strobe pulse must have rise and fall times ≤12ns, and a

WITHOUT DEGLITCHER

The two views above show the DAC-10DF during a major carry transition. Note that without the deglitcher, not only does the large glitch fly down way offscale, but also that the settling time is much longer.

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of at least 50 ns. The data inputs must remain constant Ons prior to until 10ns after the strobe pulse's leading The digital input data is transferred from the input register to the D/A conversion circuitry approximately ulse's leading edge.



WITH DEGLITCHER

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West Coast Mid-West 213/595-1783 312/894-3300

Texas 214/231-5094

SPECIFICATIONS (typical @ +25°C and nominal supply voltages, unless otherwise noted)

MODEL	DAC-10DF	DAC-10DF
	(With 48K	(With 50K
	Output Amplifier)	Output Amplifier)
RESOLUTION	10 Bits	•
Differential Linearity	±1/2LSB max	
Monotonic	+5°C to +45°C Guaranteed	•
Linearity 1	±½LSB max	*
LOGIC LEVELS	0 ≤ "0" ≤ +0.8V	•
	@ -2mA max +2.0 ≤ "1" ≤ +5.0V	
	@ 80μA max	
DIGITAL INPUTS	1 Schottky TTL Load/Bit	
STROBE INPUT	Positive Pulse, 50 to 500ns,	•
STROBE INPUT	1 Schottky TTL Load	
CODING OPTIONS ²	Offset Binary, Two's Complement	•
REFERENCE	Internal High Stability Reference Included	•
OPERATING TEMP. RANGE	0 to +70°C	
OUTPUT OPTIONS	±2.5V, ±5.0V, ±10.0V	±2.5V, ±5.0V, ±10.0V
	@ 15mA max	@ 100mA max
SETTLING TIME ³ For FS Step	500ns max	200ns max
For FS Step For 1LSB Step GLITCH	100 s max 5mV Peak (max)	200ns max 40ns max 20m1 Peak (max) (50ns Width (hyp)
For FS Step For 1LSB Step GLITCH	100ns max	40ns max
For FS Step For 1LSB Step GLITCH GAN TEMPERATURE COEFFICIENT	100 s max 5mV Peak (max) 50 width (rec) 50 ppm/°C of Reading	40ns max 20m (Peak (max)
For FS Step For 1LSB Step GLITCH GAN TEMPERATURE COEFFICIENT ZERO TEMPERATURE COEFFICIENT	100 s max 5mV Peak (max) 50 s Width (rec) 450 ppm/2 Oof Reading (max)	40ns mx 20m (Peak max) 50ns W tith (lyp)
For FS Step For 1LSB Step GLITCH GAN TEMPERATURE COEFFICIENT ZERO TEMPERATURE COEFFICIENT	100 s max 5mV Peak (max) 50 s Width (tree) 450ppm/° C of Reading (max) ±20ppm/° C of FS (max)	40ns max 20m V Peak max) 50ns With (yp) * -30ppm/0: of FS (max) -15V dc ±3% @ 2000 A max -15V dc ±3% @ 2000 A max
For FS Step For 1LSB Step GLITCH GAN TEMPERATURE COEFFICIENT ZERO TEMPERATURE COEFFICIENT POWER REQUIREMENTS	100 s max 5mV Peak (max) 50 w Width (two) 250 ppm/°C of Reading (max) ±20 ppm/°C of FS (mx) +15V dc ±3% @ 80 mA max -15V dc ±3% @ 80 mA max	40ns max 20m V Peak max) 50ns With (yp) * -30ppm/0: of FS (max) -15V dc ±3% @ 2000 A max -15V dc ±3% @ 2000 A max
For FS Step For 1LSB Step GLITCH GAN TEMPERATURE COEFFICIENT ZERO TEMPERATURE COEFFICIENT POWER REQUIREMENTS	100 s max 5mV Peak (max) 50 w Width (two) 250 ppm/°C of Reading (max) ±20 ppm/°C of FS (mx) +15V dc ±3% @ 80 mA max -15V dc ±3% @ 80 mA max +5V dc ±5% @ 400 mA max	40ns mx 20m V Peak (max) 50ns Watth (lyp)
For FS Step For 1LSB Step GLITCH GAN TEMPERATURE COEFFICIENT ZERO TEMPERATURE COEFFICIENT POWER REQUIREMENTS	100 s max 5mV Peak (max) 50 w Width (two) 20ppm/°C of Rading (max) ±20ppm/°C of FS (max) +15V dc ±3% @ 80mA max -15V dc ±3% @ 80mA max 4.5" x 6.0" x 0.67"	40ns mx 20m V Peak (max) 50ns Watth (lyp)
FOR FS Step FOR 1LSB Step GLITCH GAN TEMPERATURE COEFFICIENT ZERO TEMPERATURE COEFFICIENT POWER REQUIREMENTS SIZE & CONSTRUCTION	100 s max 5mV Peak (max) 50 s Width (two) 200ppm/°C of R:ading (max) ±20ppm/°C of FS (max) +15V dc ±3% @ 80mA max -15V dc ±5% @ 400mA max 4.5" x 6.0" x 0.67" (114.3 x 152.4 x 17.02mm)	40ns mx 20m V Peak (max) 50ns Watth (lyp)
FOR FS Step FOR 1LSB Step GLITCH GAN TEMPERATURE COEFFICIENT ZERO TEMPERATURE COEFFICIENT POWER REQUIREMENTS SIZE & CONSTRUCTION	100 s max 5mV Peak (max) 50 w Width (two) 250 ppm/°C of Reading (max) ±20 ppm/°C of FS (max) +15V dc ±3% @ 80mA max -15V dc ±3% @ 80mA max +5V dc ±5% @ 400mA max 4.5" x 6.0" x 0.67" (114.3 x 152.4 x 17.02mm) PC Plug-In Card Cinch #250-22-30-170	40ns mx 20m V Peak (max) 50ns Watth (lyp)
FOR FS Step FOR 1LSB Step GLITCH GAN TEMPERATURE COEFFICIENT ZERO TEMPERATURE COEFFICIENT POWER REQUIREMENTS SIZE & CONSTRUCTION MATING EDGE CONNECTOR	100 s max 5mV Peak (max) 50 s Width (tree) 250ppm/°C of Reading (max) ±20ppm/°C of FS (max) +15V dc ±3% @ 80mA max -15V dc ±3% @ 400mA max 4.5" x 6.0" x 0.67" (114.3 x 152.4 x 17.02mm) PC Plug-In Card	40ns mx 20mV Peak (max) 50ns Watth (lyp)
FOR FS Step FOR 1LSB Step GLITCH GAN TEMPERATURE COEFFICIENT ZERO TEMPERATURE COEFFICIENT POWER REQUIREMENTS SIZE & CONSTRUCTION MATING EDGE CONNECTOR	100 s max 5mV Peak (max) 50 w Width (two) 250 ppm/°C of Reading (max) ±20 ppm/°C of FS (max) +15V dc ±3% @ 80mA max -15V dc ±3% @ 80mA max +5V dc ±5% @ 400mA max 4.5" x 6.0" x 0.67" (114.3 x 152.4 x 17.02mm) PC Plug-In Card Cinch #250-22-30-170	40ns mx 20mV Peak (max) 50ns Watth (lyp)
FOR FS Step FOR 1LSB Step GLITCH GAN TEMPERATURE COEFFICIENT ZERO TEMPERATURE COEFFICIENT POWER REQUIREMENTS SIZE & CONSTRUCTION MATING EDGE CONNECTOR MATING COAXIAL CONNECTOR	100 s max 5mV Peak (max) 50 s Width (tree) 250ppm/°C of Reading (max) +15V dc ±3% @ 80mA max -15V dc ±3% @ 80mA max +5V dc ±5% @ 400mA max 4.5" x 6.0" x 0.67" (114.3 x 152.4 x 17.02mm) PC Plug-In Card Cinch #250-22-30-170 (supplied) Microdot #132-0300-0003 (supplied) Gain	40ns max 20mV Peak (max) 50ns Whith (hyp) 250ppm/2 of FS (max) 415V dc ±3% @ 200mA max -15V dc ±3% @ 200mA max *
FOR FS Step FOR 1LSB Step GLITCH GAN TEMPERATURE COEFFICIENT ZERO TEMPERATURE COEFFICIENT POWER REQUIREMENTS SIZE & CONSTRUCTION MATING EDGE CONNECTOR MATING COAXIAL CONNECTOR	100 s max 5mV Peak (max) 50 w Width (two) 250 ppm/°C of Reading (max) ±20 ppm/°C of FS (mx) +15 V dc ±3% @ 80mA max -15 V dc ±3% @ 80mA max +5 V dc ±5% @ 400mA max 4.5" x 6.0" x 0.67" (114.3 x 152.4 x 17.02mm) PC Plug-In Card Cinch #250-22-30-170 (supplied) Microdot #132-0300-0003 (supplied) Gain Dynamic Zero (Glitch	40ns mx 20m V Peak (max) 50ns W lith (lyp) * 130ppm/ L of FS (max) 115V to 13% @ 200mA max -15V do 13% @ 200mA max
FOR FS Step FOR 1LSB Step GLITCH GAN TEMPERATURE COEFFICIENT ZERO TEMPERATURE COEFFICIENT POWER REQUIREMENTS SIZE & CONSTRUCTION MATING EDGE CONNECTOR MATING COAXIAL CONNECTOR	100 s max 5mV Peak (max) 50 w Width (two) 20ppm/°C of Reading (max) ±20ppm/°C of FS (mx) +15V dc ±3% @ 80mA max -15V dc ±3% @ 400mA max 4.5" x 6.0" x 0.67" (114.3 x 152.4 x 17.02mm) PC Plug-In Card Cinch #250-22-30-170 (supplied) Microdot #132-0300-0003 (supplied) Gain Dynamic Zero (Glitch Suppression)	40ns max 20mV Peak (max) 50ns Watth (hyp)
FOR FS Step FOR 1LSB Step GLITCH GAN TEMPERATURE COEFFICIENT ZERO TEMPERATURE COEFFICIENT POWER REQUIREMENTS SIZE & CONSTRUCTION MATING EDGE CONNECTOR MATING COAXIAL	100 s max 5mV Peak (max) 50 w Width (two) 250 ppm/°C of Reading (max) ±20 ppm/°C of FS (mx) +15 V dc ±3% @ 80mA max -15 V dc ±3% @ 80mA max +5 V dc ±5% @ 400mA max 4.5" x 6.0" x 0.67" (114.3 x 152.4 x 17.02mm) PC Plug-In Card Cinch #250-22-30-170 (supplied) Microdot #132-0300-0003 (supplied) Gain Dynamic Zero (Glitch	40ns max 20mV Peak (max) 50ns Whith (hyp) 250ppm/2 of FS (max) 415V dc ±3% @ 200mA max -15V dc ±3% @ 200mA max *
FOR FS Step FOR 1LSB Step GLITCH GAN TEMPERATURE COEFFICIENT ZERO TEMPERATURE COEFFICIENT POWER REQUIREMENTS SIZE & CONSTRUCTION MATING EDGE CONNECTOR MATING COAXIAL CONNECTOR ADJUSTMENTS	100 s max 5mV Peak (max) 50 w Width (two) 20ppm/°C of Reading (max) ±20ppm/°C of FS (mx) +15V dc ±3% @ 80mA max -15V dc ±3% @ 400mA max 4.5" x 6.0" x 0.67" (114.3 x 152.4 x 17.02mm) PC Plug-In Card Cinch #250-22-30-170 (supplied) Microdot #132-0300-0003 (supplied) Microdot #132-0300-0003 Gain Dynamic Zero (Glitch Suppression) Offset	40ns mx 20m V Peak (max) 50ns W ith (yp) 250ppm/ L of FS (max) 115V dc ±3% @ 200mA max -15V dc ±3% @ 200mA max

Specifications same as for DAC-10DF with 48K amplifier.

ORDERING INFORMATION

DAC 10DE/VV/VV

		DAC-10DF/XX/XX
Output	(±2.5 Volts:	2.5
Range	±5.0 Volts:	5.0
	±10.0 Volts:	10
Output	Model 48K:	48
Amplifier	Model 50K:	50

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
Α	BIT 1 (MSB)	N)	INTERLOCK
В	BIT 2	P (CONNECTIONS
C	BIT 3	R	+5V dc
D	BIT 4	S)	
E	BIT 5	T }	DIGITAL GROUND
F	BIT 6	u \	
Н	BIT 7	V)	ANALOG GROUND
J	BIT 8	w /	ANALOG GROOND
K	BIT 9	X ′	+15V dc
L	BIT 10 (LSB)	Y	-15V dc
M	STROBE	Z	ANALOG GROUND

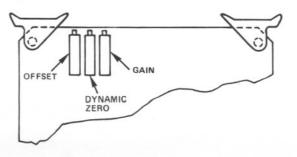
CIRCUIT CONNECTIONS

The DAC-10DF's output is connected to a coaxial cable via a Microdot RF connector. A 93Ω RG 195 cable or its equivalent is recommended. For optimum received signal shape, the receiving end of the cable must be terminated into a purely resistive load that has a resistance equal to the characteristic impedance of the cable. Because of this requirement, the ±10V output option cannot be used with a cable that has a characteristic impedance of $\leq 93\Omega$. In such an instance, the current required would exceed that available from the DAC-10DF. In order to prevent the possibility of a ground loop through the paxia cable's shield, the DAC-10DF and the circuitry it drives should be powered by separate power supplies having no common connection It is recommended that the ±15V dc power supply feeding the DAC 100F have no other loads connected to it. The power supply should have an ac output imlance at 10kHz of **∢1Ω**

Normally, the digital and analog grounds of a D/A converter would be brought out separately, run to a common point, and then joined together. However, because of the DAC-10DF's exceptionally high speed, the inductance of the ground leads is likely to cause noise in the converter's output. Therefore, the digital and analog grounds are tied together on the DAC-10DF's PC board. The IR drop along common digital and analog ground leads that may cause problems with higher resolution (e.g., 14 or 16 bit) DACs is not likely to be troublesome to a 10 bit DAC.

Because of the very high speed of the Schottky TTL input registers, it is possible that the digital input signals could be reflected back and forth between the DAC-10DF's inputs and their driving sources. This might result in a wavefront that builds up sufficient voltage to damage some of the logic. Driving the logic inputs with transmission lines, and terminating each cable at the DAC-10DF's socket with a resistor (equal to the characteristic impedance of the cable) in series with a 220pF capacitor between each input and ground will prevent these reflections.

POTENTIOMETER ADJUSTMENTS



Deviation measured from the straight line through +Full Scale and -Full Scale.

The unit is shipped connected for Offset Binary. The coding is determined by a jumper associated with 3 adjacent terminals on the PC board, lettered A, C, and B. B is jumpered to C for Offset Binary coding. A is jumpered to C for Two's

³ As measured with ±2.5 volt output, from trailing edge of clock pulse to point where output is within ±3LSB of final value.

Specifications subject to change without notice