# ANALOG DEVICES

# Low Feedthrough Multiplying D/A Converter

DAC1125

PRELIMINARY TECHNICAL DATA



**FEATURES**
- 12 Bit Resolution and Accuracy
- Two Quadrant or Four Quadrant Operation
- Four Quadrant Feedthrough <½LSB to 40kHz
- 3μs Settling Time
- 3ppm/°C Gain TC


## GENERAL DESCRIPTION

The DAC1125 is a 12-bit multiplying digital-to-analog converter. As shown in Figure 1, it functions essentially as a multiplier whose output voltage represents the product of a bipolar analog input voltage and a digitally programmed bipolar constant. This constant can be varied in 4,096 steps from -1 to 0 (Two Quadrant operation), or from -1 to +1 (Four Quadrant operation).

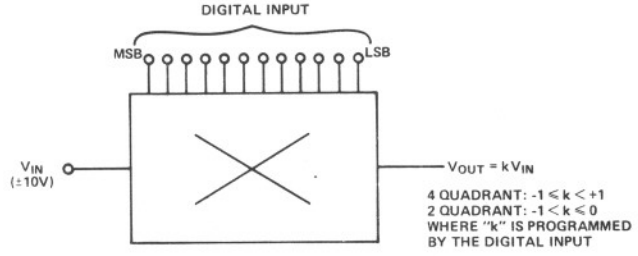



*Figure 1. DAC1125 Functional Diagram*

One of the primary features of the DAC1125 is its exceptionally low Four Quadrant Zero feedthrough. Analog input signals with frequencies of up to 40kHz produce a feedthrough which is guaranteed to be less than ±½LSB. The DAC1125 also features ±½LSB accuracy, 3μs settling time to ±0.01% of reading, and a ±10ppm/°C maximum gain temperature coefficient. The digital inputs are fully TTL/DTL compatible.

## LOW FEEDTHROUGH

The ideal multiplying D/A converter would be one which had a feedthrough of zero. For such a device, the output voltage would be zero when "k" was programmed to be zero, regardless of the amplitude or frequency of the analog input signal. However, due to capacitive coupling, switch leakage, and other effects, practical multiplying D/A's do have a measurable feedthrough which increases with frequency. In 12 bit devices available prior to the DAC1125, Four Quadrant Zero feedthrough would generally exceed ½LSB for full scale input signals of 500Hz and above. The utility of these products was, therefore, greatly restricted.

The DAC1125 combines innovative design with advanced CMOS technology to achieve a new standard of converter performance. Figure 2 shows the typical zero feedthrough as a function of input signal frequency for the Two Quadrant and Four Quadrant modes of operation. Note that the Four Quadrant Zero feedthrough is under ½LSB even at 40kHz.

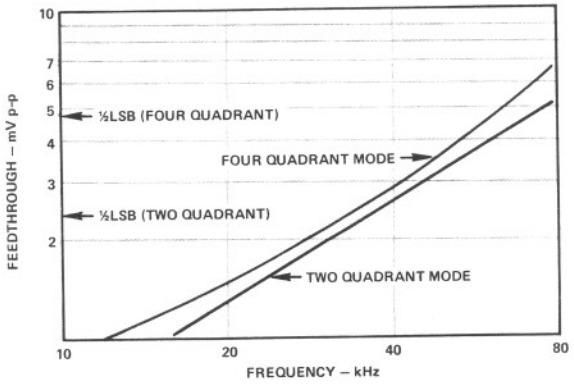



*Figure 2. Typical Zero-Code Feedthrough vs. Input Frequency (For a 20V p-p Sinewave Input)*



Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast 213/595-1783 | Mid-West 312/894-3300 | Texas 214/231-5094

# SPECIFICATIONS (Typical at +25°C and ±15VDC supplies unless otherwise noted)

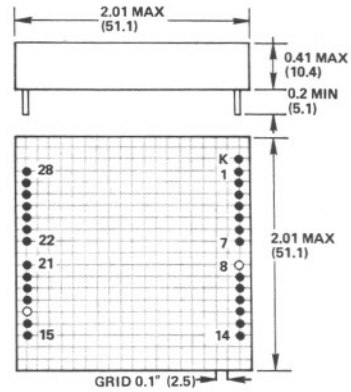
| | |
|---|---|
| RESOLUTION | 12 Bits |
| ACCURACY | |
| Relative to Input[1] | |
| Two Quadrant | ±0.4LSB max |
| Four Quadrant | ±0.5LSB max |
| Monotonicity | Guaranteed |
| | 0 to +70°C (Two Quadrant) |
| | 0 to +50°C (Four Quadrant) |
| ANALOG INPUT | |
| Voltage Range | |
| Nominal | ±10V |
| Absolute Maximum | ±15V |
| Input Impedance | 5kΩ (±1%) Shunted by ≈10pF |
| DIGITAL INPUT | |
| Logic Levels | |
| 0V ≤ Logic "0" ≤ 0.7V | -180μA max |
| 2V ≤ Logic "1" ≤ 5.5V | +10μA max |
| Coding | |
| Two Quadrant | Complementary Binary |
| Four Quadrant | Positive True Offset Binary, or Two's Complement |
| OUTPUT | |
| Voltage | ±11V max |
| Current | ±5mA max |
| Impedance | <1 ohm |
| Capacitive Load | 300pF max |
| DYNAMIC CHARACTERISTICS | |
| Feedthrough (4 Quad. Zero) | ±0.5LSB max, 0 to 40kHz |
| Settling Time[2] (to 0.01% of FS) | 3μs (10μs max) |
| Frequency Response[3] | -3dB @ 450kHz |
| Full Power Bandwidth | 500kHz (300kHz min) |
| Slew Rate | 20V/μs |
| Output Noise[4] | |
| Two Quadrant | 5mV p-p |
| Four Quadrant | 8mV p-p |
| Phase Shift[5] | -0.5° @ 5kHz |
| TEMPERATURE COEFFICIENTS | |
| Gain | 3ppm/°C (10ppm/°C max) |
| Zero | |
| Two Quadrant | 20μV/°C max |
| Four Quadrant | 50μV/°C max |
| Differential Nonlinearity | 3ppm/°C |
| POWER REQUIREMENT[6] | |
| Positive Supply | 13V to 17V @ 17mA |
| Negative Supply | -12V to -18V @ -10mA |
| POWER SUPPLY REJECTION | >80dB |
| TEMPERATURE RANGE | |
| Operating | 0° to +70°C |
| Storage | -55°C to +125°C |
| PRICE (1-9) | $295 |

[1] For a ±10V sinewave, 0 to 10kHz.
[2] For a 20V output step of either polarity resulting from an analog or digital input change.
[3] For a ±10V sinewave input and output.
[4] White noise at output as measured over a 20MHz bandwidth.
[5] Input to output phase shift for a ±10V sinewave output.
[6] If input and output voltage ranges are restricted to ±5V, the positive supply may be reduced to 8.5V and the negative supply reduced to -7V.

Specifications subject to change without notice.

## OUTLINE DIMENSIONS

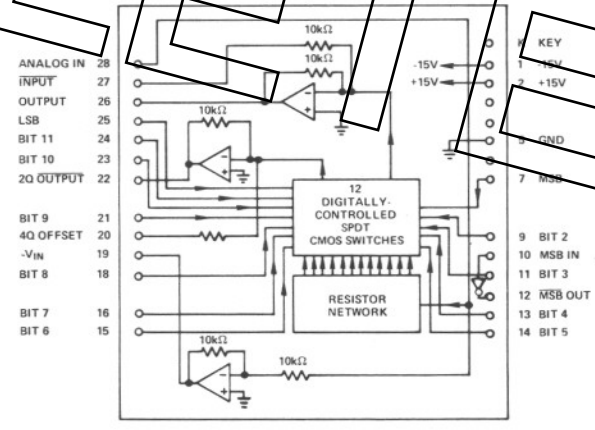
Dimensions shown in inches and (mm).




BOTTOM VIEW

NOTE:
Terminal pins installed only in shaded hole locations
Module weight: 1.6 ounces (45 grams)
All pins are gold plated half-hard brass, (MIL–G–45204), 0.019" ±0.001" (0.483 ±0.025mm) dia.
For plug-in mounting card order Board No. AC4102 @ $15.

## DAC1125 BLOCK DIAGRAM



## PRINCIPLE OF OPERATION

The DAC1125 consists of two identical current summing D/A's in one package. Figure 3 shows its circuitry in greatly simplified form.

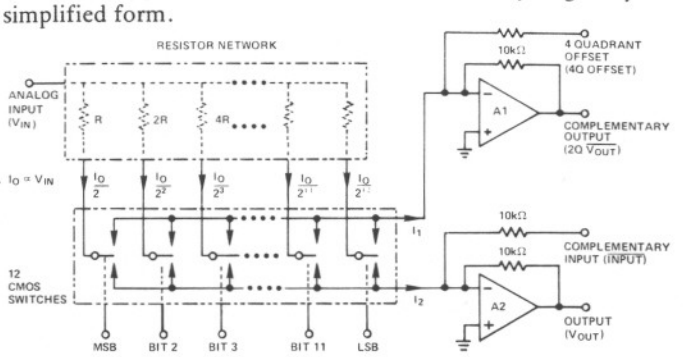



*Figure 3. Simplified DAC1125 Circuit*

An analog voltage which can vary from −10V to +10V is applied to the analog input. The resistor network develops a series of 12 binarily weighted currents which are proportional to the input voltage. These 12 currents are directed to either of two op amp summing junctions by a series of 12 digitally controlled SPDT CMOS switches. When a logic "1" is applied to the switch control line, the corresponding bit current goes to the summing junction of A1 and when logic "0" is applied it goes to A2. The maximum current going to A1 will occur when a digital input of 111111111111 is applied. Any other digital input will divert current to A2. Thus, for a fixed $V_{IN}$, the sum of $I_1$ and $I_2$ is a constant.

## TWO QUADRANT OPERATION

In the Two Quadrant mode of operation, the COMPLEMENTARY INPUT and FOUR QUADRANT OFFSET inputs are grounded. The OUTPUT voltage is related to the INPUT voltage and the digitally programmed constant, k, by:

$$V_{OUT} = k\ V_{IN};\ -0.99976 \leqslant k \leqslant 0$$

Table I shows the relationship between the complementary binary coded digital input and the nominal value of k for this mode of operation. Note that a 1LSB step is represented by a fractional change of 0.00024.

| DIGITAL INPUT | k |
|---|---|
| 111111111111 | 0.00000 |
| 111111111110 | −0.00024 |
| 101111111111 | −0.25000 |
| 100000000000 | −0.49976 |
| 011111111111 | −0.50000 |
| 001111111111 | −0.75000 |
| 000000000000 | −0.99976 |

*Table I. Values of k for the Two Quadrant Mode (Complementary Binary Code)*

The COMPLEMENTARY OUTPUT voltage is related to the INPUT and OUTPUT voltages by the following two expressions:

$$V_{OUT} + 2Q\overline{V_{OUT}} = -0.99976\ V_{IN}$$

$$2Q\overline{V_{OUT}} = -(k + 0.99976)\ V_{IN}$$

The values of k as seen at the COMPLEMENTARY OUTPUT are not factory adjusted and may vary by ±1 percent from the ideal values.

## FOUR QUADRANT OPERATION

To achieve Four Quadrant operation, the COMPLEMENTARY OUTPUT is connected to the COMPLEMENTARY INPUT. This subtracts the output of A1 from A2. To implement offset binary code, in which a digital input of 100000000000 gives an output of 0.0V, a small amount of current must be subtracted from I1. This current, proportional to $V_{IN}$, has to shift the OUTPUT voltage by ½LSB. This is done by using a third inverting op amp (not shown in Figure 3) to develop a voltage equal to $-V_{IN}$. A jumper connected between the output of this op amp and the 4Q OFFSET terminal provides the necessary ½LSB offset current. The OUTPUT voltage is thus related to the INPUT voltage and the digitally programmed constant, k, by:

$$V_{OUT} = k\ V_{IN};\ -1 \leqslant k \leqslant 0.99951$$

Table II shows the relationship between offset binary coded digital inputs and the nominal value of k. Note that a 1LSB step is represented by a fractional change of 0.00049.

| DIGITAL INPUT | k |
|---|---|
| 111111111111 | +0.99951 |
| 110000000000 | +0.50000 |
| 100000000001 | +0.00049 |
| 100000000000 | 0.00000 |
| 011111111111 | −0.00049 |
| 010000000000 | −0.50000 |
| 000000000000 | −1.00000 |

*Table II. Values of k for the Four Quadrant Mode (Offset Binary Code)*

A TTL inverter (input at pin 10, output at pin 12) is available for the purpose of inverting the MSB to obtain Two's Complement input coding in the Four Quadrant mode. Table III shows the relation between the nominal value of k and the digital input for this mode.

| DIGITAL INPUT | k |
|---|---|
| 011111111111 | +0.99951 |
| 010000000000 | +0.50000 |
| 000000000001 | +0.00049 |
| 000000000000 | 0.00000 |
| 111111111111 | −0.00049 |
| 110000000000 | −0.50000 |
| 100000000000 | −1.00000 |

*Table III. Values of k for the Four Quadrant Mode (Two's Complement Code)*

## INPUT-OUTPUT RELATIONSHIPS

The input-output relationships are further illustrated below in Figure 4 which shows several two quadrant and four quadrant outputs for a 10V sinewave input and various digital codes.

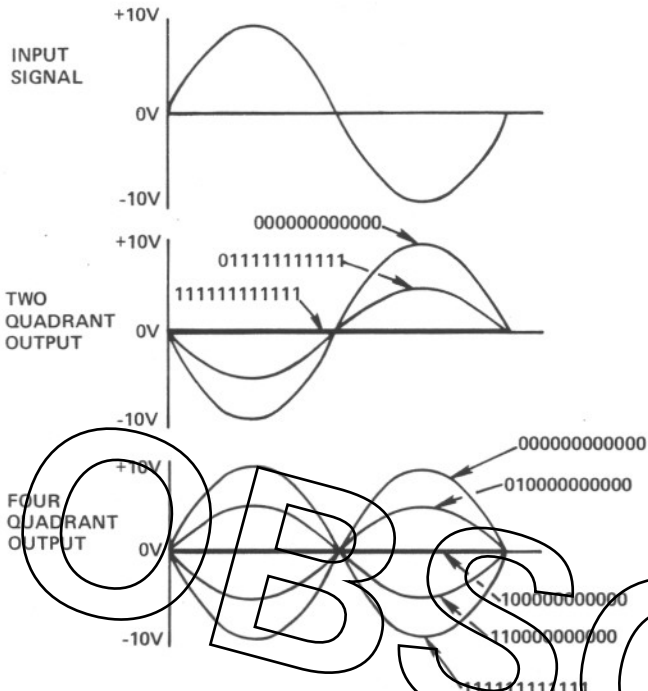



*Figure 4. Response to Sinewave Input for Various Digital Inputs*

## MODULE CONNECTIONS

The DAC1125 is connected as shown in Figure 5 for two-quadrant, and Figure 6 for four-quadrant operation.

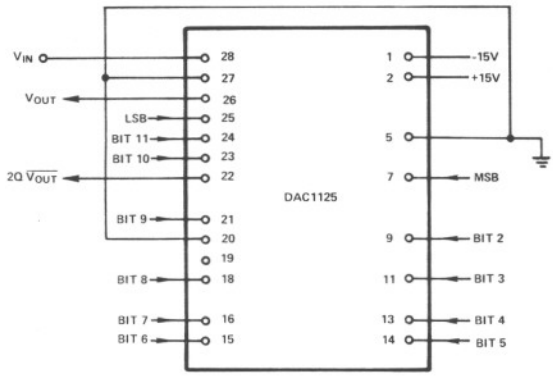



*Figure 5. Connections for Two Quadrant Operation*

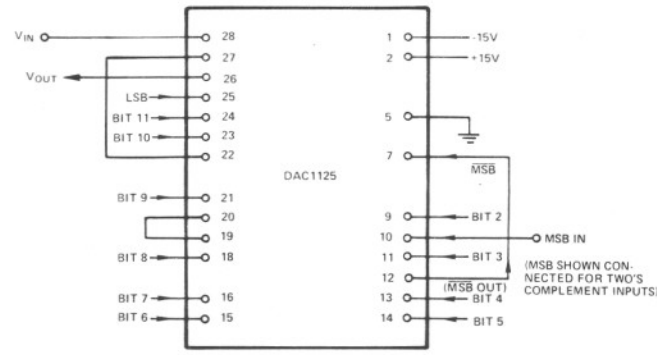



*Figure 6. Connections for Four Quadrant Operation*

All connections between module pins, especially where pins 20 and 27 are involved, should be made with short leads. The use of shielded cable is recommended for analog signal inputs and outputs if the lead length is greater than approximately one foot (300mm). The DAC1125 has internal 0.2μF capacitors which bypass the ±15V supplies and, therefore, external bypass capacitors will only be required in exceptionally noisy environments.

## HANDLING CONSIDERATIONS

Care must be taken in the handling of the DAC1125 to prevent electrostatic damage to its internal CMOS switches. The unit should be transported on conductive foam or other suitable material and should only be handled by properly grounded personnel. The ground pin must be connected before power is applied. Electrostatic damage, should it occur, can result in excessive power supply current, degraded performance, or total failure.

## THE AC4102 MOUNTING CARD

The AC4102 mounting card is available to assist in evaluation of the DAC1125. This 3″ x 3″ (76 x 76mm) printed circuit card has sockets which allow a DAC1125 to be plugged directly onto it. Each of the 28 active pin sockets is connected to a turret terminal so that connections can be easily made to the module without soldering directly to its pins.



C337–10–3/75

PRINTED IN U.S.A.