FEATURES
3-Port Galvanic Isolation
Guaranteed Monotonic 0 to +70°C
Microprocessor Compatible Interface
Increment/Decrement Backup Control
May be Powered from Loop Supply
Low Power: 450mW typ
Output Will Drive 0Ω Loads
Bumpless Transfer, Auto to Manual

APPLICATIONS
Direct Digital Controllers
Ground Loop Elimination in Industrial and Process Control
High Voltage Protected Data Acquisition Systems
Digital Pressure Transducers
Driving Analog Recorders

GENERAL DESCRIPTION
Analog Devices' ISO-DAC™ (ISOlated Digital-toAnalog Converter) model DAC1423 is a low power 10-bit DAC with 4-20mA current output, designed specifically for the process and industrial control industry. Its advanced features and excellent performance make for easy application within new and existing control systems. The DAC1423 contains a CMOS holding register, allowing direct interface with microprocessors, CMOS digital-to-analog converter, voltage-to-voltage isolator and a voltage-to-loop current converter. The small size and low profile (2″ X 4″ X 0.4″) allows much greater functional density than previously available solutions.

DESIGN FEATURES AND USER BENEFITS
Microcomputer Interface: The parallel digital interface is a 5V CMOS design with independently controllable input latches and Tri-State* buffers, split into upper and lower sections (an 8-bit and a 2-bit byte) so that 8- or 16-bit bus compatibility may be achieved.

True 3-Port Isolation: The output connections and power connections are galvanically isolated, both from each other and from the digital section. Each will accommodate a wide range of power supply voltages and may be operated from the same supply, if desired.

Increment/Decrement: Increment/decrement control is achieved via the input latch/counter. An internal slow speed clock is supplied for this operation. Overflow/underflow lockout circuitry is used to prevent full scale "bumps" from occurring.

*Tri-State is a trademark of National Semiconductor Corporation.

Adjustable Offset and Span: The ISO-DAC has offset and span accuracies of ±2LSB's (±0.2% FSR) each. However, if the user desires adjustable offset and span, there are provisions for ±10% adjustment range for each.

High CMV Isolation: The isolation barriers will withstand 1.5V dc continuously, or 1kV rms @ 60Hz for 60 seconds. The ISO-DAC is designed to meet the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability). Common Mode Rejection is excellent; typically, 103dB @ 60Hz for a 250Ω load.

Synchronized: The ISO-DAC may be synchronized to an external system clock, multiple DAC1423's may be on synchronized to one another. In the event of loss of external sync, the DAC1423 will "free run" on its own oscillator.

Isolated Power Out: An internally derived +5V supply is brought out so that the user may power a small amount of application circuitry from the DAC1423's power supply.

ISA-S50.1: The three terminal output structure conforms to the Instrument Society of America Standard ISA-S50.1, "Compatibility of Analog Signals for Electronic Industrial Process Instruments."

SPECIFICATIONS (typical @ +25°C, V_{LOOP} = +24 volts unless otherwise specified)

MODEL	DAC1423
DIGITAL INPUTS	
Resolution	10 Bits
Levels, CMOS V_{DD} = 5V	"1" = $>$ 3.3V @ 1µA
	"0" = $<$ 1.7V @ 1µA
Strobe	Level Sensitive (See Table 2)
ANALOG OUTPUTS	
Type	ISA S50.1 Type 3 Meets or Exceeds Class U
Nominal Range	4-20mA
Compliance	V_{LOOP} −6V
Output Impedance	$>$ 4MΩ @ dc
Minimum Load	0Ω
Maximum Load	(V_{LOOP} −6V/I_{OUT})
Maximum Capacitive Load	Unlimited
STABILITY AND ACCURACY	
Monotonicity	Guaranteed, 0 to +70°C
Integral Nonlinearity	±1/2LSB
Differential Nonlinearity	±1/2LSB
Temperature Stability	
Offset	50ppm FSR/°C
Span	50ppm FSR/°C
Adjustability	±10% each, Offset and Span
Initial Error, Untrimmed[1]	±2LSB's each, Offset and Span
Power Supply Rejection	20ppm FSR/V
Noise, 10Hz to 100Hz[2]	0.1LSB
Warm Up Time to Rated Accuracy	5 minutes
Warm Up Drift	0.5LSB
ISOLATION	
Max CMV, Inputs to Outputs	
ac, 60Hz, 1 minute	1000V rms
dc, Continuous	1500V dc
CMR, Inputs to Outputs, 60Hz, R_L = 250Ω	103dB
POWER	
Loop Supply Range	12−36V dc
Loop Supply Current	I_{OUT} + 5mA
Power Supply Range[3]	14−36V dc
Power Supply Current[3]	20mA
ENVIRONMENTAL	
Operating Temperature	0 to +70°C
Storage Temperature	−25°C to +85°C

NOTES:
[1] Both offset and span error are adjustable to zero. See Figure 2 for details.
[2] Load = 750Ω ‖ 1,000pF and slow clock disabled.
[3] The DAC1423 can be entirely powered from the loop supply. See Figures 4 and 5 for details.

Specifications subject to change without notice.

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

NOTE:
TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS.
MODULE WEIGHT: 60.8G
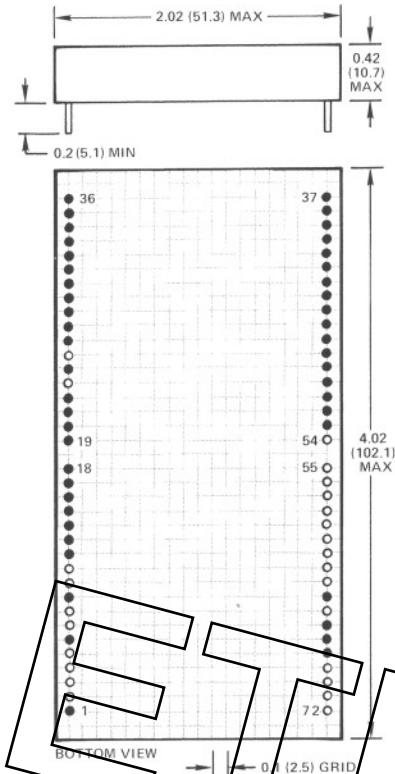
MATING CARD
AC1582
(See Figure 13)

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	I_{OUT}	72	NC
2	NC	71	NC
3	NC	70	NC
4	NC	69	NC
5	NC	68	SYNC IN
6	+V_{LOOP}	67	+V POWER
7	NC	66	SYNC OUT
8	NC	65	NC
9	COMMON	64	PWR COMMON
10	NC	63	NC
11	NC	62	NC
12	NC	61	NC
13	WIDE SPAN	60	NC
14	PRECISION SPAN	59	NC
15	+V_{REF}	58	NC
16	WIDE OFFSET	57	NC
17	PRECISION OFFSET	56	NC
18	SPAN COMMON	55	NC
19	DIGITAL COMMON[1]	54	NC
20	+5V_{OUT}	53	DIGITAL COMMON[1]
21	LOAD HIGH	52	CLOCK IN
22	LOAD LOW	51	LSB OUT
23	NC	50	BIT 9 OUT
24	LSB IN	49	BIT 8 OUT
25	NC	48	BIT 7 OUT
26	BIT 9 IN	47	BIT 6 OUT
27	BIT 8 IN	46	BIT 5 OUT
28	UP/$\overline{DN}$	45	READ HIGH
29	BIT 7 IN	44	READ LOW
30	BIT 6 IN	43	BIT 4 OUT
31	BIT 5 IN	42	BIT 3 OUT
32	BIT 4 IN	41	BIT 2 OUT
33	BIT 3 IN	40	MSB OUT
34	BIT 2 IN	39	CLOCK OUT
35	MSB IN	38	C_T
36	CLEAR	37	DIGITAL COMMON[1]

[1] PINS 19, 37 and 53 ARE INTERNALLY CONNECTED.

THEORY OF OPERATION

The ISO-DAC produces an isolated 4 to 20mA output current which is proportional to the input digital word. Each ISO-DAC contains a μcomputer compatible input section consisting of a 10-bit input latch, a 10-bit tri-state output and the associated control lines for read and write operations. A 10-bit CMOS digital-to-analog converter converts the digital word to a voltage that is modulated, carried across the isolation barrier, demodulated, and converted to a 4 to 20mA current output.

The remarkable performance of the ISO-DAC is derived from the carrier isolation technique which is used to transfer both signal and power between the input circuitry and the output stage. High CMV isolation, with excellent linearity, is achieved by the transformer coupling between the internal DAC, modulator section and the current output circuitry.
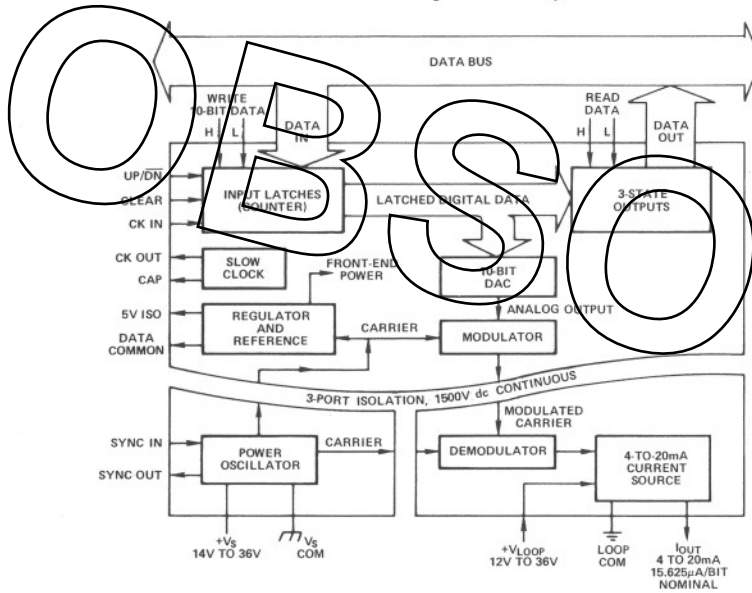

Figure 1. Block Diagram of the DAC1423

OFFSET AND SPAN ADJUSTMENTS

The DAC1423's initial offset and span accuracies are typically ±2LSB's (±0.2% FSR) each. If offset and span adjustments are not necessary, use the connections shown in Figure 2a.

Both offset and span errors are adjustable to zero with two external potentiometers, as shown in Figure 2b. To adjust the offset, apply a digital input of 0000000000 and adjust the offset potentiometer until an output of 4mA is obtained. Once the appropriate offset adjustment has been made, apply a digital input of 1111111111 and adjust the span potentiometer until 19.984mA is obtained. The offset and span adjustments are slightly interactive.

The offset and span potentiometers can provide a wide adjustment range to satisfy the particular needs of the application.

DIGITAL INPUT	NOMINAL CURRENT OUTPUT
Binary Code	
1111111111	+19.984mA
0000000001	+ 4.016mA
0000000000	+ 4.000mA

Table 1. Nominal Input-Output Relationships

The adjustment range of the span control will be typically ±10% full scale range (±2mA), while that of the offset control will be ±10% of offset (±0.4mA). Owing to the impedances involved, it is suggested that the adjustment pots be located near their respective connections or be well-guarded in order to avoid noise pickup.
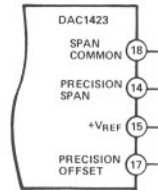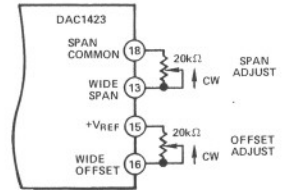

Figure 2a.   Figure 2b.

Figure 2. Precision and Adjustable Offset and Span

APPLICATION HINTS

The power supply should be carefully checked for noise, which would affect performance, and overshoot which could damage the device.

Unused digital inputs must always be grounded or taken to V_{DD} to ensure correct operation. Particular care should be taken when digital inputs are routed to another PC card. It is recommended that inputs open-circuited when PC cards are disconnected be taken to V_{DD} or GND via high value (1MΩ) resistors to prevent the accumulation of static charges.

ISOLATION CHARACTERISTICS

The DAC1423 employs a "three port" isolation architecture which allows for a great deal of flexibility in its application (see Figure 3). The power connections (pins 64, 66—68) are galvanically isolated from any other part of the module and may be subjected to the full common mode range with respect to either digital common or output common. Similarly, the output connections (pins 1, 6, 9) are isolated in the same manner from either power common or digital common.
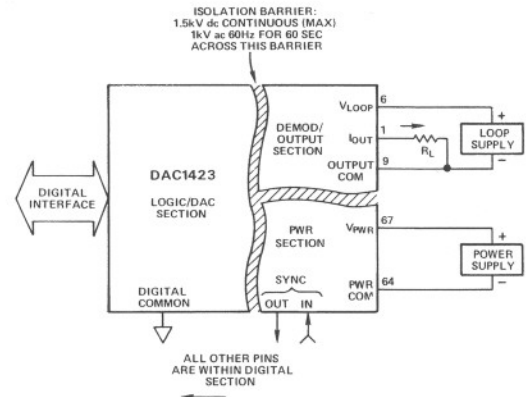

Figure 3. Illustration of Isolation Barrier Within the DAC1423

Figures 4 and 5 show two methods of utilizing the isolation characteristics of the DAC1423. In Figure 4, the DAC1423 is shown with separate loop supply and power supply. This configuration is useful when it is desirable to derive power for the module from the system without losing output isolation. This configuration is also useful when using external synchronization or multiple units, since the sync controls are referenced to power common. Figure 5 shows the use of a single supply for both power and loop current. This technique is useful when

the loop supply is the most secure power source, since the DAC1423 will remain operable even though the system has failed, as long as the loop supply continues to operate.
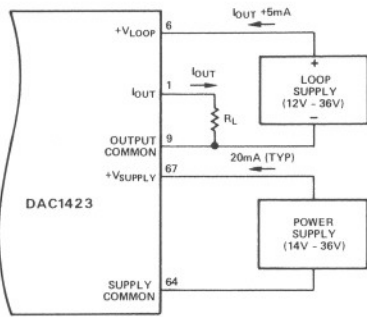

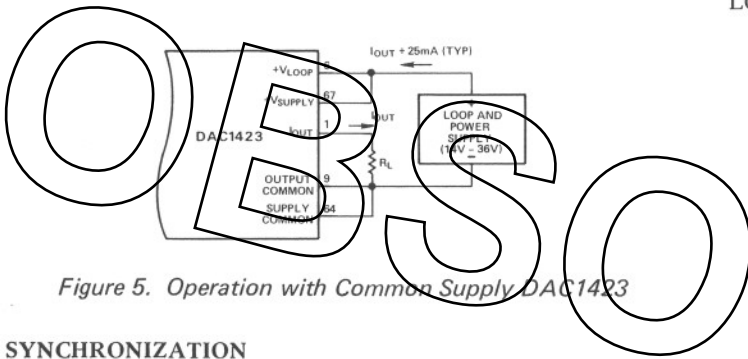Figure 4. Operation with Isolated Loop and Power Supplies DAC1423

Figure 5. Operation with Common Supply DAC1423

SYNCHRONIZATION

The DAC1423 contains an internal oscillator which generates the carrier frequency for the modulation process. In most cases, there is no appreciable leakage from this oscillator, and it may be ignored by the user. However, when a DAC1423 is used in a system which contains a clock at or near this carrier frequency, or when several DAC1423's are used adjacent to one another, it is possible that a heterodyning phenomenon can occur which results in beat notes that may (or may not) fall within the system's passband. For this reason, the DAC1423 contains provisions for external or multiple synchronization. Pin 68 is the SYNC IN pin which can be driven from an external clock. The external clock should be within 15% of free running frequency of the DAC1423 (200kHz ±15%). It should be a 5V CMOS level (50% duty cycle) via a 2200pF capacitor in series with pin 68.

If external sync is not used, leave the SYNC IN pin unconnected; the DAC1423 will free run at approximately 200kHz. Note that the SYNC IN signal is referred to power common, not loop common or digital common.

When multiple DAC1423's are used, it is recommended that their sync provisions be "daisy chained" as shown in Figure 6. The SYNC OUT pin of one DAC1423 is used as the external sync drive for the next DAC1423. Note that the first DAC1423 in the chain may either "free run" or be synchronized from an external source.
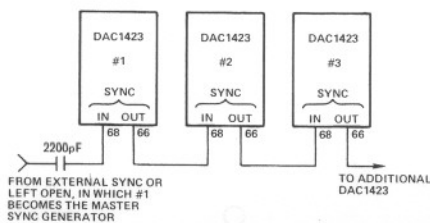

Figure 6. Synchronizing Multiple DAC1423's

The performance of the DAC1423 running in the sync mode is essentially no different from the free running mode, except that there may be slight offset and span shifts ($\approx$1LSB) if the carrier frequency is pulled appreciably from its free running frequency. In no case should the carrier frequency be pulled more than ±15% from its nominal free running frequency.

DIGITAL INTERFACE (PARALLEL)

The parallel interface of the DAC1423 is a 5V CMOS design, arranged to offer a great deal of interfacing flexibility to a variety of user systems.

The interface consists of a 10-bit input latch, a 10-bit tri-state output, and the associated control lines for read and write operations. As shown in Figure 7, the 8 lower bits and 2 upper bits of both the latch and the tri-state are separately controlled, allowing interfaces to both 8-bit and 16-bit bus architectures. For 10-bit or greater bus operation, the LO and HIGH write lines may be connected together, as well as the LO and HIGH read lines.
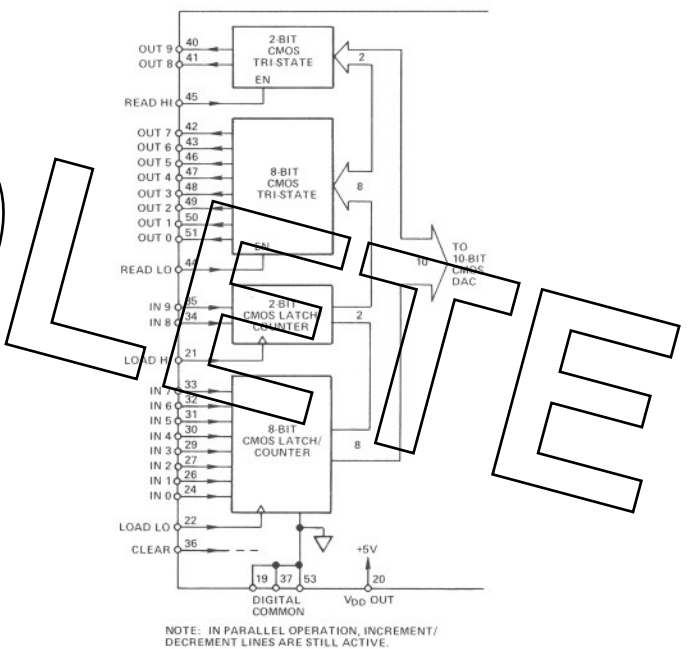

Figure 7. DAC1423 Digital Interface Architecture

An example of an 8-bit microprocessor interface is shown in Figure 8. In this case, the data is arranged as two bytes, right justified. The digital inputs to the DAC1423 are CMOS, therefore, rigid logic levels are required. In some cases, double buffering may be required for bus interface.

The output drive capability of the tri-states is 1 TTL load; in general, the DAC1423 may be used directly on most NMOS or CMOS microcomputer buses if the 3.3V minimum logic "1" level is observed. In some cases, pullups may be required.

In the event of computer failure, the bus inputs must go to either a high or a low state, but read, write and clear lines must go to a low state.

BUMPLESS TRANSFER

In process control applications, there will be times when the computer power fails and critical controls must be operated manually. To avoid causing a "bump" in the process, such as commanding a manually closed valve to fully open when switched to automatic control, it is essential that the computer knows the exact condition of the system when it resumes control. This is known as "bumpless transfer".

Bumpless transfer, when switching between automatic and manual control, is provided by the readback capability of the ISO-DAC's output tri-state logic. It constantly monitors the status of the input register; therefore, when switching from manual to automatic control, the computer can read the status of the ISO-DAC before resuming the algorithm.
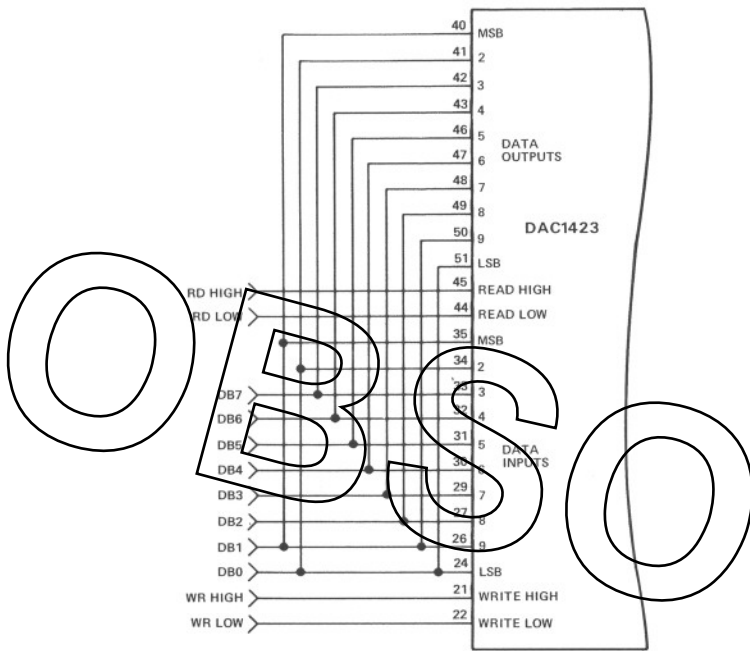
SYMBOL	MEANING	MIN	TYP	MAX	UNITS
t_{SD}	Strobe to Data Time	–	315	–	ns
t_{DS}	Data Set-Up Time	0	–	–	ns
t_{DH}	Data Hold Time	–	100	–	ns
t_{WS}	Write Strobe Width	–	100	–	ns
t_{OE}	Output Enable Time	–	100	–	ns
t_{OD}	Output Disable Time	–	80	–	ns
t_{CD}	Clock to Data Time	–	315	–	ns
t_{CW}	Clock Width	–	200	–	ns
t_{UDS}	Up/Down Set-Up Time	–	250	–	ns
t_{CR}	Clock Repetition Period	–	–	330	ns

Table 2. Timing Requirements

INCREMENT/DECREMENT CONTROL

Increment/decrement operation under computer or manual control is possible with the input latch/counter in the DAC1423. The DAC1423 also contains overflow/underflow lockout circuitry, and a slow speed clock output is provided. The timing diagram shown in Figures 9 and 10 give guidelines for increment/decrement operation. Figure 11 shows the ISO-DAC in the manual back-up mode using increment/decrement control logic. In this circuit, part of Z_1 latches the direction line, UP/$\overline{DN}$. Z_2 and the remainder of Z_1 gate the clock "on"—after one RC time delay. The RC time delay is determined by R_T and C_T which the user supplies. The same circuit could be used for computer control by simply replacing the pushbutton switch with the proper logic.

Figure 8. Typical Interface to 8-Bit μComputer
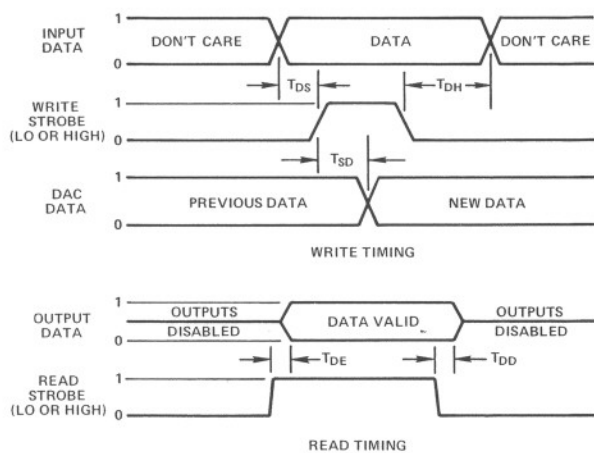
Figure 9. Read/Write Timing

¹REPRESENTS DATA PRESENTED TO X-STATE AND DAC INPUTS
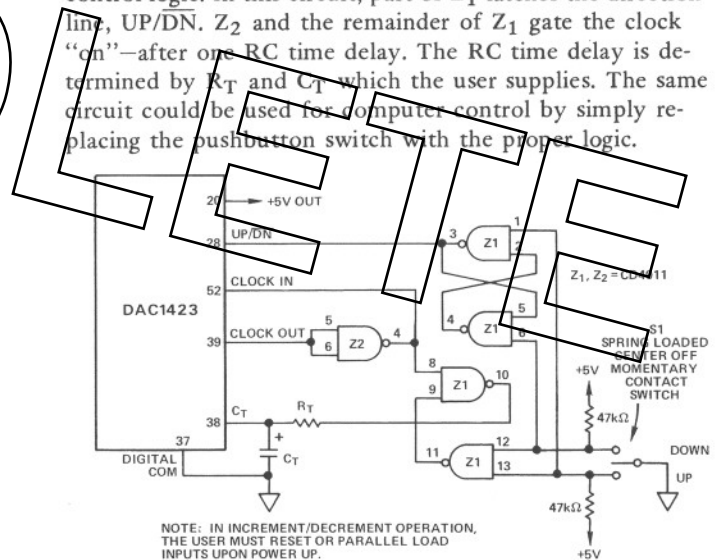²SAME CHARACTERISTIC OCCURS WHEN DECREMENTED TO ZERO
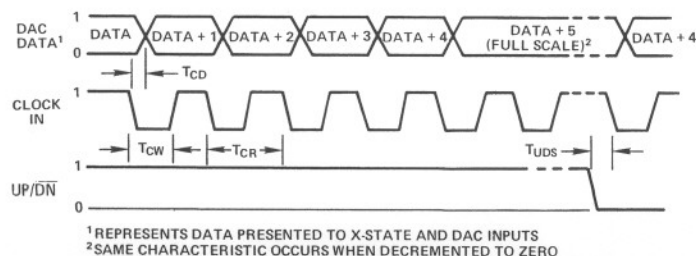
Figure 10. Increment/Decrement Timing

NOTE: IN INCREMENT/DECREMENT OPERATION, THE USER MUST RESET OR PARALLEL LOAD INPUTS UPON POWER UP.

Figure 11. Increment/Decrement Control

SLOW CLOCK OPERATION

The DAC1423 provides a slow speed clock circuit for the user's convenience in operating the increment/decrement feature. This clock requires a resistor and capacitor to set its operating frequency, as shown in Figure 12. When the slow clock is not used, connect pin 38 to digital common (pin 37) and disable the slow clock to prevent any feedthrough of the clock signal to the output.
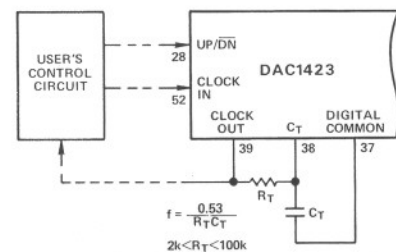

$$f = \frac{0.53}{R_T C_T}$$

$2k < R_T < 100k$

Figure 12. Using the Slow Clock

CLEAR

In many industrial controls, it is desirable to have the ISO-DAC go to a known state when the system is first powered up. The clear pin, pin 36, is provided for just such cases. Strobing the clear pin will reset the input latch/counter to all 0's. Tying pin 36 to the computer reset bus provides an asynchronous means to initiate the system to a known state.

+5V OUTPUT

A +5V output is provided for powering a small amount of user supplied circuitry. This output is referred to digital common and is, therefore, isolated both from the loop and from the power supply. The outboard devices may draw up to a maximum of 0.5mA from this pin (pin 20); however, it is suggested that the user by-pass this pin to digital common with a 0.1μF or greater capacitor in order to avoid externally injected glitches from disturbing the internal circuitry of the DAC1423.

AC1582 MOUNTING CARD

The AC1582 mounting card is available to assist in evaluating the DAC1423. As shown in Figure 13, the AC1582 is an edge connector card with pin receptacles for plugging in the DAC1423. This card includes offset and span adjustment potentiometers, power supply by-pass capacitors and the logic needed for increment/decrement control. Increment/decrement is enabled via connection to J2. In addition, the card allows for several user selectable configurations:

1. 8- or 16-bit bus interface;
2. Single supply for both power and loop current. Supply delivered via P_1 or TB_1;
3. Separate loop supply and power supply;
4. Offset and Span—fixed or adjustable.

These configurations can be programmed by user-installed jumpers, as shown in the wiring chart of Table 3. Jumper locations are not shown in Figure 13, but are labeled on the mounting card.
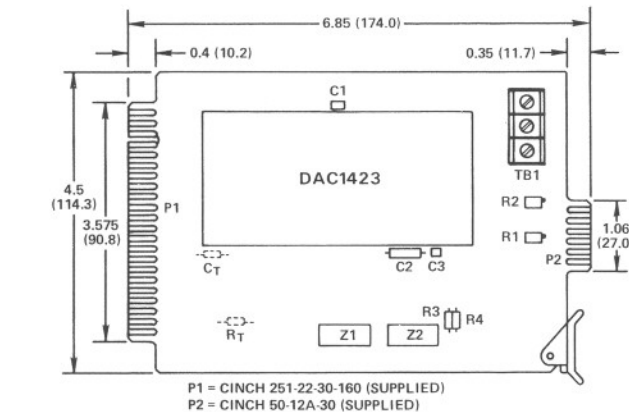
P1

PIN	FUNCTION	PIN	FUNCTION
1	MSB IN	A	MSB OUT
2	BIT 2 IN	B	BIT 2 OUT
3	BIT 3 IN	C	BIT 3 OUT
4	BIT 4 IN	D	BIT 4 OUT
5	BIT 5 IN	E	BIT 5 OUT
6	BIT 6 IN	F	BIT 6 OUT
7	BIT 7 IN	H	BIT 7 OUT
8	BIT 8 IN	J	BIT 8 OUT
9	BIT 9 IN	K	BIT 9 OUT
10	LSB IN	L	LSB OUT
11	WRITE HIGH	M	READ HIGH
12	WRITE LOW	N	READ LOW
13	CLEAR	P	DIGITAL COMMON
14	NC	R	+5V_{OUT}
15	NC	S	NC
16	NC	T	NC
17	+V POWER	U	PWR COMMON
18	SYNC IN	V	SYNC OUT
19	NC	W	NC
20	NC	X	NC
21	+V_{LOOP}	Y	LOOP COMMON
22	NC	Z	NC

P2

PIN	FUNCTION
A	DIG COM
B	DECREMENT
C	INCREMENT

TB1

PIN	FUNCTION
1	+V_{LOOP}
2	I_{OUT}
3	LOOP COMMON

Table 3. AC1582 Mounting Card Connector Designations

Options	User-Installed Jumpers[1]
8-Bit Bus Interface	J1, J2, J4, J5
16-Bit Bus Interface	J3, J6
Single Supply	J7, J8, J13, J14
Dual Supply (V_{LOOP} via P1)[2]	J13, J14
Offset and Span, Fixed	J10, J12
Offset and Span, Adjustable	J9, J11

Notes:
[1] Jumper locations are not shown in Figure 13, but are labeled on AC1582.
[2] Loop supply normally accessible via TB1.

P1 = CINCH 251-22-30-160 (SUPPLIED)
P2 = CINCH 50-12A-30 (SUPPLIED)

Figure 13. AC1582 Mounting Card.
Dimensions shown in inches and (mm).

NOTES
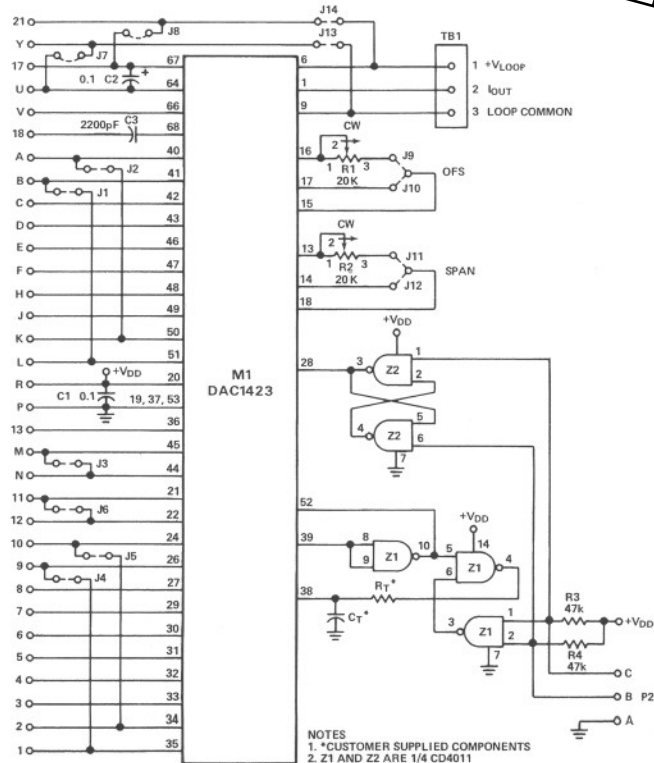1. *CUSTOMER SUPPLIED COMPONENTS
2. Z1 AND Z2 ARE 1/4 CD4011

Figure 14. Schematic Diagram for AC1582 Mounting Card