High Resolution, Digital to Analog Converter

DAC-14/16QM, DAC-QG

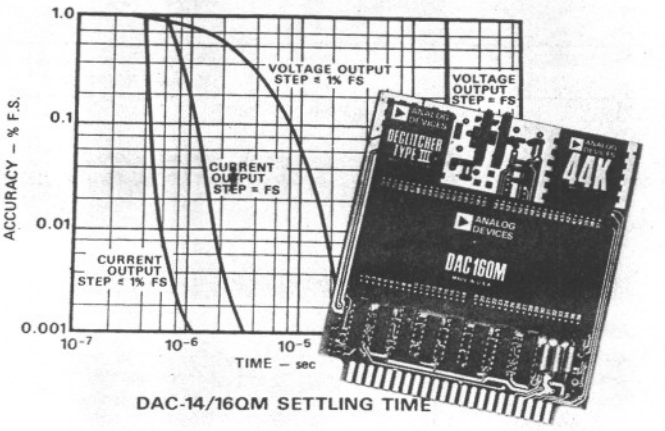
FEATURES

DAC-14/16QM

- 16 Bit Resolution
- Linearity Error Less Than: ±0.0015% (16 Bit Model)
  ±0.003% (14 Bit Model)
- Monotonic
- Compact 2" x 4" x 0.4" Module
- DTL/TTL Compatible

DAC-QG

- Versatile Input Register
- Many Code Options
- Optional Amplifiers for Fastest Settling or Highest Stability
- Optional Transient Suppressor
- 4 Terminal Output Connection



DAC-14/16QM SETTLING TIME

GENERAL DESCRIPTION OF THE DAC-14/16QM

The DAC-14/16QM high resolution digital to analog converters are compact 2" x 4" x 0.4" modules that offer true state-of-the-art performance in applications demanding the utmost in resolution and accuracy. Both units feature 16 bit resolution. The DAC-14QM has a maximum linearity error of 0.003% (at +25°C) while the DAC-16QM has a maximum linearity error of only 0.0015% (at +25°C).

DESCRIPTION OF THE DAC-QG

The DAC-QG is a manifold board which accepts any DAC-QM from 8 to 16 bits and offers several optional circuit supplements. The library of options includes: a "deglitcher" for limiting switching transients to 2 millivolts; a versatile input register with provisions for one of five input codes; and a choice of high-performance discrete output amplifiers to attain either optimum settling time, optimum stability, or lowest cost by using the IC amplifier contained in the DAC-QM. The DAC-QG also contains the offset and gain adjust potentiometers required by the DAC-QM.

DESIGN CONSIDERATIONS

Extreme care is required in the design, production, and application of converters such as the DAC-14/16QM/QG in order to insure that the fine resolution, broad dynamic range, and the high degree of accuracy and linearity expected of these precision devices is actually achieved. Factors of only secondary concern in the design of 12 bit converters can have an overwhelmingly adverse impact on the operation of a 16 bit unit. Consider the fact that a 16 bit converter with a 10VFS output range has an LSB of only 153μV! Problems such as thermocouple effects, voltage drops in connectors, low level noise, radio frequency interference and output amplifier temperature drift simply cannot be ignored. Several practical installation guidelines are offered in the following sections to help the user avoid these problems. Reprints of a two part series written for Electronics magazine by the staff of Analog Devices, Inc. discussing the details of high resolution data conversion are also available to aid in the application of these devices.

PERFORMANCE

Analog Devices, Inc. is committed to an extensive testing program which assures the customer that every unit received is truly the precision device described in this data sheet. Some very visible results of this program are the three documents shipped with every converter. The first certifies calibration with methods and equipment traceable to the National Bureau of Standards. The second certifies the performance of the converter's internal reference zener over temperature and over 1000 hours of burn-in. The third shows the actual linearity deviation of the converter by means of a recording which plots the difference between the converter's output and the output of a super-precision DAC at each of the 65,536 possible input words.

Ten-thousand hours of testing were also performed in order to actually measure the long-term stability of these devices. The impressive result was a linearity shift of less than 8ppm/10,000 hours!

SPECIFICATIONS (typical @ +25°C and rated supply voltages, unless otherwise noted)

MODEL	QM	QG (THE QM ON A CARD MOUNTED ASS'Y) WITH IC AMP	WITH 184L	WITH 44K
RESOLUTION	16 Bits	*	*	*
LINEARITY				
(Straight Line – Zero to FS)	Monotonic	*	*	*
DAC-16 XX	±<0.0015%	*	*	*
DAC-14 XX	±<0.003%	*	*	*
DIGITAL INPUTS				
(DTL/TTL Compatible)				
Logic "0"	0V <E_0 <+0.8V @ –3mA	0V <E_0 <+0.8V @ –1.6mA	**	**
Logic "1"	+2.0V <E_1 <+5.0V @ 10μA	+2.0V <E_1 <+5V @ 20μA	**	**
CODE OPTIONS	Compl. Binary (CB)	Binary, BCD, 2's Compl. BIN,	**	**
	Compl. BCD (CBD)	Sign Plus Mag. BIN/BCD	**	**
OUTPUT				
Current Mode	0 to –2mA (CB) (CBD)	Voltage Mode Output Only		
	±1mA (CB)			
Source Impedance	15,000Ω ±0.01% (CB)			
	9,000Ω ±0.01% (CBD)			
Voltage Mode	0 to +10V (CB) (CBD)	0 to +10V (Unipolar Codes)	*	*
	±5V, ±10V (CB)	±5V, ±10V (Bipolar Codes)	*	*
Output Impedance	<1Ω	*	<0.001Ω	<0.05Ω
Output Current	±1mA (Int. Amp)	*	±2mA	±10mA
DYNAMIC RESPONSE				
Current Mode		Voltage Mode Output Only		
Settling Time	(See Figure 1)			
Peak Noise (worst case)	50% FS, 300ns			
rms Noise (10Hz to 1MHz)	±50μV			
Voltage Mode				
Settling Time	(See Figure 1)	(see Figure 2a, 2b)	*	*
Peak Noise (worst case)	2% FS, 5μs	(see Figure 3)	*	*
rms Noise (10Hz to 1MHz)	<0.0001% FS	*	<0.0002% FS	
REFERENCE				
Internal	+6.00V ±0.01% (±5ppm/°C)	*	*	*
ADJUSTMENTS				
Gain	(User Supplied)	(Provided)	**	**
Unipolar Offset	50Ω Pot	≈0.1% FS Range	**	**
Bipolar Offset	100kΩ Pot	≈0.07% FS Range	**	**
Dynamic Zero	20Ω Pot	≈0.15% FS Range	**	**
POWER REQUIREMENTS				
+5V dc ±10%	@ 40mA	@ 220mA	*	*
+15V dc ±2%	@ 20mA	@ 35mA	*	*
–15V dc ±2%	@ 50mA	@ 65mA	*	*
POWER SUPPLY SENSITIVITY[2]				
Current Mode		Voltage Mode Output Only		
Gain	±7ppm			
Unipolar Offset	±<1ppm			
Bipolar Offset	±<7ppm			
Voltage Mode				
Gain	±7ppm	±<10ppm	±<15ppm	±<30ppm
Unipolar Offset	±<2.5ppm	±<4ppm	±<1ppm	±<10ppm
Bipolar Offset	±5ppm	±<10ppm	±<7ppm	±<15ppm
TEMPERATURE COEFFICIENT				
(Expressed in ppm of FS/°C)				
Gain	±<1ppm (exclusive of reference)	±15ppm[3]	±7ppm[3]	±30ppm[3]
Unipolar Offset	±<1ppm	±9ppm	±0.5ppm	±25ppm
Bipolar Offset	±<3ppm	±15ppm	±7ppm	±7ppm
RECOMMENDED RECALIBRATION				
Interval		30 Days	*	*
TEMPERATURE RANGE				
Operating Within Specs	+20°C to +30°C	*	*	*
Operating	0 to +70°C	*	*	*
Storage	–55°C to +125°C	*	*	*
DIMENSIONS	Module: 2" x 4" x 0.4"	CARD: 4½" x 4¾"	**	**

[1] 16 Bit BCD (4 decimal digits) priced same as 14 Bit Binary.
[2] Expressed in ppm of FS/% change in ±15V supplies.
[3] Includes ±5ppm for reference.

*Specifications same as QM.
**Specifications same as QG with IC Amp.
Specifications subject to change without notice.

INSTALLATION

The following installation guidelines are offered to help minimize the potential causes of error discussed previously:

1. Locate the unit and the wiring to its connector so as to provide optimum isolation from sources of RFI and EMI.
2. Attempt to locate the unit and its connector in a plane of thermal equipotential. It must be appreciated that popular electronic wiring materials usually involve different metals, and the junctions will act as thermocouples if they are located in regions of differing temperature.
3. It is important to connect the +5V logic supply common (usually a carrier of pulse noise) to the analog supply common at a point that minimizes system noise.
4. When using the DAC-QG, the user must properly connect the four-terminal output amplifier to allow inherent circuit compensation for contact resistance.

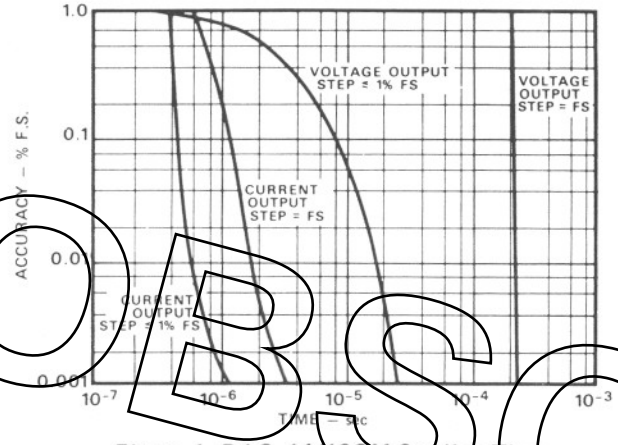


Figure 1. DAC-14/16QM Settling Time

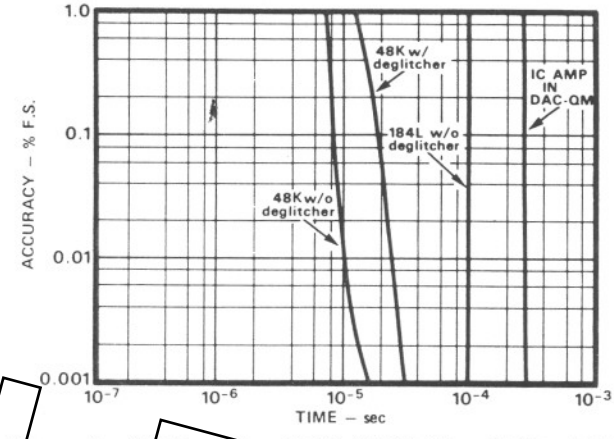


Figure 2a. Settling Time DAC-16QG, Step ∓FS to ±FS

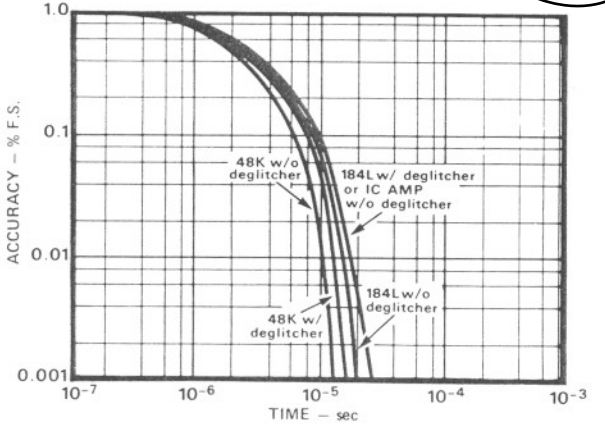


Figure 2b. Settling Time DAC-16QG, Step ≤1% FS

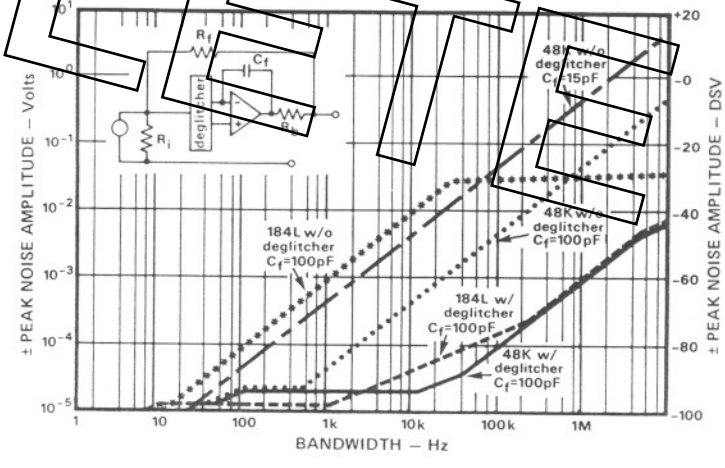


Figure 3. DAC-16QG, ±Peak Noise vs. Bandwidth

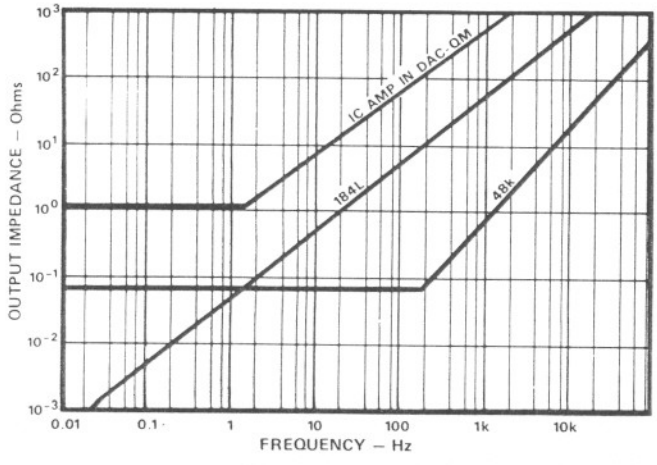


Figure 4. Output Impedance vs. Frequency

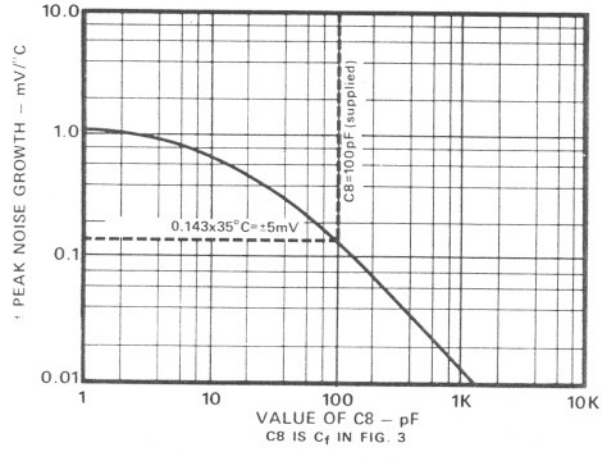


Figure 5. ±Peak Noise Growth per °C vs. Value of C8 (cf) when using Deglitcher

INPUT CODING

The DAC-14/16QM accepts data directly at its μDAC switch inputs and is available with either complementary binary (used as complementary offset binary for bipolar operation) and complementary BCD codes.

OUTPUT PROGRAMMING

The output amplifier circuit of the DAC-14/16QM is jumper programmed at the module terminals, allowing the user to determine which of the three possible output ranges will be used. Feedback resistance value is determined according to the following table by jumpers at pins 68 and 70 which provide 10k (8k for BCD units) and 5k ohms respectively.

OUTPUT RANGE	FEEDBACK RESISTOR	OFFSET ADJUST	ZERO ADJUST
0 to +10V	Complementary Binary: Connect 47 to 70 Complementary BCD: Connect 47 to 68	Ground 46	Connect 71 to Zero Adjust Pot
±10V	Complementary Offset Binary: Connect 47 to 68	Connect 44, 46 to Offset Adjust Pot	Not Connected
±5V	Complementary Offset Binary: Connect 47 to 70	Connect 44, 46 to Offset Adjust Pot	Not Connected

RANGE PROGRAMMING TABLE

ADJUSTMENT PROCEDURE

A voltmeter capable of 1/10LSB resolution and accuracy (e.g., 15μV for a 16 bit DAC) at both ends of the DAC-QM's output range is required. The accuracy of the converter subsequent to calibration is directly dependent upon the accuracy of the voltmeter.

The user must supply a 50Ω gain adjust pot (connected as shown in Figures 6, 7). This is used to adjust the output range to desired full scale values after the zero point has been set.

For unipolar (0 to +10V) operation, the user must supply a 100kΩ zero adjust pot (connected as shown in Figure 6) in addition to the gain adjust pot. To adjust the zero point apply the input code that should result in an output of zero. Adjust the zero pot until an output of 0V ±1/10LSB is obtained.

For bipolar operation (±5V, ±10V) the user must supply a 20Ω offset adjust pot (connected as shown in Figure 7) in addition to the gain adjust pot. To adjust the zero point, apply the input code that should result in an output of zero. Adjust the offset pot until an output of 0V ±1/10LSB is obtained.

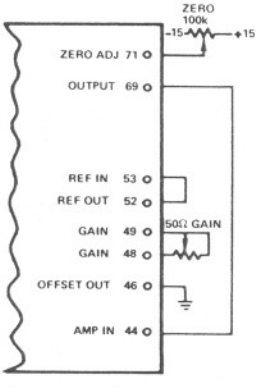


Figure 6. Connections for Unipolar Operation

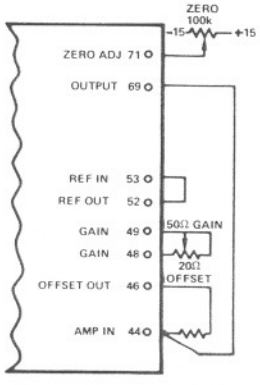
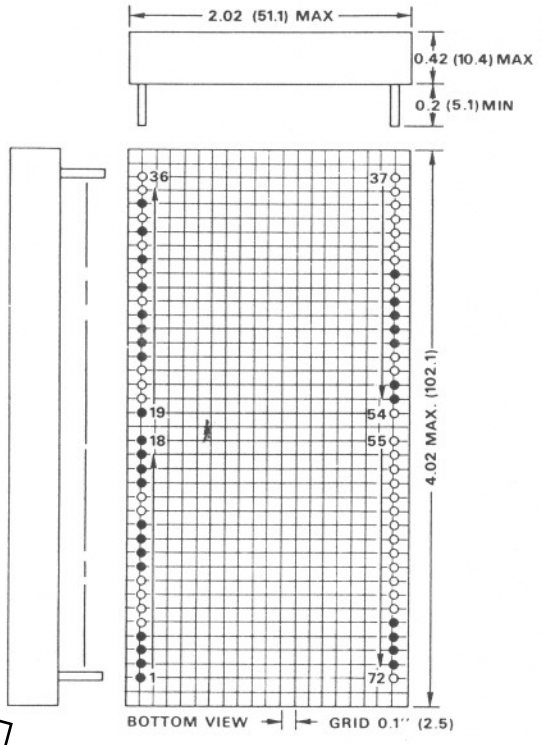


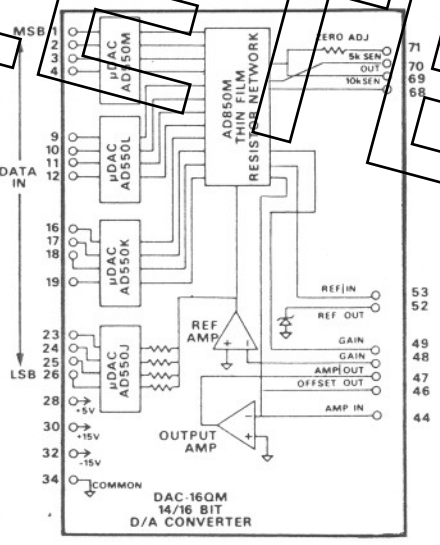
Figure 7. Connections for Bipolar Operation

OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (mm).



BLOCK DIAGRAM AND PIN DESIGNATIONS



ORDERING GUIDE:

DAC-	XX Linearity	QM	/XXX
	14 Bits 16 Bits		C-B (Complementary Binary) CBD[1] (Complementary BCD)

Note:
[1] CBD available only in 16-bit resolution

INPUT OPTIONS

The DAC-QG can be ordered with direct input, or in the case of the 14/16 bit models with the optional input register. When direct input is chosen, the user may only select one of the codes which is standard for the particular DAC-QM which is mounted. When the optional input register is chosen, the user may select any one of the following codes: Binary, 2's Complement, Sign plus Magnitude Binary, BCD, Sign plus Magnitude BCD. The code ordered by the user is set at the factory by means of various jumpers in the logic circuitry.

STROBE CHARACTERISTICS OF OPTIONAL REGISTER

Figure 8 shows the idealized strobe characteristics of the optional input register. The system utilizes a dynamic strobe circuit, transferring input data to the register essentially at the time of the leading edge of the strobe pulse. Due to the extremely wide dynamic range of operation of the DAC-16QG, it is an important consideration to operate all circuits in optimum noise modes. For instance, the DAC-16QG will operate when its strobe rise time is faster than indicated, but the larger high frequency content on the fast leading edge is liable to leak through the circuit and cause detectable noise at the output. In the same way, noise caused by the strobe trailing edge is inherently minimized by the circuit unless the trailing edge occurs much longer than 500ns after the leading edge. Here again, the circuit will work properly with the long strobe, but it is likely that detectable noise will appear at the output.

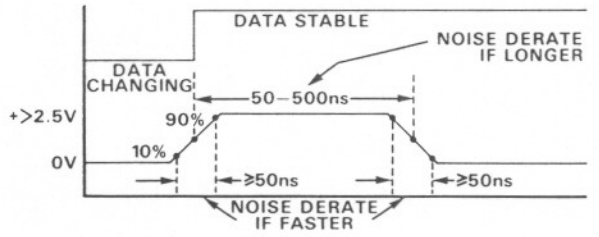


Figure 8. DAC-14/16QG Strobe with Optional Input Register

CONVERTER OPTIONS

The DAC-QG is normally ordered with the DAC-14/16QM. However, any converter in the DAC-QM line, such as the DAC-12QM, could be used, thereby providing it with transient suppression and a high performance output amplifier.

OUTPUT OPTIONS

The user can choose one of three standard output amplifier options. The first is the economical IC amplifier internal to the DAC-QM module; the second is the ultra-low drift model 184L chopperless amplifier, and the third is the fast settling model 44K amplifier.

Regardless of the amplifier chosen, the user may select any one of three output ranges by installing jumpers between terminals on the circuit board. Figure 9 shows the location of these terminals. The range programming table shows the proper connections to make to obtain the desired output range.

When the 2's complement or the Sign plus magnitude binary codes have been chosen, the ±5V or ±10V range may be used. When the Binary or BCD codes have been chosen, the +10V range may be used. When the Sign plus magnitude BCD code is used, the ±10V connections are made. However, the output range for the 16 bit converter will actually be ±8V which corresponds to the maximum code of ±7.999 for the 15 bits plus sign.

The Deglitcher Type II is also available as an option to limit converter switching transients to 0.2 millivolts. Since these switching transients are seen in all digital to analog converters due to the fact that switch turn-off time is not exactly the same as switch turn on time, the Deglitcher Type II is a key contributor to true state-of-the-art performance in the DAC-QG.

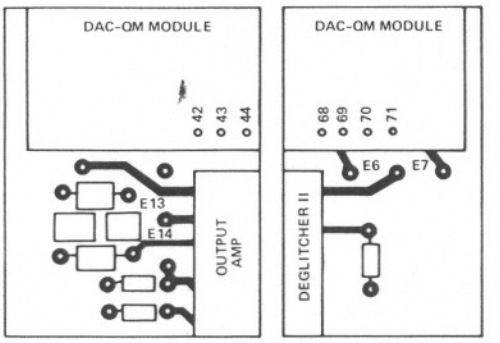


Figure 9. Top View of Portions of Circuit Board Showing Locations of Range Program Jumpers

JUMPER	E6	E7	E13	E14
0 to +10V	Not Connected	Connected	Not Connected	Connected
±5V	Not Connected	Connected	Connected	Not Connected
±10V	Connected	Not Connected	Connected	Not Connected

RANGE PROGRAMMING TABLE

OUTPUT CONNECTIONS

A four terminal output connection is utilized on the DAC-QG in order to allow inherent circuit compensation of connector contact resistance. To take advantage of this feature, the user must make connection of the "sense" lines (terminals 18 and 21) as close as possible to the actual loads.

It is important to connect the +5V logic supply common (usually a carrier of pulse noise) to the analog supply common at a point that minimizes system noise. The commons are kept isolated in the DAC-QG.

Figure 10 illustrates the proper output and grounding connections.

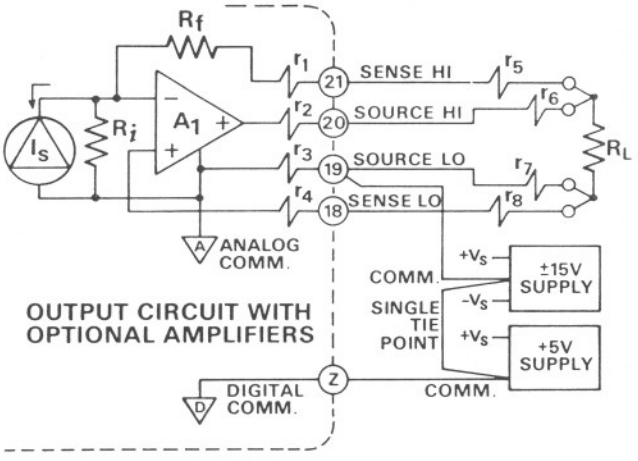


Figure 10. Output and Grounding Connections

ADJUSTMENT PROCEDURE

A voltmeter capable of 1/10LSB resolution and accuracy (e.g., 15μV for a 0 to +10V, 16 bit DAC) at both ends of the DAC-QG's output range and an oscilloscope are required. The accuracy of the converter subsequent to calibration is directly dependent upon the accuracy of the voltmeter.

The zero adjustment should be made first, followed by the offset adjustment, and then the gain adjustment.

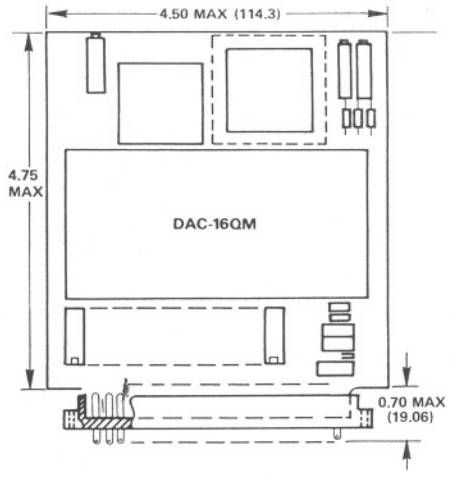
Zero adjustment (R3): with an oscilloscope connected to the DAC-QG's output, and any input code, apply a repetitive strobe pulse to the strobe input. Adjust R3 to minimize the height of glitches that occur with each strobe pulse.

Offset adjustment (R2): connect the voltmeter to the DAC-QG's output. For unipolar units, strobe the input code that should result in an output of zero. Adjust R2 until the converter's output is within ±1/10LSB of zero. For bipolar units, strobe in the code that should give minus full scale. Adjust R2 until the output reads minus full scale within ±10LSB. If the offset adjustment potentiometer's range is not sufficient to complete the adjustment, back it off one revolution and use the zero adjustment potentiometer (R3) to finish the adjustment.

Gain adjustment (R4): strobe in the input code that should give a positive full scale output. Adjust R4 until the DAC-QG's output reads plus nominal full scale minus 1LSB within ±1/10LSB.

OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (cm).



CINCH CONNECTOR 251-22-30-160 (SUPPLIED)

PIN	FUNCTION	PIN	FUNCTION
1–17	N.C.	K	BIT 9
18	ANALOG SENSE LOW	L	BIT 10
19	ANALOG SOURCE LOW	M	BIT 11
20	ANALOG SOURCE HIGH	N	BIT 12
21	ANALOG SENSE HIGH	P	BIT 13
22	ANALOG REF. IN/OUT	R	BIT 14
A	BIT 1 (MSB)	S	BIT 15
B	BIT 2	T	BIT 16 (LSB)
C	BIT 3	U	STROBE
D	BIT 4	V	N.C.
E	BIT 5	W	+5V
F	BIT 6	X	+15V
H	BIT 7	Y	-15V
J	BIT 8	Z	GRD

ORDERING GUIDE

DAC-XX QG / XXX / XXX / XXXX / XXX / XXXX

INPUT		OUTPUT AMPLIFIER	
REG	REGISTER	STND	INTERNAL AMP
DIR	DIRECT	FAST	44K
		STAB	184L

LOGIC CODE	
BIN	BINARY
2SC	TWO'S COMPLEMENT
SMB	SIGN PLUS MAGNITUDE BINARY
BCD	BINARY CODED DECIMAL
SMD	SIGN PLUS MAGNITUDE BCD

RESOLUTION	REFERENCE	
08	INT	INTERNAL
10	EXT	EXTERNAL
12		
14		
16		

DEGLITCHER	
DEGL	DEGLITCHER II (USE WITH FAST OR STAB AMP)
NONE	NO DEGLITCHER (USE WITH ANY AMP)